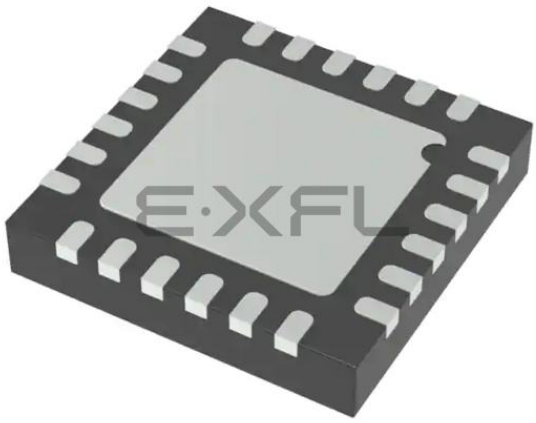
Infineon Technologies - XMC1100Q024F0016ABXUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-24-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100q024f0016abxuma1

XMC1100

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex™-M0
32-bit processor core

Data Sheet

V1.4 2014-05

Microcontrollers

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

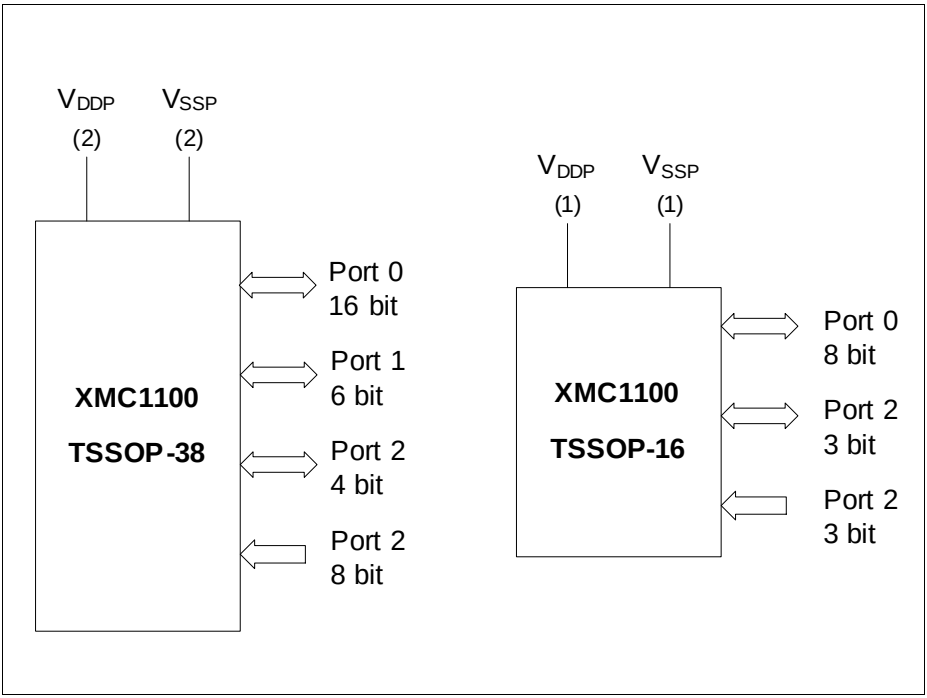


Figure 2 XMC1100 Logic Symbol for TSSOP-38 and TSSOP-16

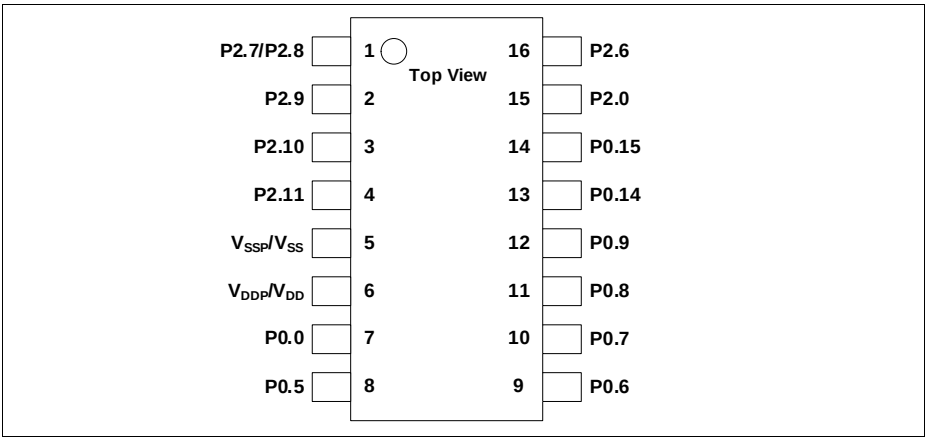


Figure 5 XMC1100 **PG-TSSOP-16 Pin Configuration** (top view)

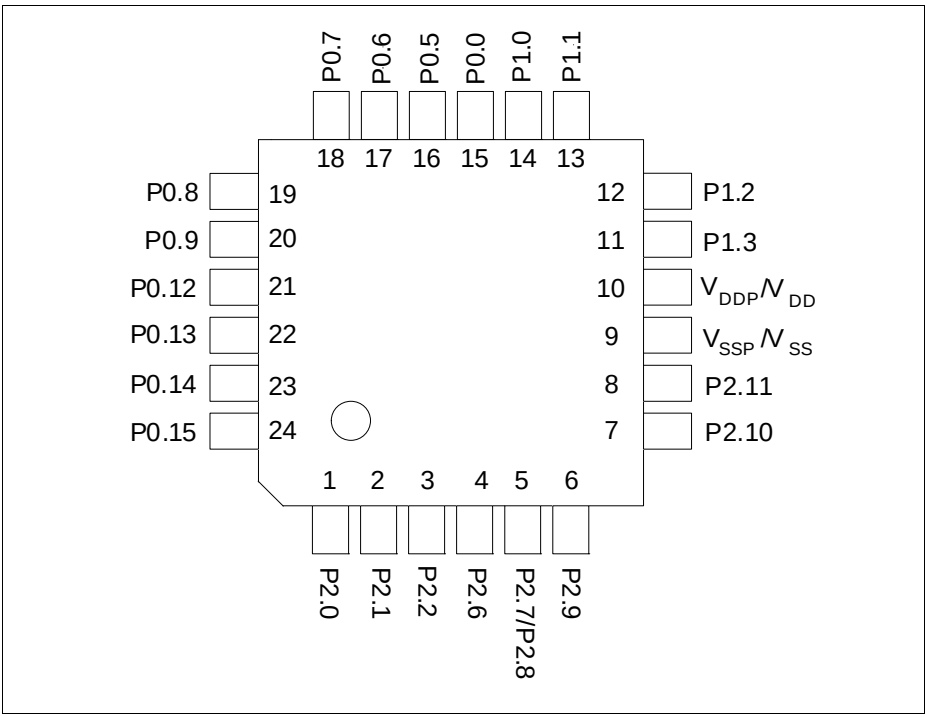


Figure 6 XMC1100 **PG-VQFN-24 Pin Configuration** (top view)

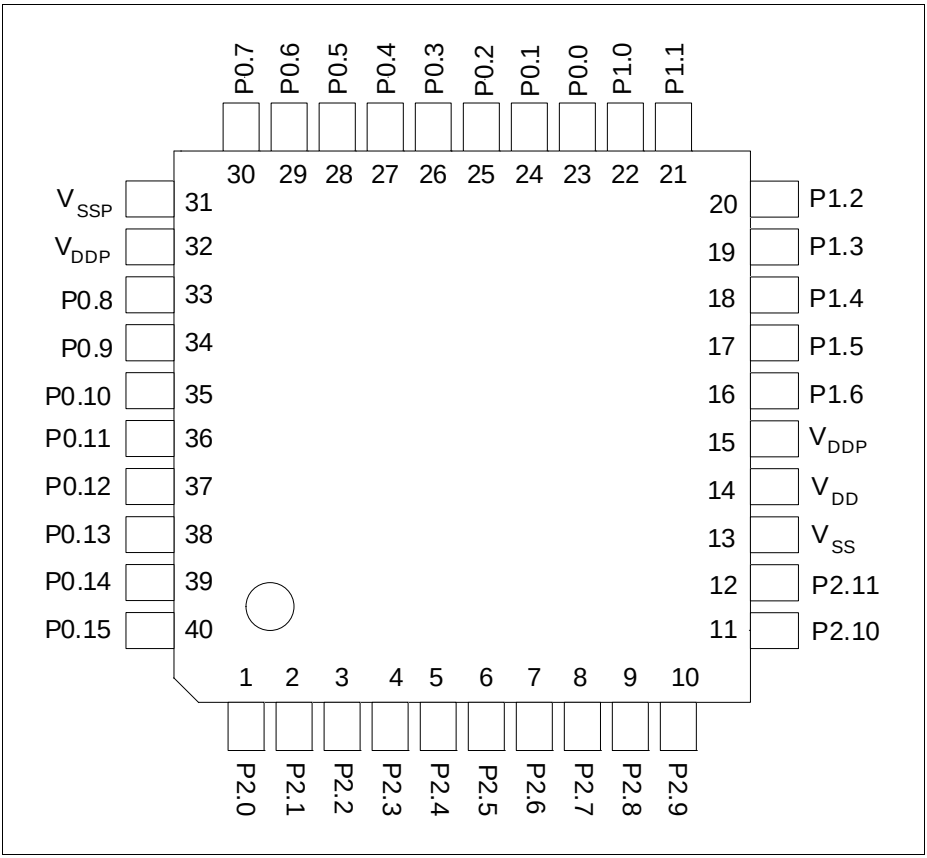


Figure 7 XMC1100 **PG-VQFN-40 Pin Configuration** (top view)

Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (TSSOP28/16, VQFN24)	I_{MVDD1}	SR	–	130	mA	3)
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	3)
Maximum current out of V_{SS} (TSSOP28/16, VQFN24)	I_{MVSS1}	SR	–	130	mA	3)
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	3)

1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Not subject to production test, verified by design/characterization.

4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

Table 12 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC		1		–	GNCTRxz.GAINy = 00_B (unity gain)
			3		–	GNCTRxz.GAINy = 01_B (gain g1)
			6		–	GNCTRxz.GAINy = 10_B (gain g2)
			12		–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	V_{DDP} = 5.0 V
		3	–	–	1 / f_{ADC}	V_{DDP} = 3.3 V
		30	–	–	1 / f_{ADC}	V_{DDP} = 1.8 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC		9		1 / f_{ADC}	2)
Conversion time in 12-bit mode	t_{C12} CC		20		1 / f_{ADC}	2)
Maximum sample rate in 12-bit mode 3)	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC		18		1 / f_{ADC}	2)
Maximum sample rate in 10-bit mode 3)	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC		16		1 / f_{ADC}	2)

3.2.3 Temperature Sensor Characteristics

Table 13 Temperature Sensor Characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[2)]	T_{TSAL} CC	–	+/-20	–	°C	T_J = -40 °C (calibrated)
		–	+/-12	–	°C	T_J = -25 °C (calibrated)
		-5	–	5	°C	T_J = 0 °C
		-2	–	2	°C	T_J = 25 °C (calibrated)
		-4	–	4	°C	T_J = 70 °C
		-2	–	2	°C	T_J = 115 °C (calibrated)

1) Not subject to production test, verified by design/characterization.

2) The temperature sensor accuracy is independent of the supply voltage.

3.3 AC Parameters

3.3.1 Testing Waveforms

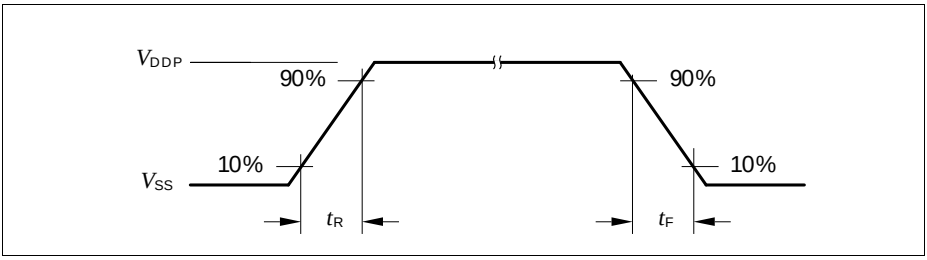


Figure 9 Rise/Fall Time Parameters

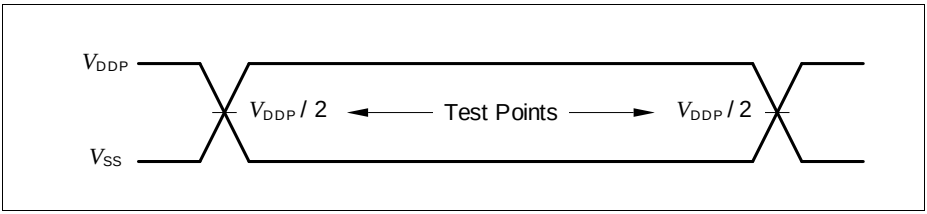


Figure 10 Testing Waveform, Output Delay

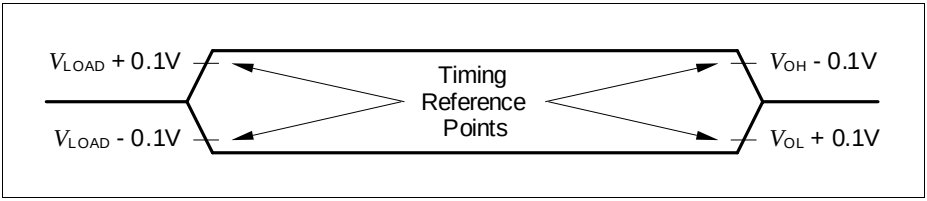


Figure 11 Testing Waveform, Output High Impedance

3.3.2 Output Rise/Fall Times

Table 17 provides the characteristics of the output rise/fall times in the XMC1100. **Figure 9** describes the rise time and fall time parameters.

Table 17 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on High Current Pad[1)2)]	t_{HCPR}, t_{HCPF}	–	9	ns	50 pF @ 5 V[3)]
		–	12	ns	50 pF @ 3.3 V[4)]
		–	25	ns	50 pF @ 1.8 V[5)]
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	12	ns	50 pF @ 5 V[6)]
		–	15	ns	50 pF @ 3.3 V[7)].
		–	31	ns	50 pF @ 1.8 V[8)].

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
4) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
7) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
8) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.

3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

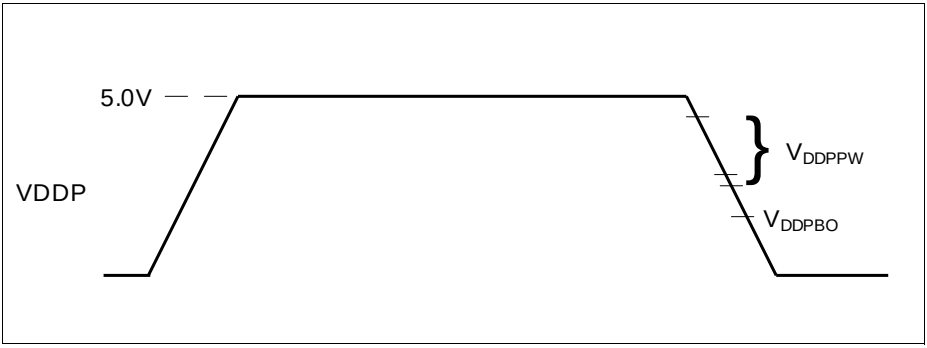


Figure 12 Supply Threshold Parameters

3.3.4 On-Chip Oscillator Characteristics

Table 19 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1100.

Table 19 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	63.5	64	64.5	MHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)[2]
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[2]
Accuracy with calibration based on temperature sensor	Δf_{LTT}	CC	-1.3	–	1.25	%	with respect to f_{NOM}(typ), over temperature (T_A = 0 °C to 105 °C)[2]
			-2.6	–	1.25	%	with respect to f_{NOM}(typ), over temperature (T_A = -40 °C to 105 °C)[2]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

Figure 13 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

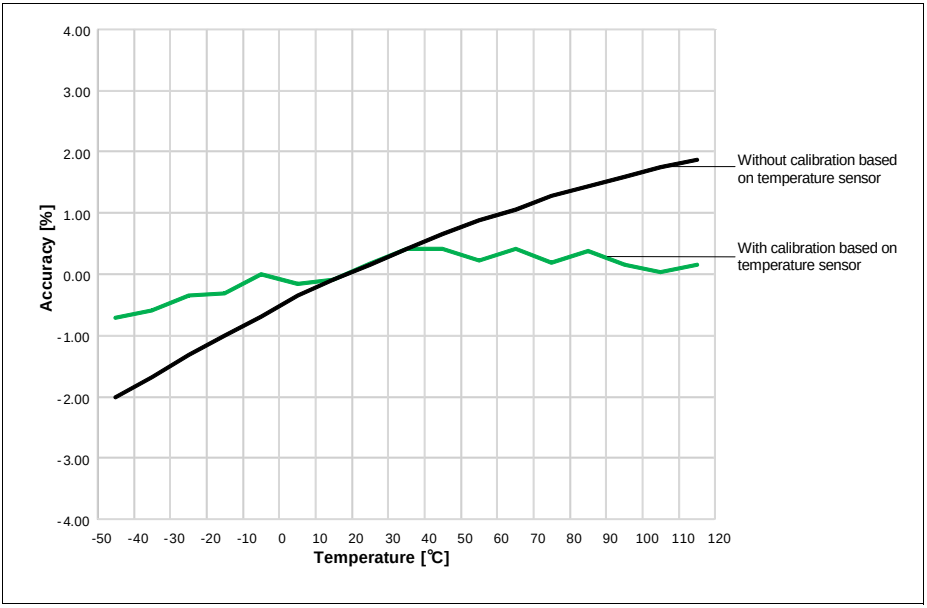


Figure 13 Typical DCO1 accuracy over temperature

Table 20 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1100.

Table 20 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	32.5	32.75	33	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)[2]
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[2]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

3.3.6 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 22 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

Table 24 USIC SSC Slave Mode Timing (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

3.3.7.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 25 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 26 USIC IIC Fast Mode Timing [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

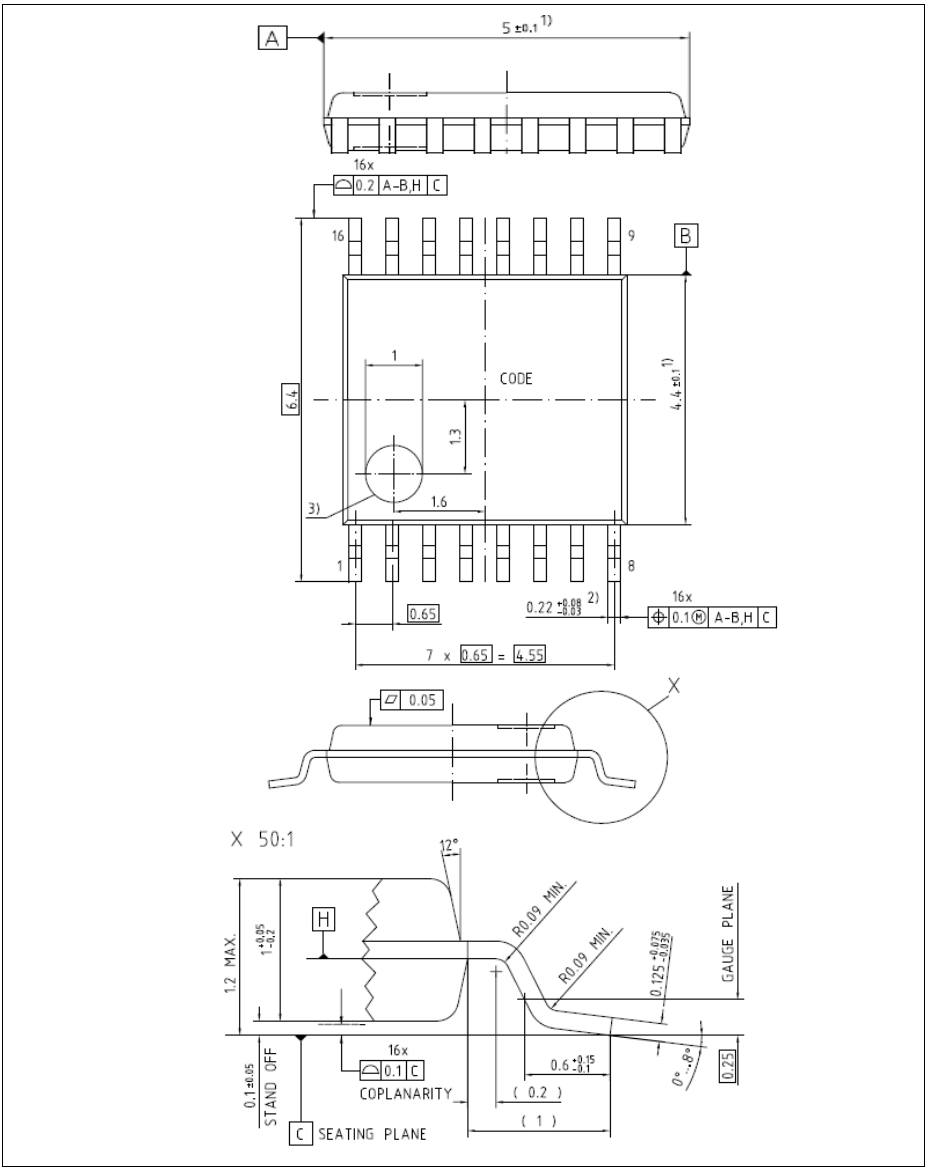


Figure 20 PG-TSSOP-16-8

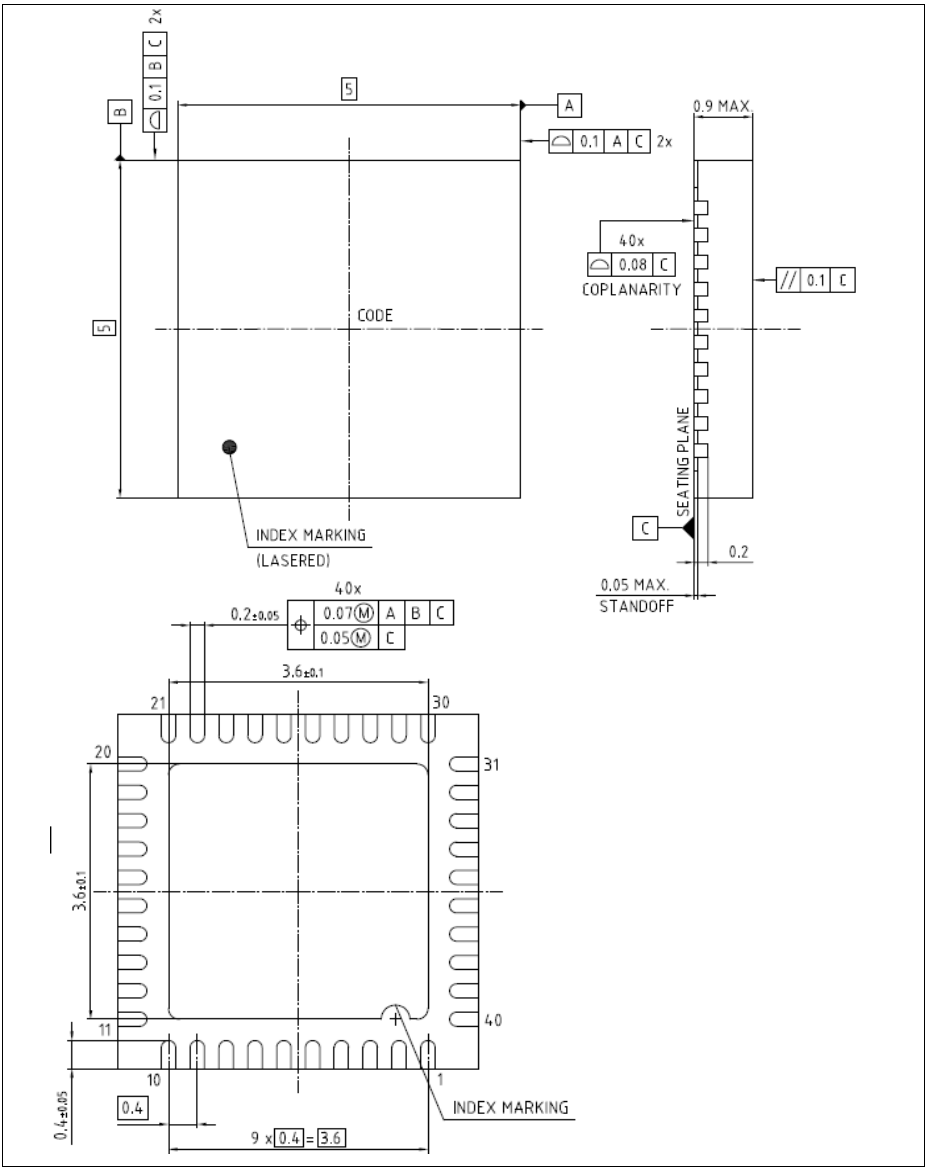


Figure 22 PG-VQFN-40-13

All dimensions in mm.

5 Quality Declaration

Table 30 shows the characteristics of the quality parameters in the XMC1100.

Table 30 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020C