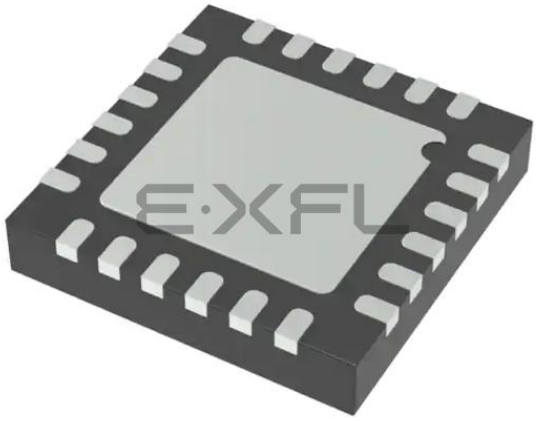
# Infineon Technologies - XMC1100Q024F0064ABXUMA1 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 18 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-VFQFN Exposed Pad |
| Supplier Device Package | PG-VQFN-24-19 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100q024f0064abxuma1 |

# XMC1100

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex™-M0
32-bit processor core

## Data Sheet

V1.4 2014-05

Microcontrollers

# Table of Contents

  - High code density with 32-bit performance
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support
  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests

**On-Chip Memories**

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 64 kbytes on-chip Flash program and data memory

**On-Chip Peripherals**

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- A/D Converters, up to 12 channels, includes a 12-bit analog to digital converter
- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times
- Temperature Sensor (TSE)

**Input/Output Lines**

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

**On-Chip Debug Support**

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

## 1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set

- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1100 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1100 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1100** is used for all derivatives throughout this document.

## 1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

**Table 1 Synopsis of XMC1100 Device Types**

| Derivative | Package | Flash Kbytes | SRAM Kbytes |
|---|---|---|---|
| XMC1100-T016F0008 | PG-TSSOP-16-8 | 8 | 16 |
| XMC1100-T016F0016 | PG-TSSOP-16-8 | 16 | 16 |
| XMC1100-T016F0032 | PG-TSSOP-16-8 | 32 | 16 |
| XMC1100-T016F0064 | PG-TSSOP-16-8 | 64 | 16 |
| XMC1100-T016X0064 | PG-TSSOP-16-8 | 64 | 16 |
| XMC1100-T038F0016 | PG-TSSOP-38-9 | 16 | 16 |
| XMC1100-T038F0032 | PG-TSSOP-38-9 | 32 | 16 |
| XMC1100-T038F0064 | PG-TSSOP-38-9 | 64 | 16 |
| XMC1100-T038X0064 | PG-TSSOP-38-9 | 64 | 16 |
| XMC1100-Q024F0008 | PG-VQFN-24-19 | 8 | 16 |
| XMC1100-Q024F0016 | PG-VQFN-24-19 | 16 | 16 |
| XMC1100-Q024F0032 | PG-VQFN-24-19 | 32 | 16 |
| XMC1100-Q024F0064 | PG-VQFN-24-19 | 64 | 16 |
| XMC1100-Q040F0016 | PG-VQFN-40-13 | 16 | 16 |

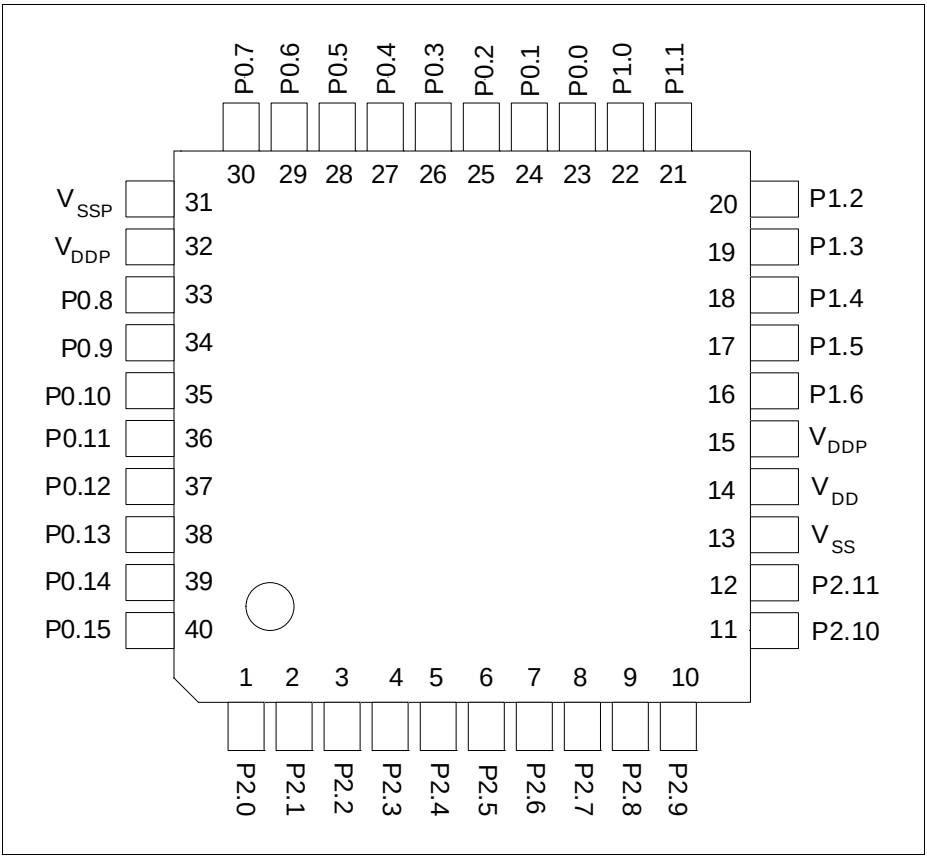


**Figure 7** XMC1100 **PG-VQFN-40 Pin Configuration** (top view)

## Table 8 Port I/O Functions

| Function | Outputs | | | | | | | | | Inputs | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | HWO0 | HWO1 | HWI0 | HWI1 | Input | Input | Input | Input | Input | Input | Input |
| P0.0 | ERU0.PDOUT0 | | ERU0.GOUT0 | CCU40.OUT0 | | USIC0_CH0.SELO0 | USIC0_CH1.SELO0 | | | | | CCU40.IN0C | | | | USIC0_CH0.DX2A | USIC0_CH1.DX2A | |
| P0.1 | ERU0.PDOUT1 | | ERU0.GOUT1 | CCU40.OUT1 | | | SCU.VDROP | | | | | CCU40.IN1C | | | | | | |
| P0.2 | ERU0.PDOUT2 | | ERU0.GOUT2 | CCU40.OUT2 | | VADC0.EMUX02 | | | | | | CCU40.IN2C | | | | | | |
| P0.3 | ERU0.PDOUT3 | | ERU0.GOUT3 | CCU40.OUT3 | | VADC0.EMUX01 | | | | | | CCU40.IN3C | | | | | | |
| P0.4 | | | | CCU40.OUT1 | | VADC0.EMUX00 | WWDT.SERVICE_OUT | | | | | | | | | | | |
| P0.5 | | | | CCU40.OUT0 | | | | | | | | | | | | | | |
| P0.6 | | | | CCU40.OUT0 | | USIC0_CH1.MCLKOUT | USIC0_CH1.DOUT0 | | | | | CCU40.IN0B | | | | USIC0_CH1.DX0C | | |
| P0.7 | | | | CCU40.OUT1 | | USIC0_CH0.SCLKOUT | USIC0_CH1.DOUT0 | | | | | CCU40.IN1B | | | | USIC0_CH0.DX1C | USIC0_CH1.DX0D | USIC0_CH1.DX1C |
| P0.8 | | | | CCU40.OUT2 | | USIC0_CH0.SCLKOUT | USIC0_CH1.SCLKOUT | | | | | CCU40.IN2B | | | | USIC0_CH0.DX1B | USIC0_CH1.DX1B | |
| P0.9 | | | | CCU40.OUT3 | | USIC0_CH0.SELO0 | USIC0_CH1.SELO0 | | | | | CCU40.IN3B | | | | USIC0_CH0.DX2B | USIC0_CH1.DX2B | |
| P0.10 | | | | | | USIC0_CH0.SELO1 | USIC0_CH1.SELO1 | | | | | | | | | USIC0_CH0.DX2C | USIC0_CH1.DX2C | |
| P0.11 | | | | USIC0_CH0.MCLKOUT | | USIC0_CH0.SELO2 | USIC0_CH1.SELO2 | | | | | | | | | USIC0_CH0.DX2D | USIC0_CH1.DX2D | |
| P0.12 | | | | | | USIC0_CH0.SELO3 | | | | | | CCU40.IN0A | CCU40.IN1A | CCU40.IN2A | CCU40.IN3A | USIC0_CH0.DX2E | | |
| P0.13 | WWDT.SERVICE_OUT | | | | | USIC0_CH0.SELO4 | | | | | | | | | | USIC0_CH0.DX2F | | |
| P0.14 | | | | | | USIC0_CH0.DOUT0 | USIC0_CH0.SCLKOUT | | | | | | | | | USIC0_CH0.DX0A | USIC0_CH0.DX1A | |
| P0.15 | | | | | | USIC0_CH0.DOUT0 | USIC0_CH1.MCLKOUT | | | | | | | | | USIC0_CH0.DX0B | | |
| P1.0 | | CCU40.OUT0 | | | | | USIC0_CH0.DOUT0 | | USIC0_CH0.DOUT0 | | USIC0_CH0.HWIN0 | | | | | USIC0_CH0.DX0C | | |
| P1.1 | VADC0.EMUX00 | CCU40.OUT1 | | | | USIC0_CH0.DOUT0 | USIC0_CH1.SELO0 | | USIC0_CH0.DOUT1 | | USIC0_CH0.HWIN1 | | | | | USIC0_CH0.DX0D | USIC0_CH0.DX1D | USIC0_CH1.DX2E |
| P1.2 | VADC0.EMUX01 | CCU40.OUT2 | | | | | USIC0_CH1.DOUT0 | | USIC0_CH0.DOUT2 | | USIC0_CH0.HWIN2 | | | | | USIC0_CH1.DX0B | | |
| P1.3 | VADC0.EMUX02 | CCU40.OUT3 | | | | USIC0_CH1.SCLKOUT | USIC0_CH1.DOUT0 | | USIC0_CH0.DOUT3 | | USIC0_CH0.HWIN3 | | | | | USIC0_CH1.DX0A | USIC0_CH1.DX1A | |
| P1.4 | VADC0.EMUX10 | USIC0_CH1.SCLKOUT | | | | USIC0_CH0.SELO0 | USIC0_CH1.SELO1 | | | | | | | | | USIC0_CH0.DX5E | USIC0_CH1.DX5E | |
| P1.5 | VADC0.EMUX11 | USIC0_CH0.DOUT0 | | | | USIC0_CH0.SELO1 | USIC0_CH1.SELO2 | | | | | | | | | USIC0_CH1.DX5F | | |

## Table 8 Port I/O Functions (cont'd)

| Function | Outputs | | | | | | | | | Inputs | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | HWO0 | HWO1 | HWI0 | HWI1 | Input | Input | Input | Input | Input | Input | Input |
| P1.6 | VADC0.EMUX12 | USIC0_CH1.DOUT0 | | USIC0_CH0.SCLKOUT | | USIC0_CH0.SELO2 | USIC0_CH1.SELO3 | | | | | | | USIC0_CH0.DX5F | | | | |
| P2.0 | ERU0.PDOUT3 | CCU40.OUT0 | ERU0.GOUT3 | | | USIC0_CH0.DOUT0 | USIC0_CH0.SCLKOUT | | | | | | VADC0.G0CH5 | | ERU0.0B0 | USIC0_CH0.DX0E | USIC0_CH0.DX1E | USIC0_CH1.DX2F |
| P2.1 | ERU0.PDOUT2 | CCU40.OUT1 | ERU0.GOUT2 | | | USIC0_CH0.DOUT0 | USIC0_CH1.SCLKOUT | | | | | | VADC0.G0CH6 | | ERU0.1B0 | USIC0_CH0.DX0F | USIC0_CH1.DX3A | USIC0_CH1.DX4A |
| P2.2 | | | | | | | | | | | | | VADC0.G0CH7 | | ERU0.0B1 | USIC0_CH0.DX3A | USIC0_CH0.DX4A | USIC0_CH1.DX5A |
| P2.3 | | | | | | | | | | | | | VADC0.G1CH5 | | ERU0.1B1 | USIC0_CH0.DX5B | USIC0_CH1.DX3C | USIC0_CH1.DX4C |
| P2.4 | | | | | | | | | | | | | VADC0.G1CH6 | | ERU0.0A1 | USIC0_CH0.DX3B | USIC0_CH0.DX4B | USIC0_CH1.DX5B |
| P2.5 | | | | | | | | | | | | | VADC0.G1CH7 | | ERU0.1A1 | USIC0_CH0.DX5D | USIC0_CH1.DX3E | USIC0_CH1.DX4E |
| P2.6 | | | | | | | | | | | | | VADC0.G0CH0 | | ERU0.2A1 | USIC0_CH0.DX3E | USIC0_CH0.DX4E | USIC0_CH1.DX5D |
| P2.7 | | | | | | | | | | | | | VADC0.G1CH1 | | ERU0.3A1 | USIC0_CH0.DX5C | USIC0_CH1.DX3D | USIC0_CH1.DX4D |
| P2.8 | | | | | | | | | | | | | VADC0.G0CH1 | VADC0.G1CH0 | ERU0.3B1 | USIC0_CH0.DX3D | USIC0_CH0.DX4D | USIC0_CH1.DX5C |
| P2.9 | | | | | | | | | | | | | VADC0.G0CH2 | VADC0.G1CH4 | ERU0.3B0 | USIC0_CH0.DX5A | USIC0_CH1.DX3B | USIC0_CH1.DX4B |
| P2.10 | ERU0.PDOUT1 | CCU40.OUT2 | ERU0.GOUT1 | | | | USIC0_CH1.DOUT0 | | | | | | VADC0.G0CH3 | VADC0.G1CH2 | ERU0.2B0 | USIC0_CH0.DX3C | USIC0_CH0.DX4C | USIC0_CH1.DX0F |
| P2.11 | ERU0.PDOUT0 | CCU40.OUT3 | ERU0.GOUT0 | | | USIC0_CH1.SCLKOUT | USIC0_CH1.DOUT0 | | | | | | VADC0.G0CH4 | VADC0.G1CH3 | ERU0.2B1 | USIC0_CH1.DX0E | USIC0_CH1.DX1E | |

# 3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1100.

## 3.1 General Parameters

### 3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1100 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1100 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1100 is designed in.

**Table 11 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Maximum current into $V_{DDP}$ (TSSOP28/16, VQFN24) | $I_{MVDD1}$ | SR | – | 130 | mA | 3) |
| Maximum current into $V_{DDP}$ (TSSOP38, VQFN40) | $I_{MVDD2}$ | SR | – | 260 | mA | 3) |
| Maximum current out of $V_{SS}$ (TSSOP28/16, VQFN24) | $I_{MVSS1}$ | SR | – | 130 | mA | 3) |
| Maximum current out of $V_{SS}$ (TSSOP38, VQFN40) | $I_{MVSS2}$ | SR | – | 260 | mA | 3) |

1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin.

3) Not subject to production test, verified by design/characterization.

4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when $V_{DDP}$ is powered off.

**Table 12 ADC Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum sample rate in 8-bit mode [3] | $f_{C8}$ CC | – | – | $f_{ADC}$ / 38.5 | – | 1 sample pending |
| | | – | – | $f_{ADC}$ / 54.5 | – | 2 samples pending |
| DNL error | $EA_{DNL}$ CC | – | ±2.0 | – | LSB 12 | |
| INL error | $EA_{INL}$ CC | – | ±4.0 | – | LSB 12 | |
| Gain error with external reference | $EA_{GAIN}$ CC | – | ±0.5 | – | % | SHSCFG.AREF = $00_B$ (calibrated) |
| Gain error with internal reference | $EA_{GAIN}$ CC | – | ±3.6 | – | % | SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 105°C |
| | | – | ±2.0 | – | % | SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C |
| Offset error | $EA_{OFF}$ CC | – | ±6.0 | – | LSB 12 | Calibrated |

1) Not subject to production test, verified by design/characterization.

2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

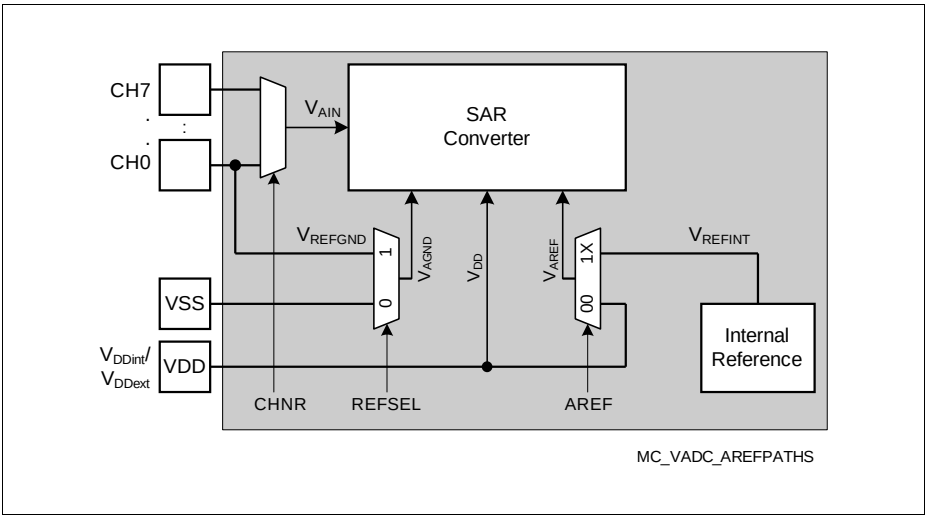


**Figure 8 ADC Voltage Supply**

### 3.2.4 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

**Table 14 Power Supply Parameters[1)]**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[2)] | Max. | | |
| Active mode current[3)] | $I_{DDPA}$ CC | – | 8.4 | 11.0 | mA | $f_{MCLK}$ = 32 MHz<br>$f_{PCLK}$ = 64 MHz |
| | | – | 3.7 | – | mA | $f_{MCLK}$ = 1 MHz<br>$f_{PCLK}$ = 1 MHz |
| Sleep mode current Peripherals clock enabled[4)] | $I_{DDPSE}$ CC | – | 5.9 | – | mA | $f_{MCLK}$ = 32 MHz<br>$f_{PCLK}$ = 64 MHz |
| Sleep mode current Peripherals clock disabled[5)] | $I_{DDPSD}$ CC | – | 1.2 | – | mA | $f_{MCLK}$ = 1 MHz<br>$f_{PCLK}$ = 1 MHz |
| Deep Sleep mode current[6)] | $I_{DDPDS}$ CC | – | 0.24 | – | mA | |
| Wake-up time from Sleep to Active mode[7)] | $t_{SSA}$ CC | – | 6 | – | cycles | |
| Wake-up time from Deep Sleep to Active mode[8)] | $t_{DSA}$ CC | – | 280 | – | µsec | |

1) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
2) The typical values are measured at $T_A$ = + 25 °C and $V_{DDP}$ = 5 V.
3) CPU and all peripherals clock enabled, Flash is in active mode.
4) CPU is sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU is sleep, Flash is powered down and code executed from RAM after wake-up.
6) CPU is sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
7) CPU is sleep, Flash is in active mode during sleep mode.
8) CPU is sleep, Flash is in power down mode during deep sleep mode.

## 3.3 AC Parameters

### 3.3.1 Testing Waveforms

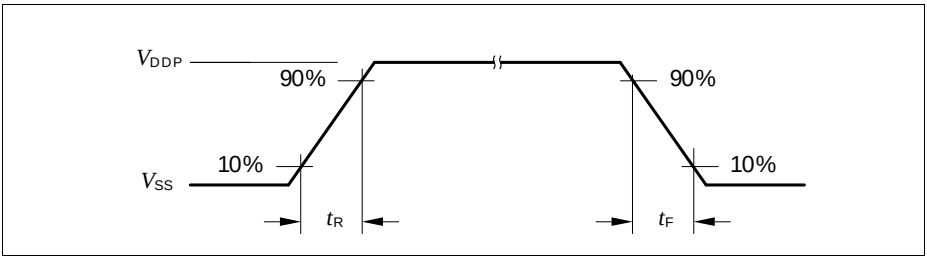


**Figure 9 Rise/Fall Time Parameters**

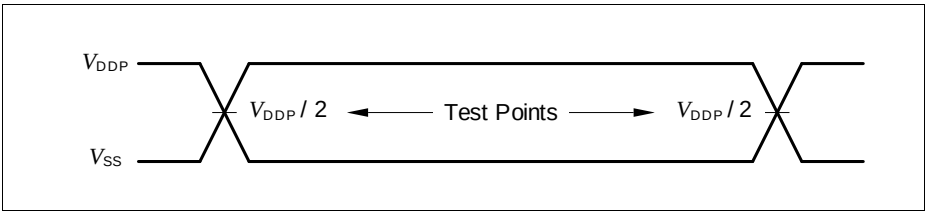


**Figure 10 Testing Waveform, Output Delay**

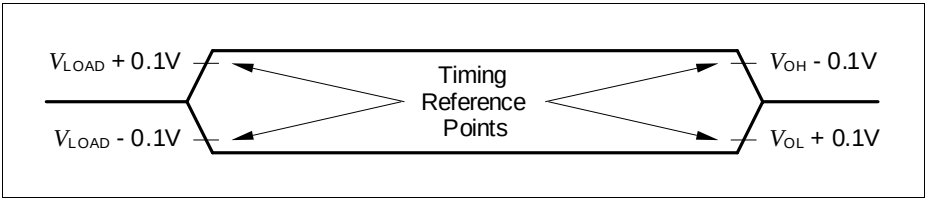


**Figure 11 Testing Waveform, Output High Impedance**

### 3.3.3 Power-Up and Supply Threshold Charcteristics

Table 18 provides the characteristics of the supply threshold in XMC1100.

**Table 18 Power-Up and Supply Threshold Parameters (Operating Conditions apply) [1]**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DDP}$ ramp-up time | $t_{RAMPUP}$ SR | $V_{DDP}$/ $S_{VDDPrise}$ | – | $10^7$ | µs | |
| $V_{DDP}$ slew rate | $S_{VDDPOP}$ SR | 0 | – | 0.1 | V/µs | Slope during normal operation |
| | $S_{VDDP10}$ SR | 0 | – | 10 | V/µs | Slope during fast transient within +/- 10% of $V_{DDP}$ |
| | $S_{VDDPrise}$ SR | 0 | – | 10 | V/µs | Slope during power-on or restart after brownout event |
| | $S_{VDDPfall}$ [2] SR | 0 | – | 0.25 | V/µs | Slope during supply falling out of the +/-10% limits[3] |
| $V_{DDP}$ prewarning voltage | $V_{DDPPW}$ CC | 2.1 | 2.25 | 2.4 | V | ANAVDEL.VDEL_ SELECT = $00_B$ |
| | | 2.85 | 3 | 3.15 | V | ANAVDEL.VDEL_ SELECT = $01_B$ |
| | | 4.2 | 4.4 | 4.6 | V | ANAVDEL.VDEL_ SELECT = $10_B$ |
| $V_{DDP}$ brownout reset voltage | $V_{DDPBO}$ CC | 1.55 | 1.62 | 1.75 | V | calibrated, before user code starts running |
| Start-up time from power-on reset | $t_{SSW}$ SR | – | 320 | – | µs | Time to the first user code instruction[4] |

1) Not all parameters are 100% tested, but are verified by design/characterisation.

2) A capacitor of at least 100 nF has to be added between $V_{DDP}$ and $V_{SSP}$ to fulfill the requirement as stated for this parameter.

### 3.3.4 On-Chip Oscillator Characteristics

**Table 19** provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1100.

**Table 19 64 MHz DCO1 Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | 63.5 | 64 | 64.5 | MHz | under nominal conditions[1] after trimming |
| Accuracy | $\Delta f_{LT}$ | CC | -1.7 | – | 3.4 | % | with respect to $f_{NOM}$(typ), over temperature (0 °C to 85 °C)[2] |
| | | | -3.9 | – | 4.0 | % | with respect to $f_{NOM}$(typ), over temperature (-40 °C to 105 °C)[2] |
| Accuracy with calibration based on temperature sensor | $\Delta f_{LTT}$ | CC | -1.3 | – | 1.25 | % | with respect to $f_{NOM}$(typ), over temperature ($T_A$ = 0 °C to 105 °C)[2] |
| | | | -2.6 | – | 1.25 | % | with respect to $f_{NOM}$(typ), over temperature ($T_A$ = -40 °C to 105 °C)[2] |

1) The deviation is relative to the factory trimmed frequency at nominal $V_{DDC}$ and $T_A$ = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

### 3.3.6 SPD Timing Requirements

The optimum SPD decision time between $0_B$ and $1_B$ is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

**Table 22 Optimum Number of Sample Clocks for SPD**

| Sample Freq. | Sampling Factor | Sample Clocks $0_B$ | Sample Clocks $1_B$ | Effective Decision Time[1)] | Remark |
|---|---|---|---|---|---|
| 8 MHz | 4 | 1 to 5 | 6 to 12 | 0.69 µs | The other closest option (0.81 µs) for the effective decision time is less robust. |

1) Nominal sample frequency period multiplied with 0.5 + (max. number of $0_B$ sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

### 3.3.7 Peripheral Timings

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

#### 3.3.7.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

*Note: Operating Conditions apply.*

**Table 23 USIC SSC Master Mode Timing**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Slave select output SELO active to first SCLKOUT transmit edge | $t_1$ | CC | 80 | – | – | ns | |
| Slave select output SELO inactive after last SCLKOUT receive edge | $t_2$ | CC | 0 | – | – | ns | |
| Data output DOUT[3:0] valid time | $t_3$ | CC | -10 | – | 10 | ns | |
| Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge | $t_4$ | SR | 80 | – | – | ns | |
| Data input DX0/DX[5:3] hold time from SCLKOUT receive edge | $t_5$ | SR | 0 | – | – | ns | |

**Table 24 USIC SSC Slave Mode Timing**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Select input DX2 setup to first clock input DX1 transmit edge[1)] | $t_{10}$ | SR | 10 | – | – | ns | |
| Select input DX2 hold after last clock input DX1 receive edge[1)] | $t_{11}$ | SR | 10 | – | – | ns | |

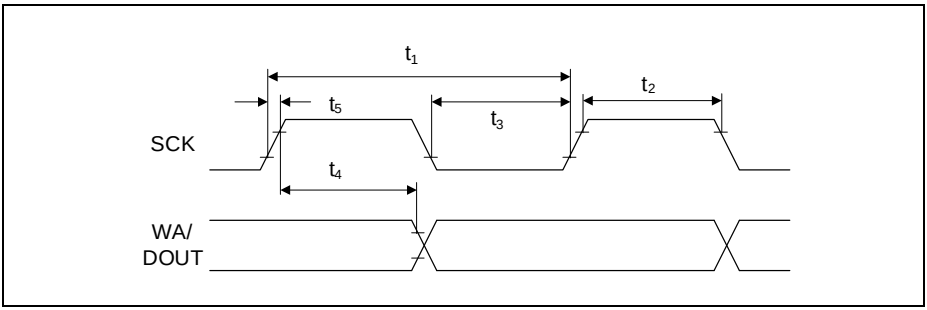


**Figure 17 USIC IIS Master Transmitter Timing**

**Table 28 USIC IIS Slave Receiver Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_6$ SR | $4/f_{MCLK}$ | - | - | ns | |
| Clock HIGH | $t_7$ SR | 0.35 x $t_{6min}$ | - | - | ns | |
| Clock Low | $t_8$ SR | 0.35 x $t_{6min}$ | - | - | ns | |
| Set-up time | $t_9$ SR | 0.2 x $t_{6min}$ | - | - | ns | |
| Hold time | $t_{10}$ SR | 10 | - | - | ns | |

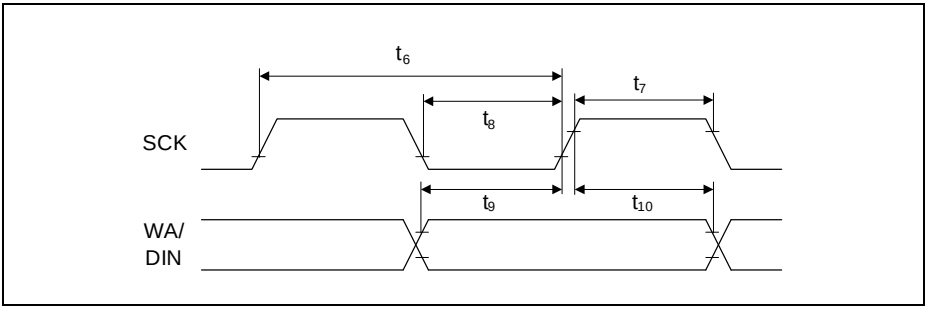


**Figure 18 USIC IIS Slave Receiver Timing**

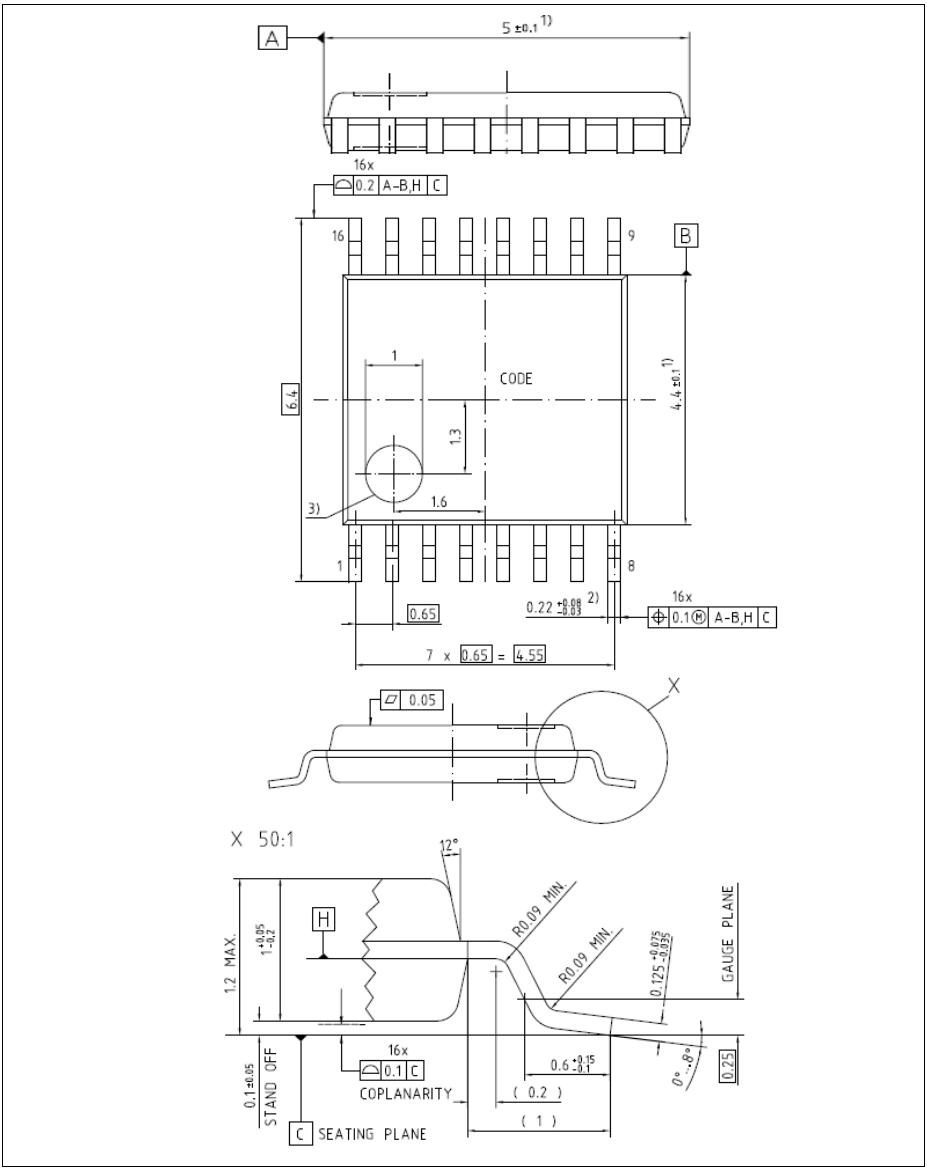


**Figure 20 PG-TSSOP-16-8**

# 5 Quality Declaration

**Table 30** shows the characteristics of the quality parameters in the XMC1100.

**Table 30 Quality Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ SR | - | 2000 | V | Conforming to EIA/JESD22-A114-B |
| ESD susceptibility according to Charged Device Model (CDM) pins | $V_{CDM}$ SR | - | 500 | V | Conforming to JESD22-C101-C |
| Moisture sensitivity level | $MSL$ CC | - | 3 | - | JEDEC J-STD-020C |