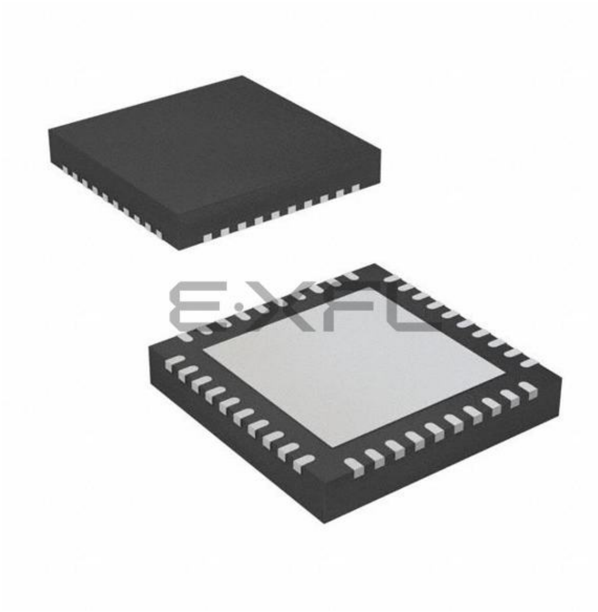
Infineon Technologies - XMC1100Q040F0016ABXUMA1 Datasheet



Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-40-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100q040f0016abxuma1

XMC1100 Data Sheet

Revision History: V1.4 2014-05

Previous Version: V1.3

Page	Subjects
Page 10	ADC channels of Table 2 is updated. Table 3 is added.
Page 10	Description for Chip Identification Number of Section 1.4 is updated.
Page 17	The pad type is corrected for P1.6 in Table 6.
Page 29	The t_{C12} , f_{C12}, t_{C10}, f_{C10}, t_{C8} and f_{C8} parameters are updated in Table 12.
Page 32	Figure 8 is added.
Page 33	The t_{SR} and t_{TSAL} parameters are updated in Table 13.
Page 36	Parameter name for t_{PSER} is updated. The $N_{WSFLASH}$ parameter and test condition for t_{RET} are added to Table 16.
Page 39	The min value for V_{DDPBO} parameter is added to Table 18. Footnote 1 is updated.
Page 41	The Δf_{LTT} parameter is added to Table 19.
Page 47	Figure 13 is added.

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Table of Contents

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1100 series devices.

The document describes the characteristics of a superset of the XMC1100 series devices. For simplicity, the various device types are referred to by the collective term XMC1100 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  - decribes the functionality of the superset of devices.
- **Data Sheets**
  - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

  - High code density with 32-bit performance
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support
  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 64 kbytes on-chip Flash program and data memory

On-Chip Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- A/D Converters, up to 12 channels, includes a 12-bit analog to digital converter
- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times
- Temperature Sensor (TSE)

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set

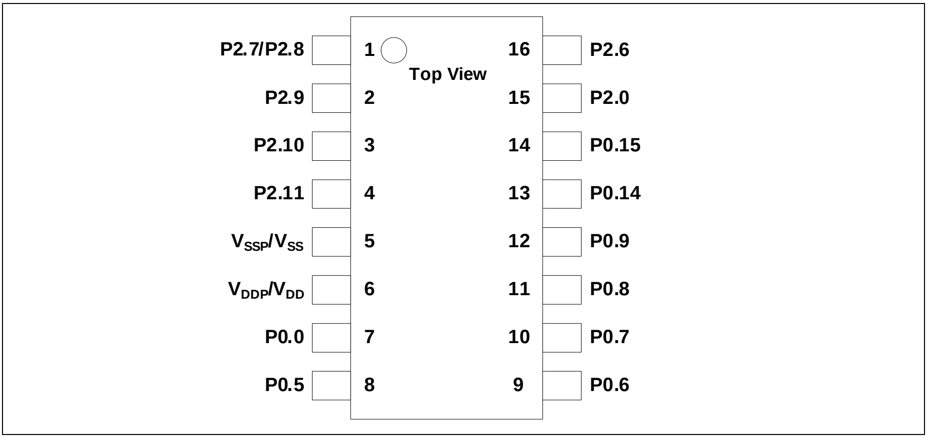

Figure 5 XMC1100 **PG-TSSOP-16 Pin Configuration** (top view)

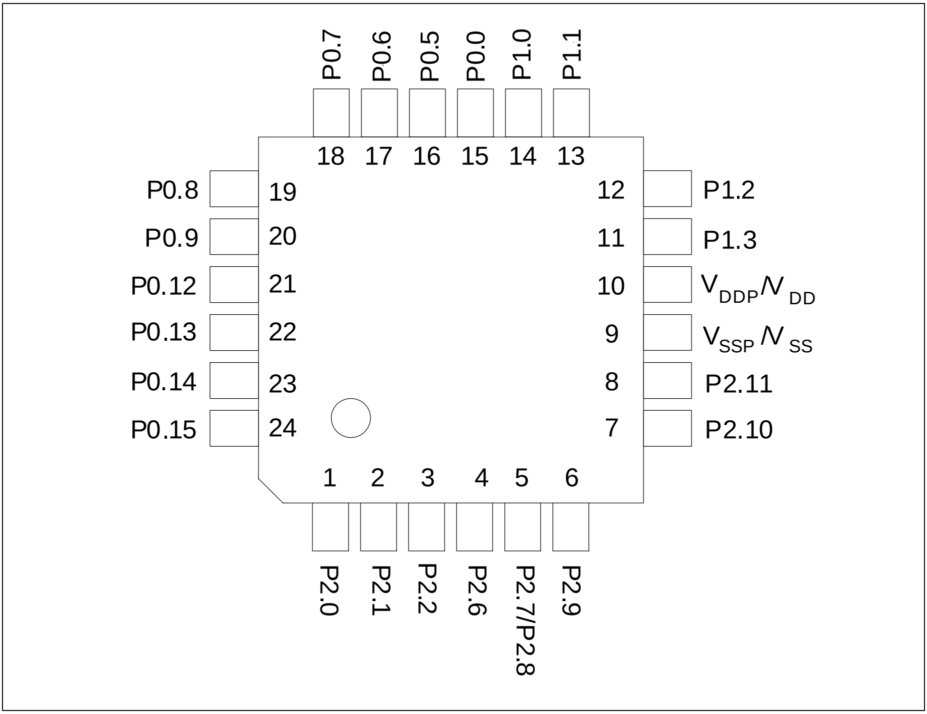

Figure 6 XMC1100 **PG-VQFN-24 Pin Configuration** (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	15	7	STD_INOUT	
P0.1	24	18	-	-	STD_INOUT	
P0.2	25	19	-	-	STD_INOUT	
P0.3	26	20	-	-	STD_INOUT	
P0.4	27	21	-	-	STD_INOUT	
P0.5	28	22	16	8	STD_INOUT	
P0.6	29	23	17	9	STD_INOUT	
P0.7	30	24	18	10	STD_INOUT	
P0.8	33	27	19	11	STD_INOUT	
P0.9	34	28	20	12	STD_INOUT	
P0.10	35	29	-	-	STD_INOUT	
P0.11	36	30	-	-	STD_INOUT	
P0.12	37	31	21	-	STD_INOUT	

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
VDDP	15	10	10	6	Power	I/O port supply
VSSP	31	25	-	-	Power	I/O port ground
VDDP	32	26	-	-	Power	I/O port supply
VSSP	Exp. Pad	-	Exp. Pad	-	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

3.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1100. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 10 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage[1]	V_{DDP} SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK} CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK} CC	–	–	66.4	MHz	Peripherals clock

[1] See also the Supply Monitoring thresholds, **Chapter 3.3.3**.

Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	0.85 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)[3]
Input Hysteresis[1]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), Standard Hysteresis
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			0.5 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(5 V), Large Hysteresis
			0.4 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(3.3 V), Large Hysteresis
			0.2 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode(2.2 V), Large Hysteresis
Pull-up resistor on port pins	R_{PUP}	CC	20	50	kohm	$V_{\mathrm{IN}} = V_{\mathrm{SSP}}$
Pull-down resistor on port pins	R_{PDP}	CC	20	50	kohm	$V_{\mathrm{IN}} = V_{\mathrm{DDP}}$
Input leakage current[2]	I_{OZP}	CC	-1	1	µA	$0 < V_{\mathrm{IN}} < V_{\mathrm{DDP}}$, $T_{\mathrm{A}} \leq 105$ °C
Overload current on any pin	I_{OVP}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{\mathrm{OV}}\|$	SR	–	25	mA	[3]
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[4]
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	–
Maximum current per high currrent pins	I_{MP1A}	SR	-10	50	mA	–

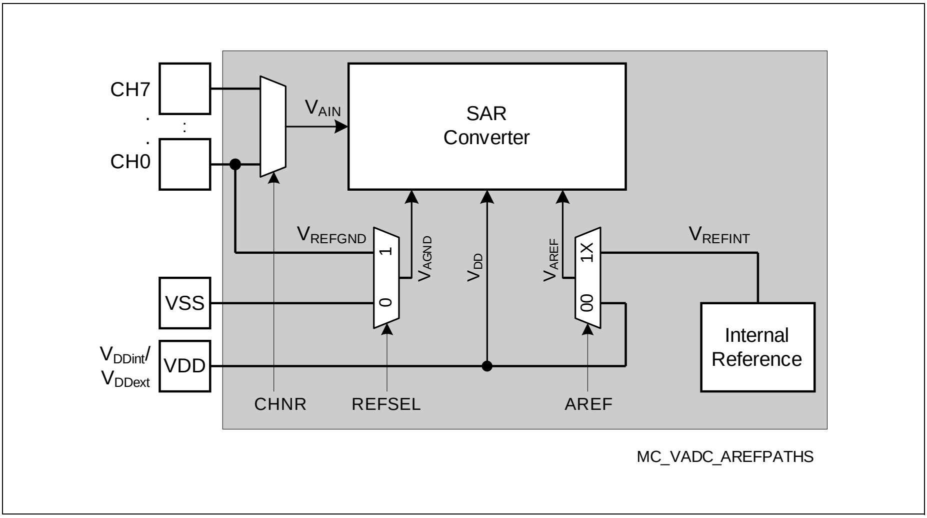

Figure 8 ADC Voltage Supply

3.3 AC Parameters

3.3.1 Testing Waveforms

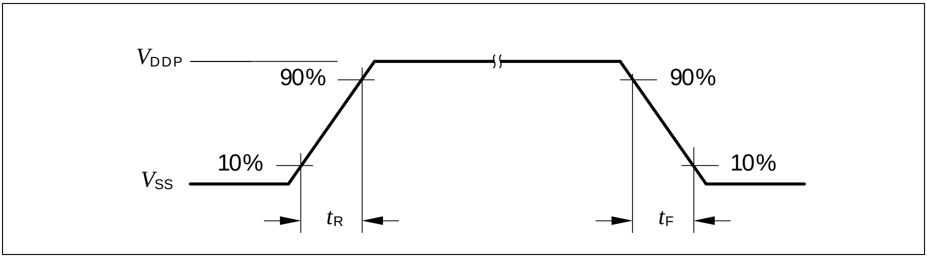

Figure 9 Rise/Fall Time Parameters

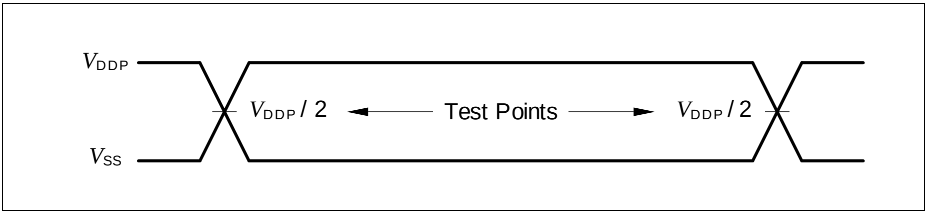

Figure 10 Testing Waveform, Output Delay

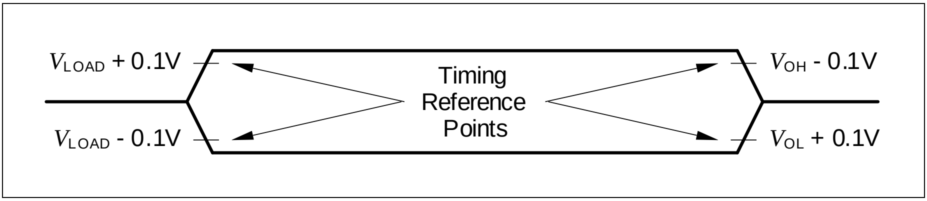

Figure 11 Testing Waveform, Output High Impedance

3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

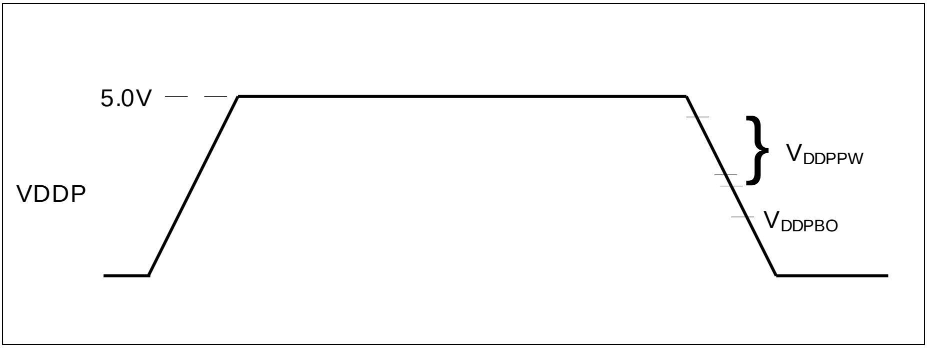

Figure 12 **Supply Threshold Parameters**

3.3.6 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 22 Optimum Number of Sample Clocks for SPD

Sample Freq.	**Sampling Factor**	**Sample Clocks 0_B**	**Sample Clocks 1_B**	**Effective Decision Time**[1]	**Remark**
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

[1] Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

3.3.7 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.7.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 23 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	0	–	–	ns	

Table 24 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10}	SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11}	SR	10	–	–	ns	

Table 26 USIC IIC Fast Mode Timing [1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

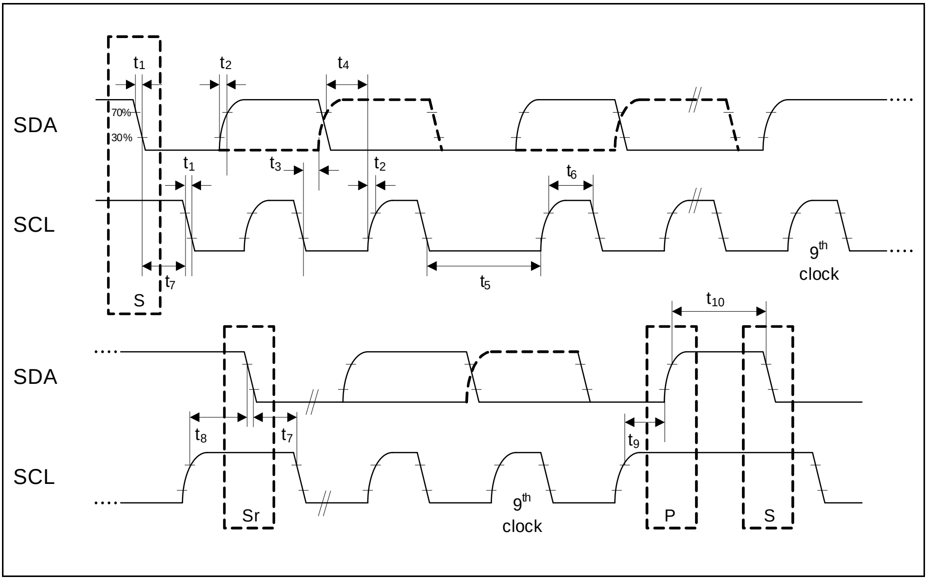

Figure 16 USIC IIC Stand and Fast Mode Timing

3.3.7.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 27 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	2/f_{MCLK}	-	-	ns	$V_{\text{DDP}} \geq 3$ V
		4/f_{MCLK}	-	-	ns	$V_{\text{DDP}} < 3$ V
Clock HIGH	t_2 CC	0.35 x $t_{1\text{min}}$	-	-	ns	
Clock Low	t_3 CC	0.35 x $t_{1\text{min}}$	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	0.15 x $t_{1\text{min}}$	ns	

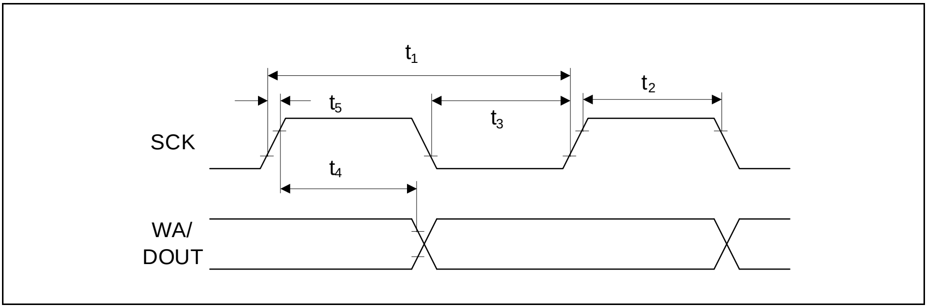

Figure 17 USIC IIS Master Transmitter Timing

Table 28 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	-	-	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	-	-	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

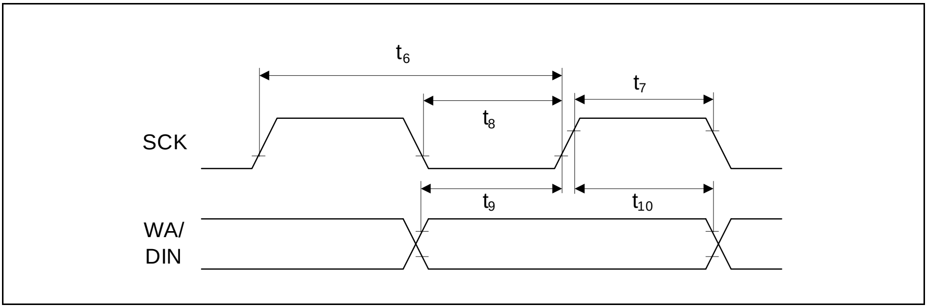

Figure 18 USIC IIS Slave Receiver Timing

4 Package and Reliability

The XMC1100 is a member of the XMC1000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 29 provides the thermal characteristics of the packages used in XMC1100.

Table 29 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8[1)
		-	70.3	K/W	PG-TSSOP-38-9[1)
		-	46.0	K/W	PG-VQFN-24-19[1)
		-	38.4	K/W	PG-VQFN-40-13[1)

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1100 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$" quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

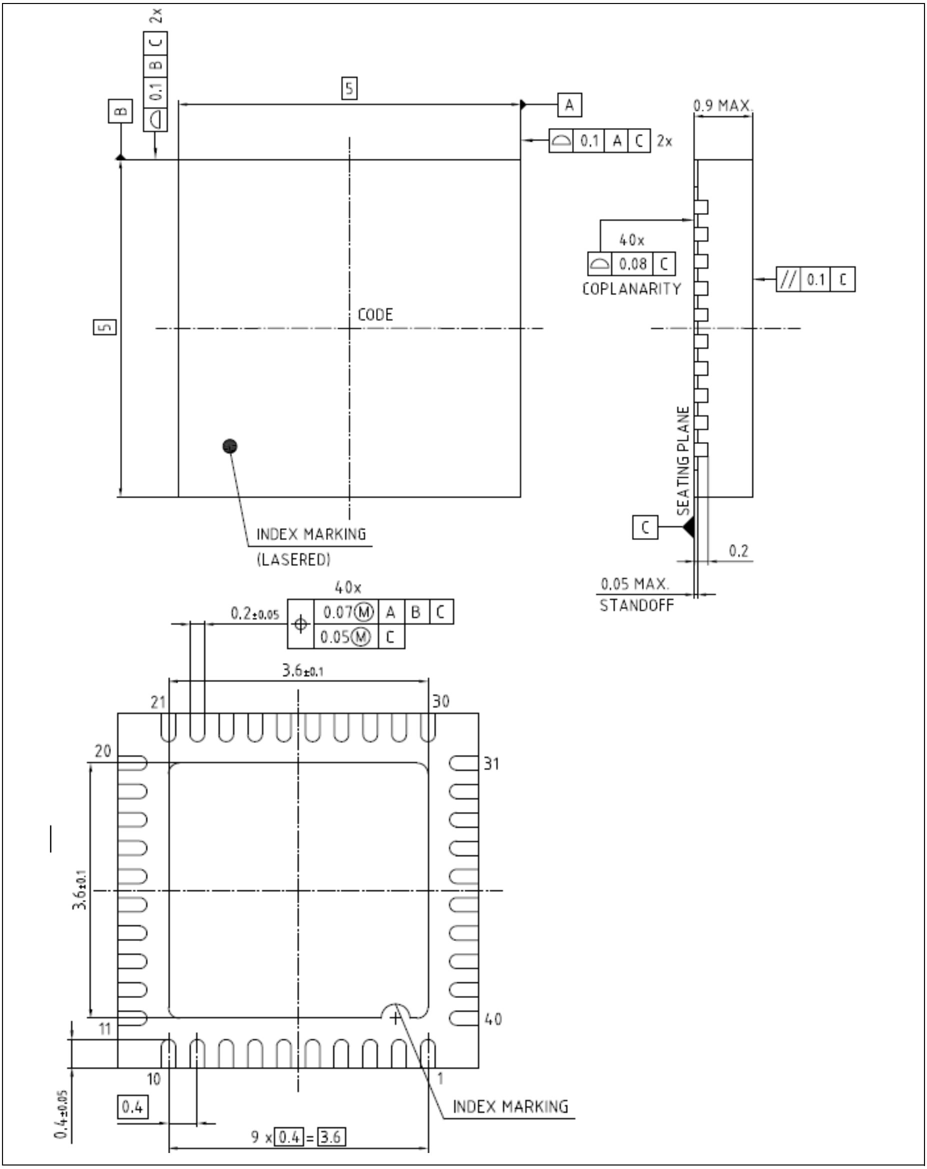

Figure 22 PG-VQFN-40-13

All dimensions in mm.

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