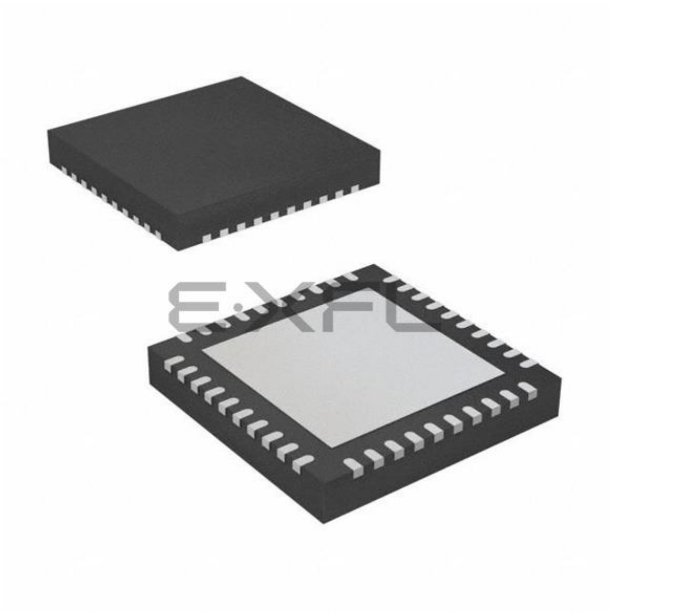

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-40-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100q040f0064abxuma1

XMC1100 Data Sheet

Revision History: V1.4 2014-05

Previous Version: V1.3	
Page	Subjects
Page 10	ADC channels of Table 2 is updated. Table 3 is added.
Page 10	Description for Chip Identification Number of Section 1.4 is updated.
Page 17	The pad type is corrected for P1.6 in Table 6.
Page 29	The t_{C12} , f_{C12}, t_{C10}, f_{C10}, t_{C8} and f_{C8} parameters are updated in Table 12.
Page 32	Figure 8 is added.
Page 33	The t_{SR} and t_{TSAL} parameters are updated in Table 13.
Page 36	Parameter name for t_{PSER} is updated. The $N_{WSFLASH}$ parameter and test condition for t_{RET} are added to Table 16.
Page 39	The min value for V_{DDPBO} parameter is added to Table 18. Footnote 1 is updated.
Page 41	The Δf_{LTT} parameter is added to Table 19.
Page 47	Figure 13 is added.

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Table of Contents

- <Z> the package variant
  – T: TSSOP
  – Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  – F: -40°C to 85°C
  – X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1100 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1100 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1100** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XMC1100 Device Types

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1100-T016F0008	PG-TSSOP-16-8	8	16
XMC1100-T016F0016	PG-TSSOP-16-8	16	16
XMC1100-T016F0032	PG-TSSOP-16-8	32	16
XMC1100-T016F0064	PG-TSSOP-16-8	64	16
XMC1100-T016X0064	PG-TSSOP-16-8	64	16
XMC1100-T038F0016	PG-TSSOP-38-9	16	16
XMC1100-T038F0032	PG-TSSOP-38-9	32	16
XMC1100-T038F0064	PG-TSSOP-38-9	64	16
XMC1100-T038X0064	PG-TSSOP-38-9	64	16
XMC1100-Q024F0008	PG-VQFN-24-19	8	16
XMC1100-Q024F0016	PG-VQFN-24-19	16	16
XMC1100-Q024F0032	PG-VQFN-24-19	32	16
XMC1100-Q024F0064	PG-VQFN-24-19	64	16
XMC1100-Q040F0016	PG-VQFN-40-13	16	16

Table 4 XMC1100 **Chip Identification Number**

Derivative	Value	Marking
XMC1100-T016F0008	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00003000 101ED083$_H$	AA
XMC1100-T016F0016	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1100-T016F0032	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1100-T016F0064	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1100-T016X0064	00011033 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1100-T038F0016	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1100-T038F0032	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1100-T038F0064	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1100-T038X0064	00011013 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1100-Q024F0008	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00003000 101ED083$_H$	AA
XMC1100-Q024F0016	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1100-Q024F0032	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1100-Q024F0064	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1100-Q040F0016	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1100-Q040F0032	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1100-Q040F0064	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083$_H$	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

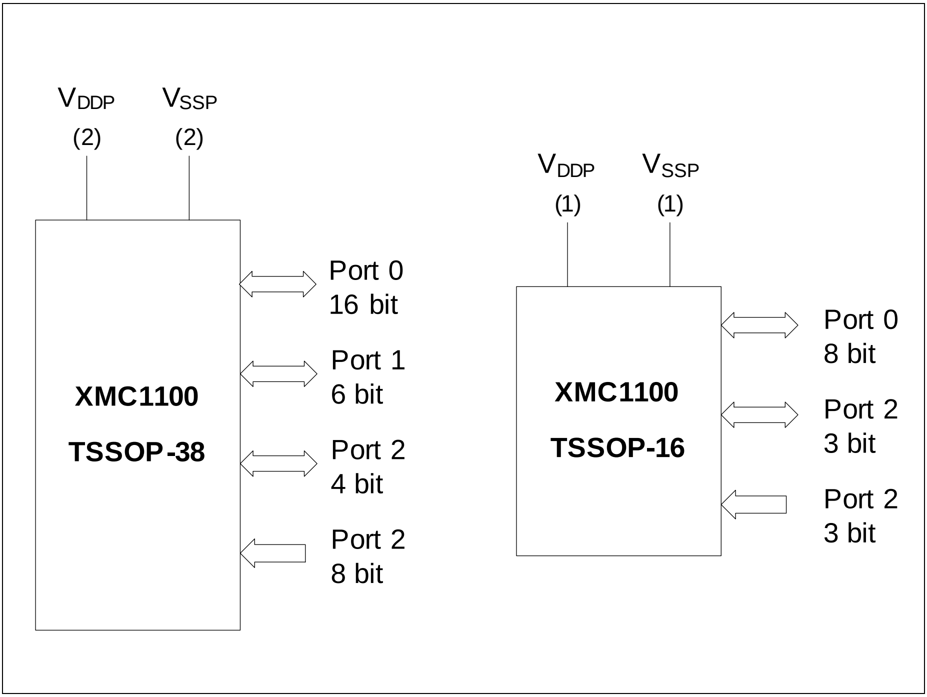

Figure 2 XMC1100 Logic Symbol for TSSOP-38 and TSSOP-16

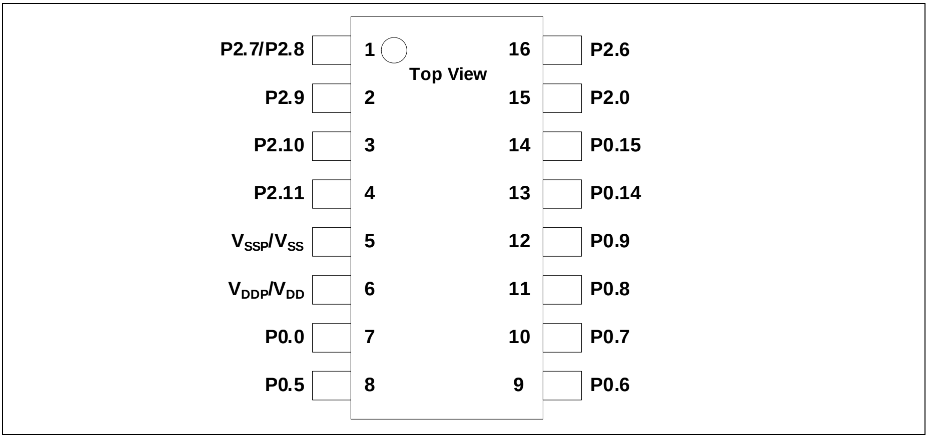

Figure 5 XMC1100 **PG-TSSOP-16 Pin Configuration** (top view)

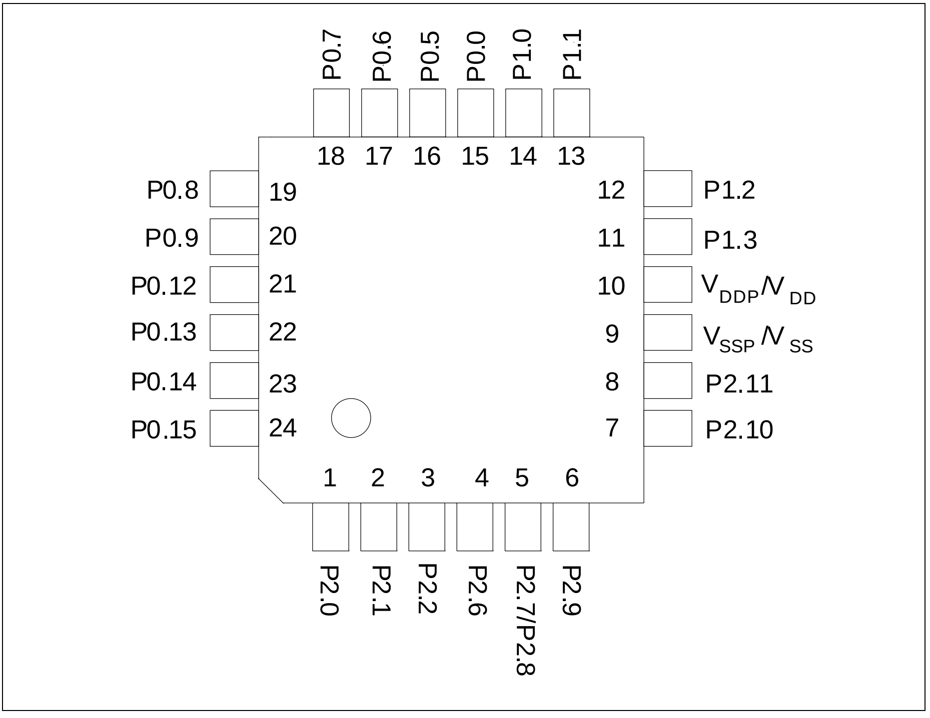

Figure 6 XMC1100 **PG-VQFN-24 Pin Configuration** (top view)

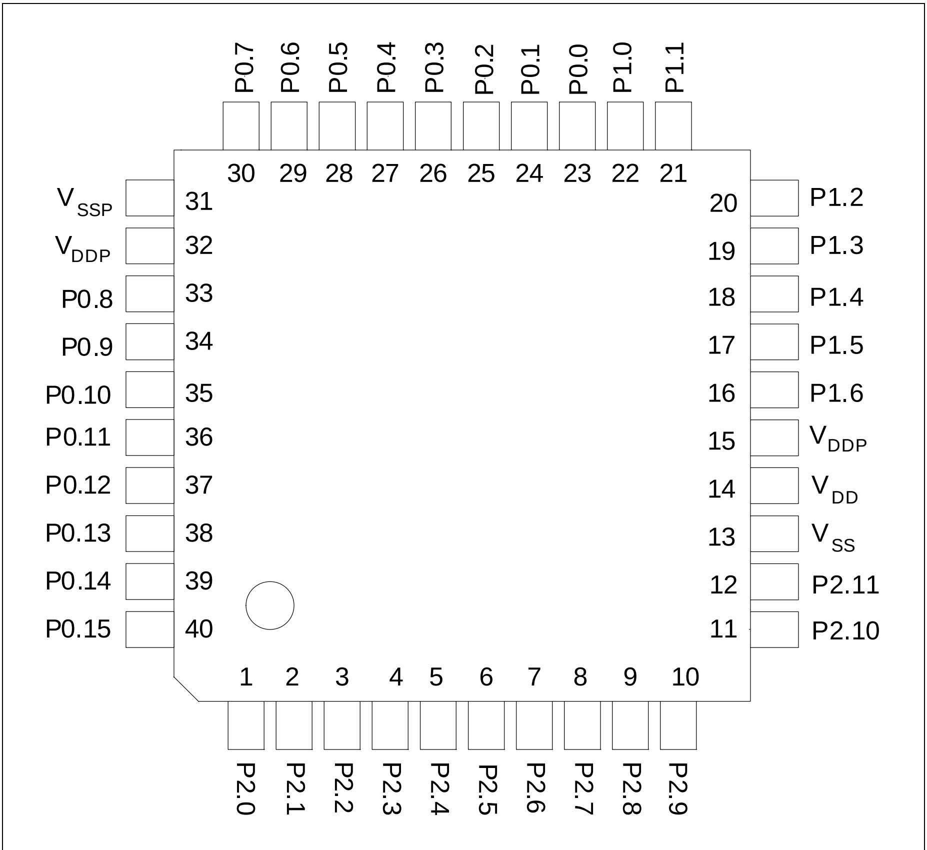

Figure 7 XMC1100 **PG-VQFN-40 Pin Configuration** (top view)

Table 8 Port I/O Functions (cont'd)

Function	Outputs									Inputs								
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input
P1.6	VADC0.EMUX12	USIC0_CH1.DOUT0		USIC0_CH0.SCLKOUT		USIC0_CH0.SELO2	USIC0_CH1.SELO3							USIC0_CH0.DX5F				
P2.0	ERU0.PDOUT3	CCU40.OUT0	ERU0.GOUT3			USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT						VADC0.G0CH5		ERU0.0B0	USIC0_CH0.DX0E	USIC0_CH0.DX1E	USIC0_CH1.DX2F
P2.1	ERU0.PDOUT2	CCU40.OUT1	ERU0.GOUT2			USIC0_CH0.DOUT0	USIC0_CH1.SCLKOUT						VADC0.G0CH6		ERU0.1B0	USIC0_CH0.DX0F	USIC0_CH1.DX3A	USIC0_CH1.DX4A
P2.2													VADC0.G0CH7		ERU0.0B1	USIC0_CH0.DX3A	USIC0_CH0.DX4A	USIC0_CH1.DX5A
P2.3													VADC0.G1CH5		ERU0.1B1	USIC0_CH0.DX5B	USIC0_CH1.DX3C	USIC0_CH1.DX4C
P2.4													VADC0.G1CH6		ERU0.0A1	USIC0_CH0.DX3B	USIC0_CH0.DX4B	USIC0_CH1.DX5B
P2.5													VADC0.G1CH7		ERU0.1A1	USIC0_CH0.DX5D	USIC0_CH1.DX3E	USIC0_CH1.DX4E
P2.6													VADC0.G0CH0		ERU0.2A1	USIC0_CH0.DX3E	USIC0_CH0.DX4E	USIC0_CH1.DX5D
P2.7													VADC0.G1CH1		ERU0.3A1	USIC0_CH0.DX5C	USIC0_CH1.DX3D	USIC0_CH1.DX4D
P2.8													VADC0.G0CH1	VADC0.G1CH0	ERU0.3B1	USIC0_CH0.DX3D	USIC0_CH0.DX4D	USIC0_CH1.DX5C
P2.9													VADC0.G0CH2	VADC0.G1CH4	ERU0.3B0	USIC0_CH0.DX5A	USIC0_CH1.DX3B	USIC0_CH1.DX4B
P2.10	ERU0.PDOUT1	CCU40.OUT2	ERU0.GOUT1				USIC0_CH1.DOUT0						VADC0.G0CH3	VADC0.G1CH2	ERU0.2B0	USIC0_CH0.DX3C	USIC0_CH0.DX4C	USIC0_CH1.DX0F
P2.11	ERU0.PDOUT0	CCU40.OUT3	ERU0.GOUT0			USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0						VADC0.G0CH4	VADC0.G1CH3	ERU0.2B1	USIC0_CH1.DX0E	USIC0_CH1.DX1E	

Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	0.85 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)[3]
Input Hysteresis[1]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), Standard Hysteresis
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			0.5 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(5 V), Large Hysteresis
			0.4 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(3.3 V), Large Hysteresis
			0.2 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode(2.2 V), Large Hysteresis
Pull-up resistor on port pins	R_{PUP}	CC	20	50	kohm	$V_{IN} = V_{SSP}$
Pull-down resistor on port pins	R_{PDP}	CC	20	50	kohm	$V_{IN} = V_{DDP}$
Input leakage current[2]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Overload current on any pin	I_{OVP}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	[3]
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[4]
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	–
Maximum current per high currrent pins	I_{MP1A}	SR	-10	50	mA	–

Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (TSSOP28/16, VQFN24)	I_{MVDD1}	SR	–	130	mA	[3)]
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	[3)]
Maximum current out of V_{SS} (TSSOP28/16, VQFN24)	I_{MVSS1}	SR	–	130	mA	[3)]
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	[3)]

1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Not subject to production test, verified by design/characterization.

4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.3 AC Parameters

3.3.1 Testing Waveforms

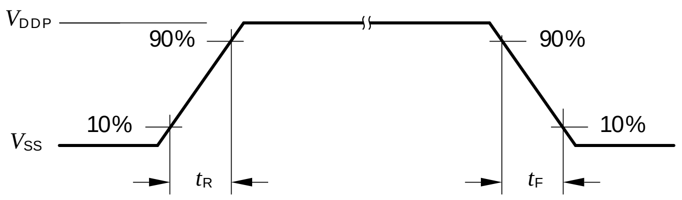

Figure 9 Rise/Fall Time Parameters

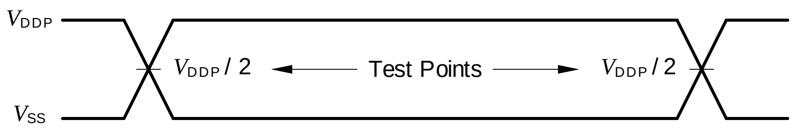

Figure 10 Testing Waveform, Output Delay

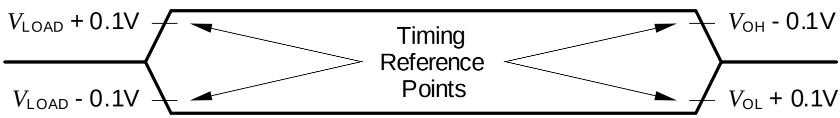

Figure 11 Testing Waveform, Output High Impedance

3.3.2 Output Rise/Fall Times

Table 17 provides the characteristics of the output rise/fall times in the XMC1100. **Figure 9** describes the rise time and fall time parameters.

Table 17 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on High Current Pad[1)2)]	t_{HCPR}, t_{HCPF}	–	9	ns	50 pF @ 5 V[3)]
		–	12	ns	50 pF @ 3.3 V[4)]
		–	25	ns	50 pF @ 1.8 V[5)]
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	12	ns	50 pF @ 5 V[6)]
		–	15	ns	50 pF @ 3.3 V[7)].
		–	31	ns	50 pF @ 1.8 V[8)].

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
4) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
7) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
8) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.

3.3.4 On-Chip Oscillator Characteristics

Table 19 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1100.

Table 19 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	63.5	64	64.5	MHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)[2]
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[2]
Accuracy with calibration based on temperature sensor	Δf_{LTT}	CC	-1.3	–	1.25	%	with respect to f_{NOM}(typ), over temperature (T_A = 0 °C to 105 °C)[2]
			-2.6	–	1.25	%	with respect to f_{NOM}(typ), over temperature (T_A = -40 °C to 105 °C)[2]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

Figure 13 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

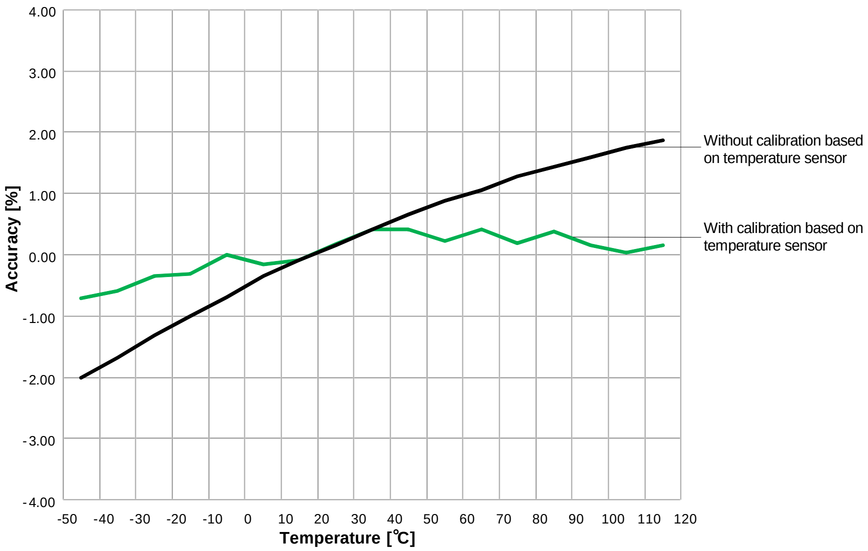

Figure 13 Typical DCO1 accuracy over temperature

Table 20 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1100.

Table 20 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	32.5	32.75	33	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)[2]
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[2]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 21 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK high time	t_1	SR	50	–	500000	ns	–
SWDCLK low time	t_2	SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3	SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4	SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5	CC	–	–	68	ns	C_L = 50 pF
			–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	CC	4	–	–	ns	

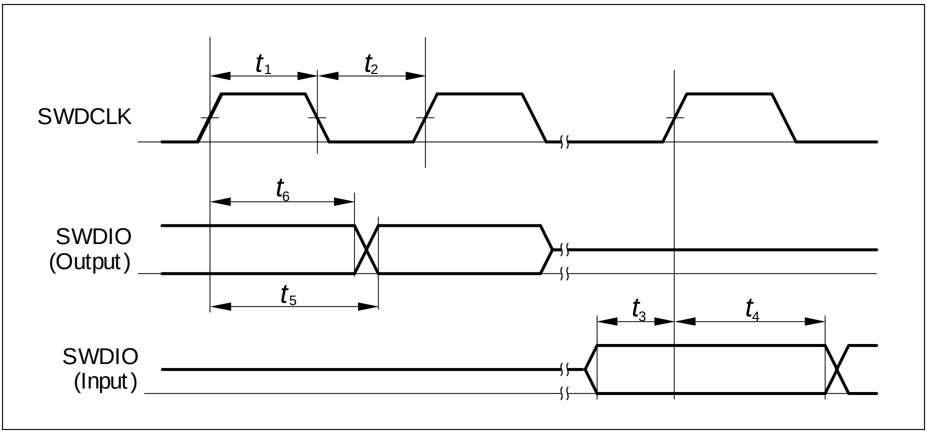

Figure 14 SWD Timing

Table 24 USIC SSC Slave Mode Timing (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1)]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1)]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

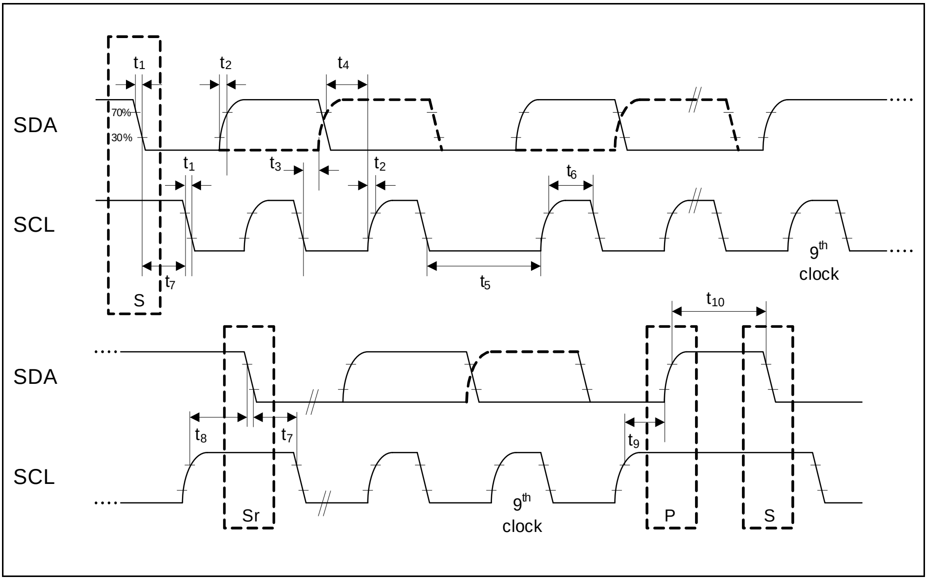

Figure 16 USIC IIC Stand and Fast Mode Timing

3.3.7.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 27 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$2/f_{MCLK}$	-	-	ns	$V_{DDP} \geq 3$ V
		$4/f_{MCLK}$	-	-	ns	$V_{DDP} < 3$ V
Clock HIGH	t_2 CC	0.35 x t_{1min}	-	-	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	0.15 x t_{1min}	ns	

4.2 Package Outlines

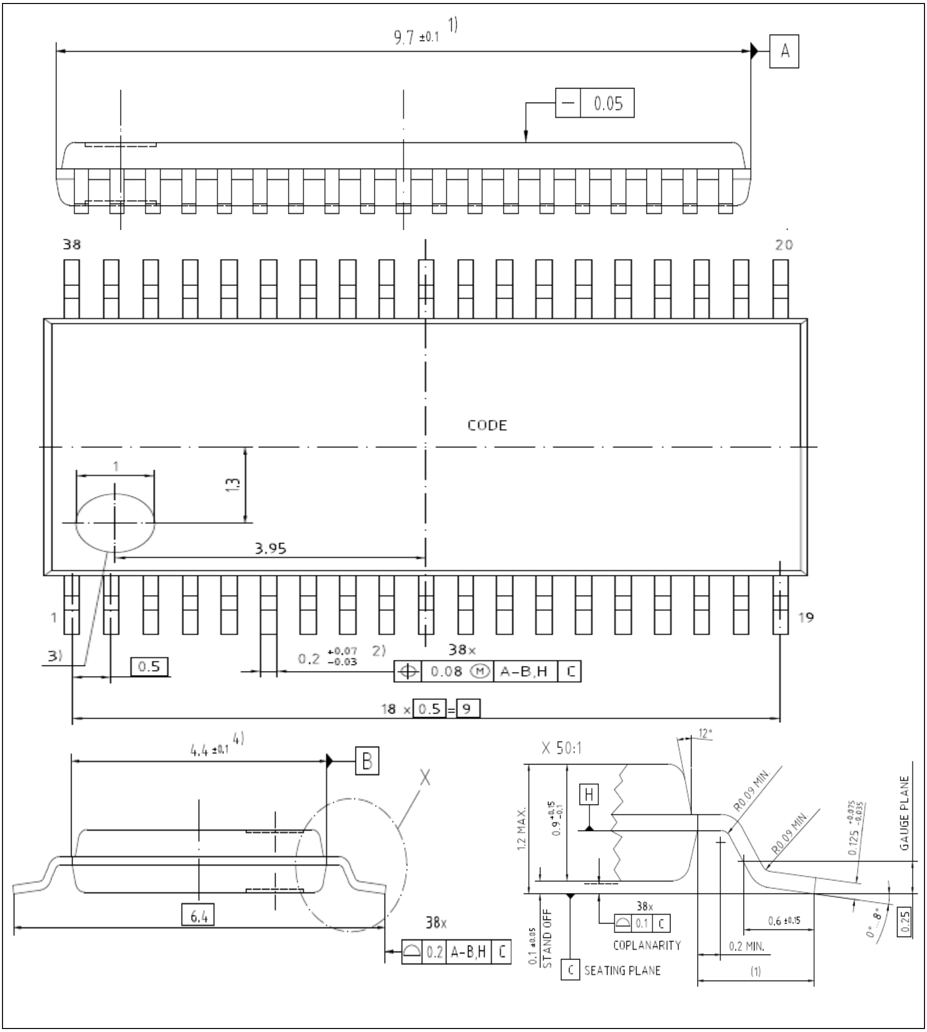

Figure 19 PG-TSSOP-38-9

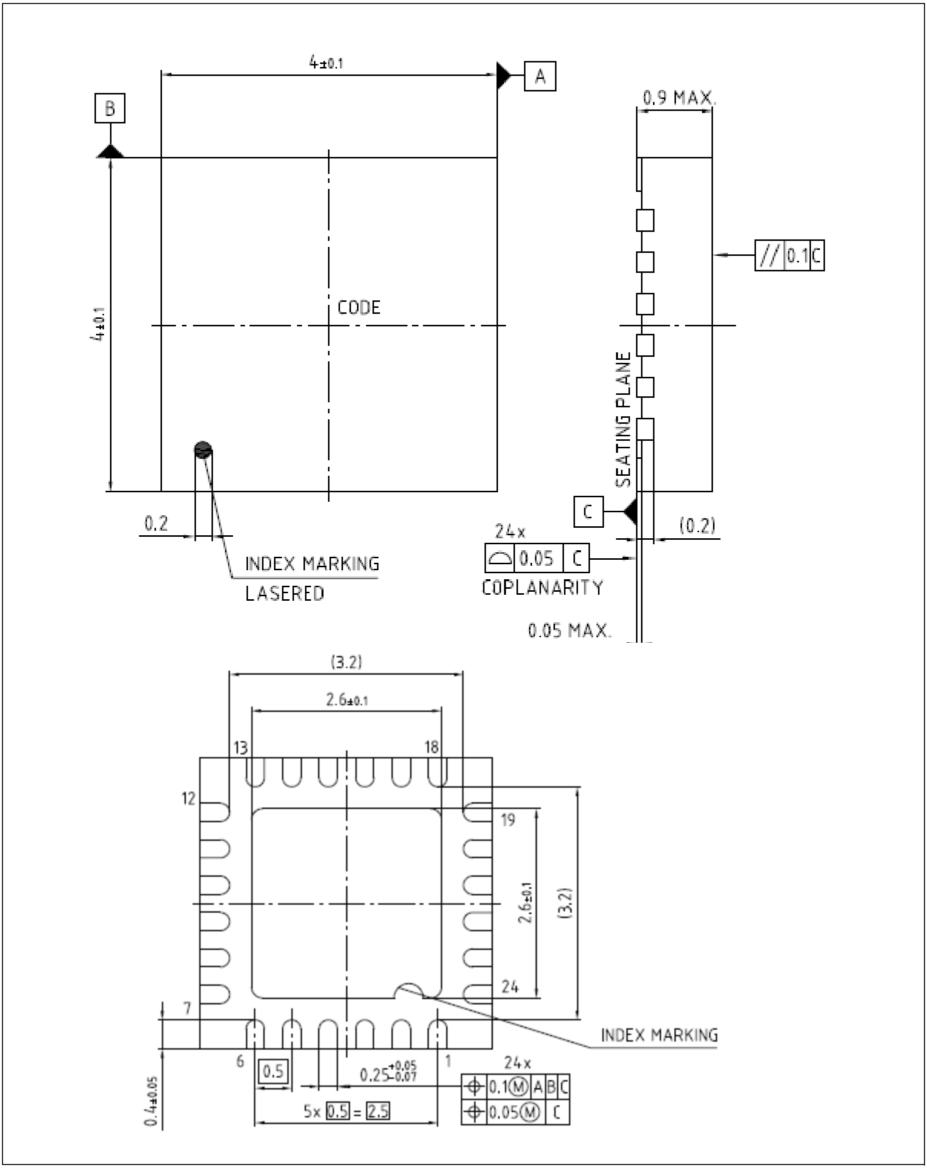

Figure 21 PG-VQFN-24-19

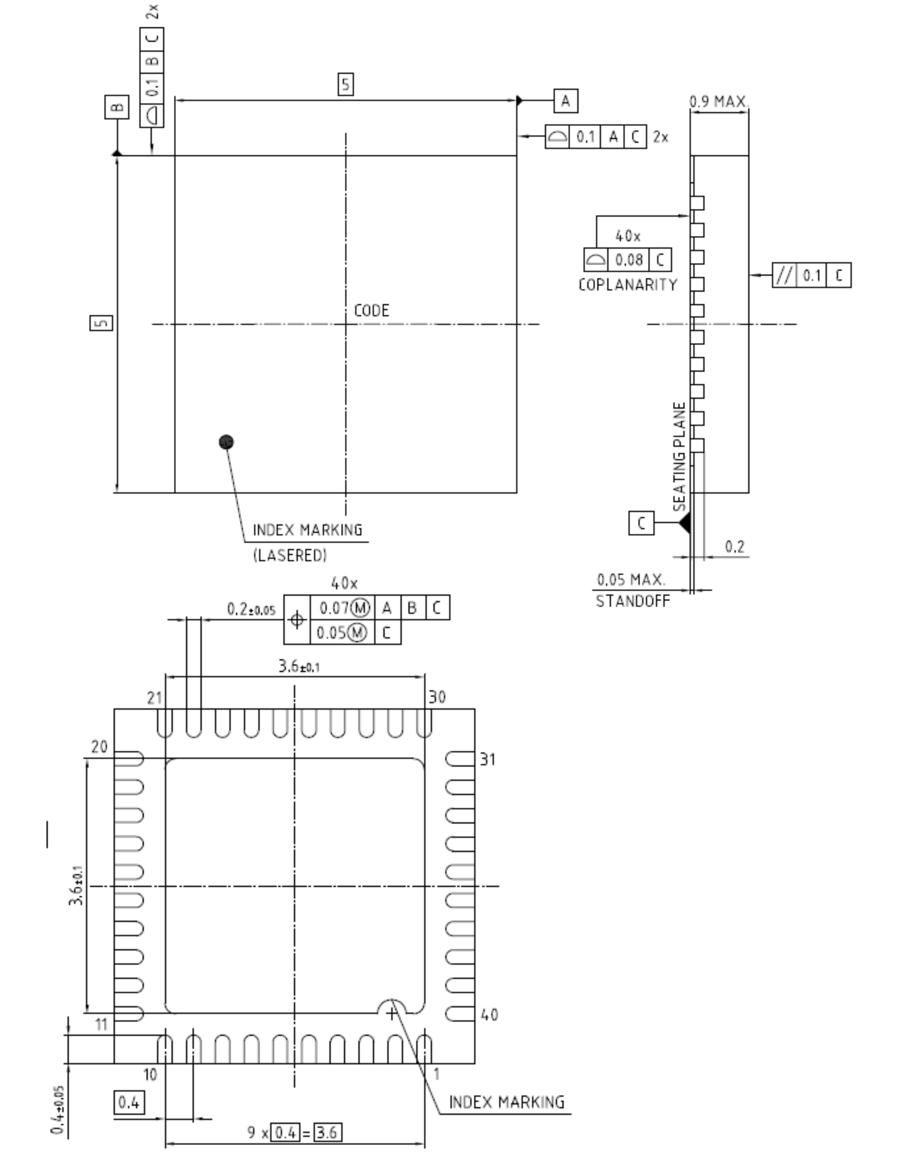

Figure 22 PG-VQFN-40-13

All dimensions in mm.