Infineon Technologies - XMC1100T016F0032AAXUMA1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	11
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100t016f0032aaxuma1

XMC1100 Data Sheet

Revision History: V1.4 2014-05

Previous Version: V1.3	
Page	Subjects
Page 10	ADC channels of Table 2 is updated. Table 3 is added.
Page 10	Description for Chip Identification Number of Section 1.4 is updated.
Page 17	The pad type is corrected for P1.6 in Table 6.
Page 29	The t_{C12} , f_{C12}, t_{C10}, f_{C10}, t_{C8} and f_{C8} parameters are updated in Table 12.
Page 32	Figure 8 is added.
Page 33	The t_{SR} and t_{TSAL} parameters are updated in Table 13.
Page 36	Parameter name for t_{PSER} is updated. The $N_{WSFLASH}$ parameter and test condition for t_{RET} are added to Table 16.
Page 39	The min value for V_{DDPBO} parameter is added to Table 18. Footnote 1 is updated.
Page 41	The Δf_{LTT} parameter is added to Table 19.
Page 47	Figure 13 is added.

Trademarks

C166™, TriCore™ and DAVE™ are trademarks of Infineon Technologies AG.

ARM®, ARM Powered® and AMBA® are registered trademarks of ARM, Limited.

Cortex™, CoreSight™, ETM™, Embedded Trace Macrocell™ and Embedded Trace Buffer™ are trademarks of ARM, Limited.

We Listen to Your Comments

Is there any information in this document that you feel is wrong, unclear or missing? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

Table of Contents

1 Summary of Features 7
1.1 Ordering Information 8
1.2 Device Types 9
1.3 Device Type Features 10
1.4 Chip Identification Number 10

2 General Device Information 12
2.1 Logic Symbols 12
2.2 Pin Configuration and Definition 14
2.2.1 Package Pin Summary 17
2.2.2 Port I/O Functions 20

3 Electrical Parameter 23
3.1 General Parameters 23
3.1.1 Parameter Interpretation 23
3.1.2 Absolute Maximum Ratings 24
3.1.3 Operating Conditions 25
3.2 DC Parameters 26
3.2.1 Input/Output Characteristics 26
3.2.2 Analog to Digital Converters (ADC) 29
3.2.3 Temperature Sensor Characteristics 33
3.2.4 Power Supply Current 34
3.2.5 Flash Memory Parameters 36
3.3 AC Parameters 37
3.3.1 Testing Waveforms 37
3.3.2 Output Rise/Fall Times 38
3.3.3 Power-Up and Supply Threshold Charcteristics 39
3.3.4 On-Chip Oscillator Characteristics 41
3.3.5 Serial Wire Debug Port (SW-DP) Timing 43
3.3.6 SPD Timing Requirements 44
3.3.7 Peripheral Timings 45
3.3.7.1 Synchronous Serial Interface (USIC SSC) Timing 45
3.3.7.2 Inter-IC (IIC) Interface Timing 48
3.3.7.3 Inter-IC Sound (IIS) Interface Timing 50

4 Package and Reliability 52
4.1 Package Parameters 52
4.1.1 Thermal Considerations 52
4.2 Package Outlines 54

5 Quality Declaration 58

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1100 series devices.

The document describes the characteristics of a superset of the XMC1100 series devices. For simplicity, the various device types are referred to by the collective term XMC1100 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

1 Summary of Features

The XMC1100 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1100 series devices are designed for general purpose applications.

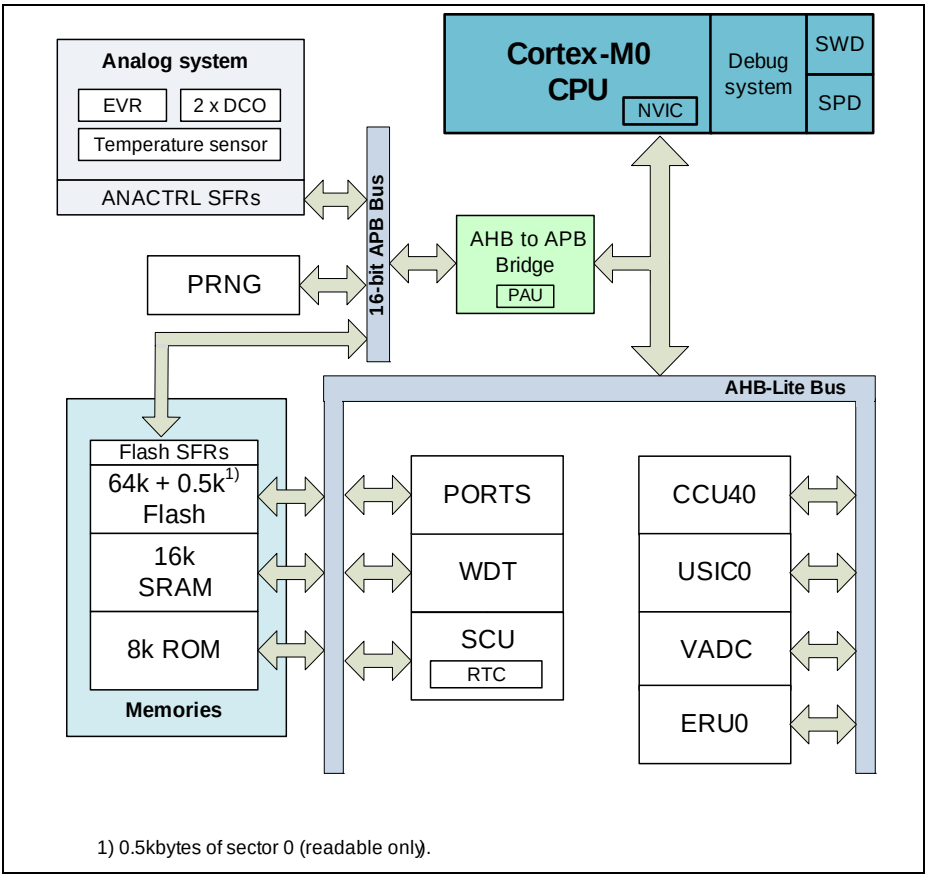

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M0 CPU
  - Most of 16-bit Thumb instruction set
  - Subset of 32-bit Thumb2 instruction set

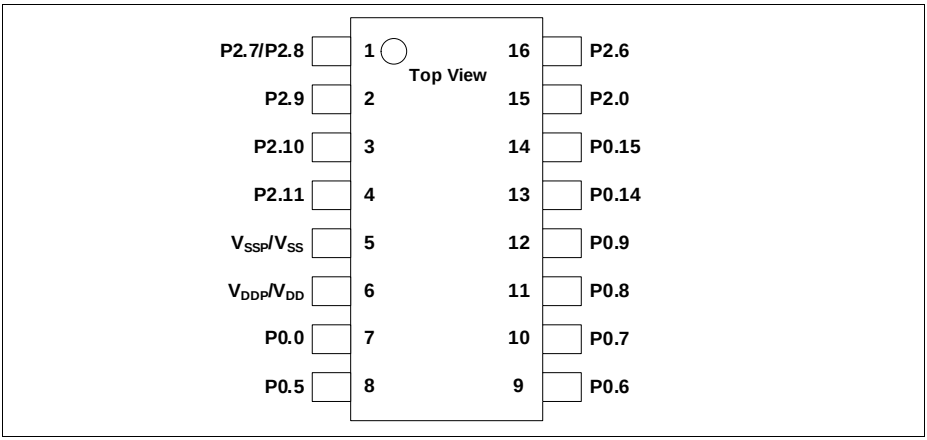

Figure 5 XMC1100 **PG-TSSOP-16 Pin Configuration** (top view)

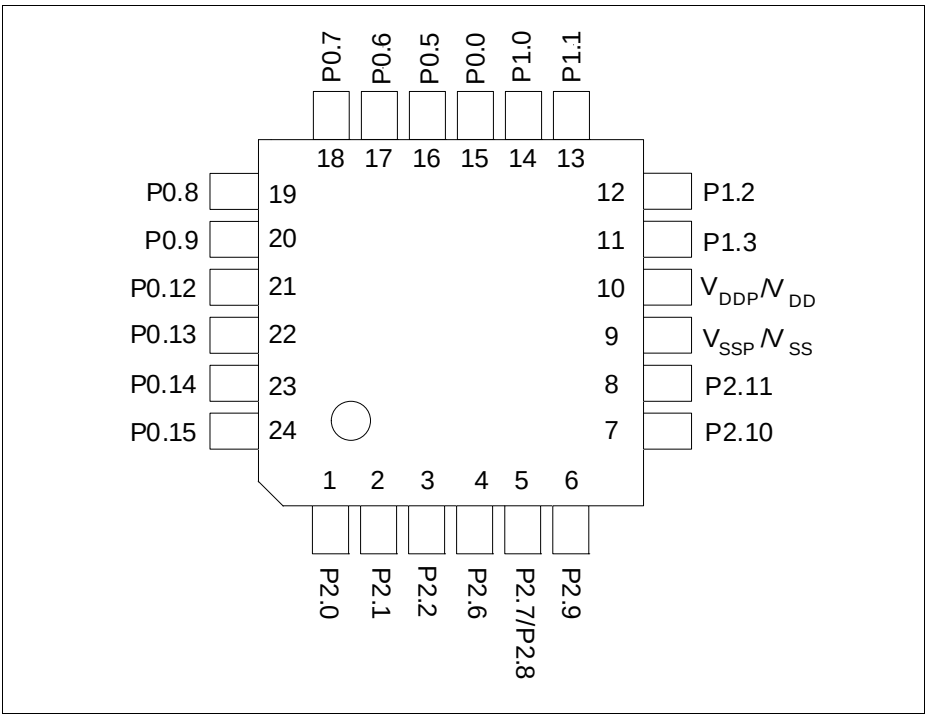

Figure 6 XMC1100 **PG-VQFN-24 Pin Configuration** (top view)

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P0.13	38	32	22	-	STD_INOUT	
P0.14	39	33	23	13	STD_INOUT	
P0.15	40	34	24	14	STD_INOUT	
P1.0	22	16	14	-	High Current	
P1.1	21	15	13	-	High Current	
P1.2	20	14	12	-	High Current	
P1.3	19	13	11	-	High Current	
P1.4	18	12	-	-	High Current	
P1.5	17	11	-	-	High Current	
P1.6	16	-	-	-	STD_INOUT	
P2.0	1	35	1	15	STD_INOUT/AN	
P2.1	2	36	2	-	STD_INOUT/AN	
P2.2	3	37	3	-	STD_IN/AN	
P2.3	4	38	-	-	STD_IN/AN	
P2.4	5	1	-	-	STD_IN/AN	
P2.5	6	2	-	-	STD_IN/AN	
P2.6	7	3	4	16	STD_IN/AN	
P2.7	8	4	5	1	STD_IN/AN	
P2.8	9	5	5	1	STD_IN/AN	
P2.9	10	6	6	2	STD_IN/AN	
P2.10	11	7	7	3	STD_INOUT/AN	
P2.11	12	8	8	4	STD_INOUT/AN	
VSS	13	9	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage. VDD has to be supplied with the same voltage as VDDP

Table 8 Port I/O Functions

Function	Outputs									Inputs								
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.PDOUT0		ERU0.GOUT0	CCU40.OUT0		USIC0_CH0.SELO0	USIC0_CH1.SELO0					CCU40.IN0C				USIC0_CH0.DX2A	USIC0_CH1.DX2A	
P0.1	ERU0.PDOUT1		ERU0.GOUT1	CCU40.OUT1			SCU.VDROP					CCU40.IN1C						
P0.2	ERU0.PDOUT2		ERU0.GOUT2	CCU40.OUT2		VADC0.EMUX02						CCU40.IN2C						
P0.3	ERU0.PDOUT3		ERU0.GOUT3	CCU40.OUT3		VADC0.EMUX01						CCU40.IN3C						
P0.4				CCU40.OUT1		VADC0.EMUX00	WWDT.SERVICE_OUT											
P0.5				CCU40.OUT0														
P0.6				CCU40.OUT0		USIC0_CH1.MCLKOUT	USIC0_CH1.DOUT0					CCU40.IN0B				USIC0_CH1.DX0C		
P0.7				CCU40.OUT1		USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0					CCU40.IN1B				USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C
P0.8				CCU40.OUT2		USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT					CCU40.IN2B				USIC0_CH0.DX1B	USIC0_CH1.DX1B	
P0.9				CCU40.OUT3		USIC0_CH0.SELO0	USIC0_CH1.SELO0					CCU40.IN3B				USIC0_CH0.DX2B	USIC0_CH1.DX2B	
P0.10						USIC0_CH0.SELO1	USIC0_CH1.SELO1									USIC0_CH0.DX2C	USIC0_CH1.DX2C	
P0.11				USIC0_CH0.MCLKOUT		USIC0_CH0.SELO2	USIC0_CH1.SELO2									USIC0_CH0.DX2D	USIC0_CH1.DX2D	
P0.12						USIC0_CH0.SELO3						CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0.DX2E		
P0.13	WWDT.SERVICE_OUT					USIC0_CH0.SELO4										USIC0_CH0.DX2F		
P0.14						USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT									USIC0_CH0.DX0A	USIC0_CH0.DX1A	
P0.15						USIC0_CH0.DOUT0	USIC0_CH1.MCLKOUT									USIC0_CH0.DX0B		
P1.0		CCU40.OUT0					USIC0_CH0.DOUT0		USIC0_CH0.DOUT0		USIC0_CH0.HWIN0					USIC0_CH0.DX0C		
P1.1	VADC0.EMUX00	CCU40.OUT1				USIC0_CH0.DOUT0	USIC0_CH1.SELO0		USIC0_CH0.DOUT1		USIC0_CH0.HWIN1					USIC0_CH0.DX0D	USIC0_CH0.DX1D	USIC0_CH1.DX2E
P1.2	VADC0.EMUX01	CCU40.OUT2					USIC0_CH1.DOUT0		USIC0_CH0.DOUT2		USIC0_CH0.HWIN2					USIC0_CH1.DX0B		
P1.3	VADC0.EMUX02	CCU40.OUT3				USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0		USIC0_CH0.DOUT3		USIC0_CH0.HWIN3					USIC0_CH1.DX0A	USIC0_CH1.DX1A	
P1.4	VADC0.EMUX10	USIC0_CH1.SCLKOUT				USIC0_CH0.SELO0	USIC0_CH1.SELO1									USIC0_CH0.DX5E	USIC0_CH1.DX5E	
P1.5	VADC0.EMUX11	USIC0_CH0.DOUT0				USIC0_CH0.SELO1	USIC0_CH1.SELO2									USIC0_CH1.DX5F		

3.2.2 Analog to Digital Converters (ADC)

Table 12 shows the Analog to Digital Converter (ADC) characteristics.

Table 12 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	1.8	–	3.0	V	SHSCFG.AREF = 11_B
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground (SH0-CH0, SH1-CH0)	V_{REFGND} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Internal reference voltage (full scale value)	V_{REFINT} CC	4.82	5	5.18	V	-40°C - 105°C
		4.9	5	5.1	V	0°C - 85°C [1]
Switched capacitance of an analog input[1]	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	[1]
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	[1]

Table 12 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC		1		–	GNCTRxz.GAINy = 00_B (unity gain)
			3		–	GNCTRxz.GAINy = 01_B (gain g1)
			6		–	GNCTRxz.GAINy = 10_B (gain g2)
			12		–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	V_{DDP} = 5.0 V
		3	–	–	1 / f_{ADC}	V_{DDP} = 3.3 V
		30	–	–	1 / f_{ADC}	V_{DDP} = 1.8 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC		9		1 / f_{ADC}	2)
Conversion time in 12-bit mode	t_{C12} CC		20		1 / f_{ADC}	2)
Maximum sample rate in 12-bit mode 3)	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC		18		1 / f_{ADC}	2)
Maximum sample rate in 10-bit mode 3)	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC		16		1 / f_{ADC}	2)

3.2.3 Temperature Sensor Characteristics

Table 13 Temperature Sensor Characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[2)]	T_{TSAL} CC	–	+/-20	–	°C	T_J = -40 °C (calibrated)
		–	+/-12	–	°C	T_J = -25 °C (calibrated)
		-5	–	5	°C	T_J = 0 °C
		-2	–	2	°C	T_J = 25 °C (calibrated)
		-4	–	4	°C	T_J = 70 °C
		-2	–	2	°C	T_J = 115 °C (calibrated)

1) Not subject to production test, verified by design/characterization.

2) The temperature sensor accuracy is independent of the supply voltage.

3.2.4 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Table 14 Power Supply Parameters[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[2)]	Max.		
Active mode current[3)]	I_{DDPA} CC	–	8.4	11.0	mA	f_{MCLK} = 32 MHz f_{PCLK} = 64 MHz
		–	3.7	–	mA	f_{MCLK} = 1 MHz f_{PCLK} = 1 MHz
Sleep mode current Peripherals clock enabled[4)]	I_{DDPSE} CC	–	5.9	–	mA	f_{MCLK} = 32 MHz f_{PCLK} = 64 MHz
Sleep mode current Peripherals clock disabled[5)]	I_{DDPSD} CC	–	1.2	–	mA	f_{MCLK} = 1 MHz f_{PCLK} = 1 MHz
Deep Sleep mode current[6)]	I_{DDPDS} CC	–	0.24	–	mA	
Wake-up time from Sleep to Active mode[7)]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[8)]	t_{DSA} CC	–	280	–	µsec	

1) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
2) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V.
3) CPU and all peripherals clock enabled, Flash is in active mode.
4) CPU is sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU is sleep, Flash is powered down and code executed from RAM after wake-up.
6) CPU is sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
7) CPU is sleep, Flash is in active mode during sleep mode.
8) CPU is sleep, Flash is in power down mode during deep sleep mode.

3.3 AC Parameters

3.3.1 Testing Waveforms

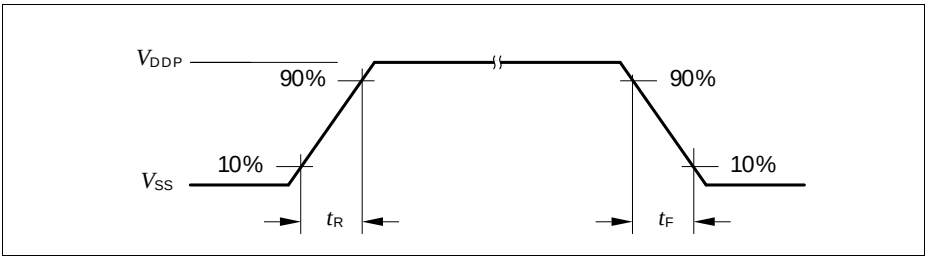

Figure 9 Rise/Fall Time Parameters

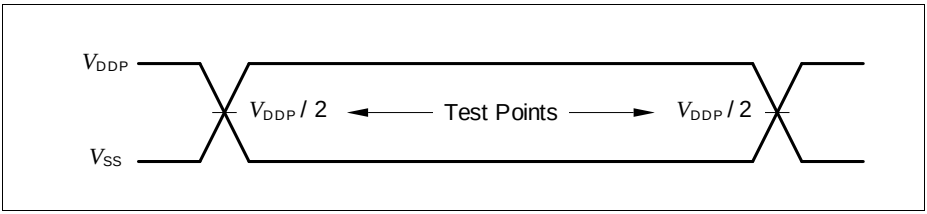

Figure 10 Testing Waveform, Output Delay

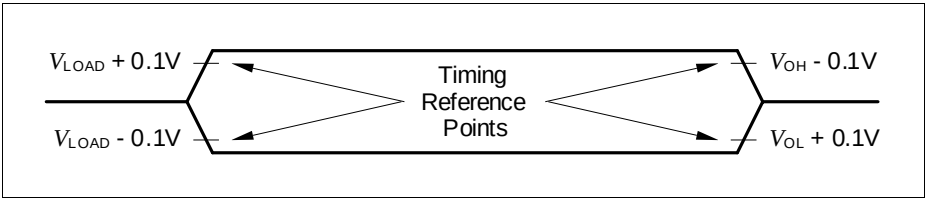

Figure 11 Testing Waveform, Output High Impedance

3.3.2 Output Rise/Fall Times

Table 17 provides the characteristics of the output rise/fall times in the XMC1100. **Figure 9** describes the rise time and fall time parameters.

Table 17 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on High Current Pad[1)2)]	t_{HCPR}, t_{HCPF}	–	9	ns	50 pF @ 5 V[3)]
		–	12	ns	50 pF @ 3.3 V[4)]
		–	25	ns	50 pF @ 1.8 V[5)]
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	12	ns	50 pF @ 5 V[6)]
		–	15	ns	50 pF @ 3.3 V[7)].
		–	31	ns	50 pF @ 1.8 V[8)].

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
4) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
7) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
8) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.

Figure 13 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

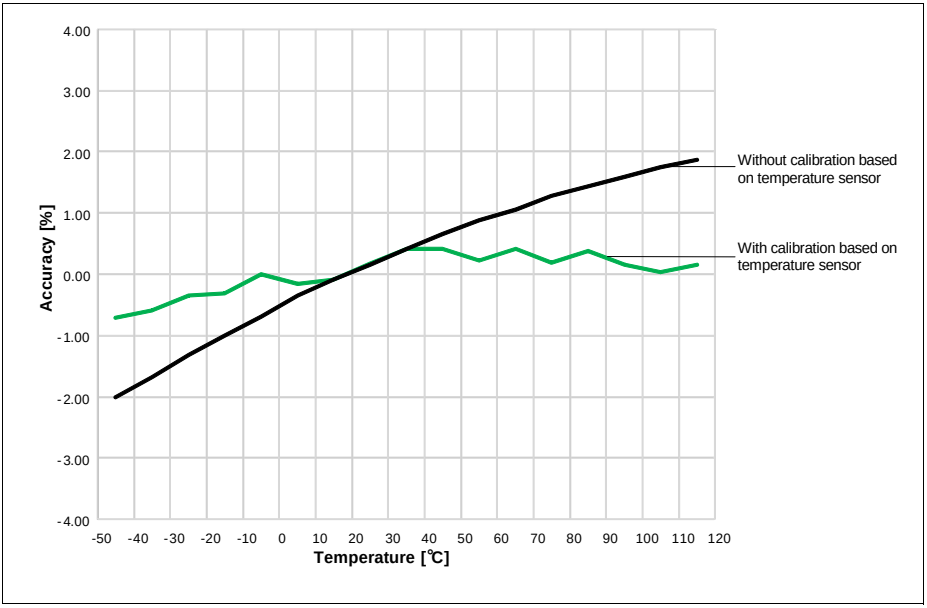

Figure 13 Typical DCO1 accuracy over temperature

Table 20 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1100.

Table 20 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	32.5	32.75	33	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)[2]
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[2]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

Table 24 USIC SSC Slave Mode Timing (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

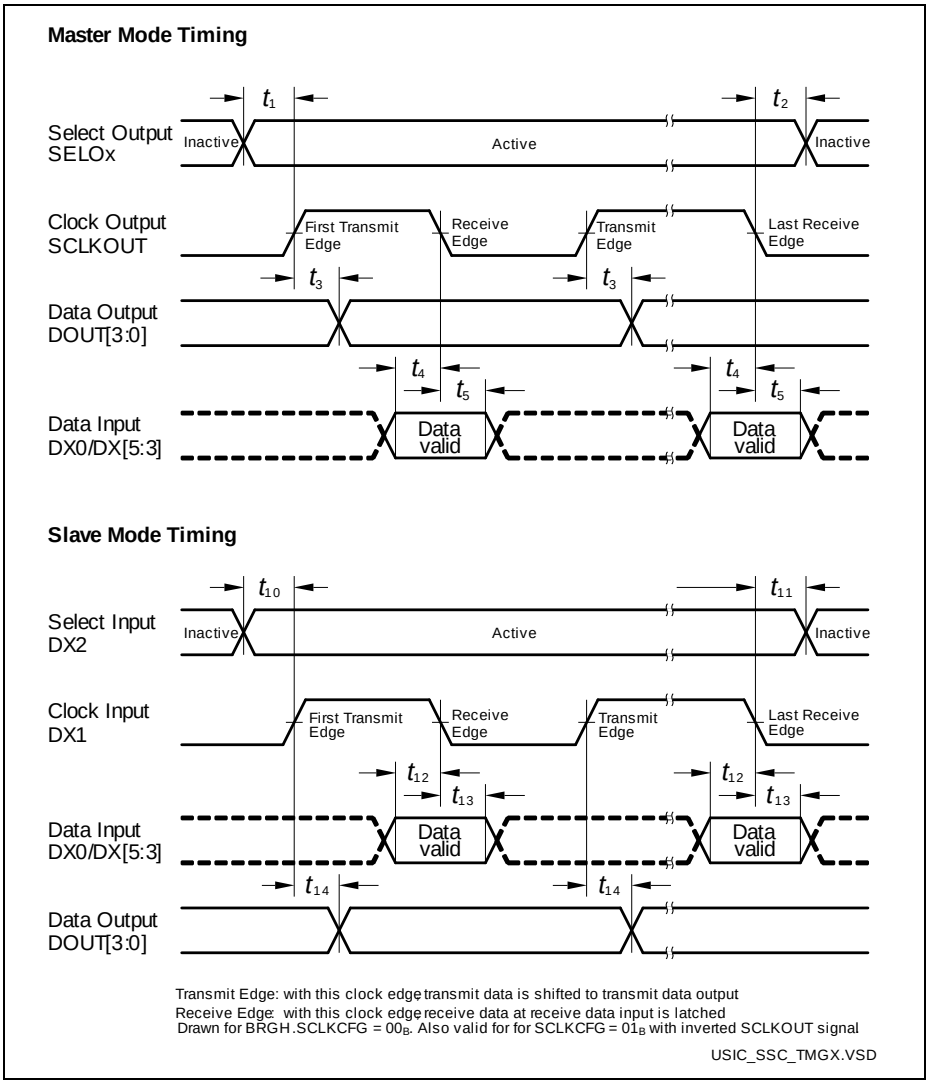

Figure 15 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

Table 26 USIC IIC Fast Mode Timing [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

4 Package and Reliability

The XMC1100 is a member of the XMC1000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 29 provides the thermal characteristics of the packages used in XMC1100.

Table 29 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8[1)]
		-	70.3	K/W	PG-TSSOP-38-9[1)]
		-	46.0	K/W	PG-VQFN-24-19[1)]
		-	38.4	K/W	PG-VQFN-40-13[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1100 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

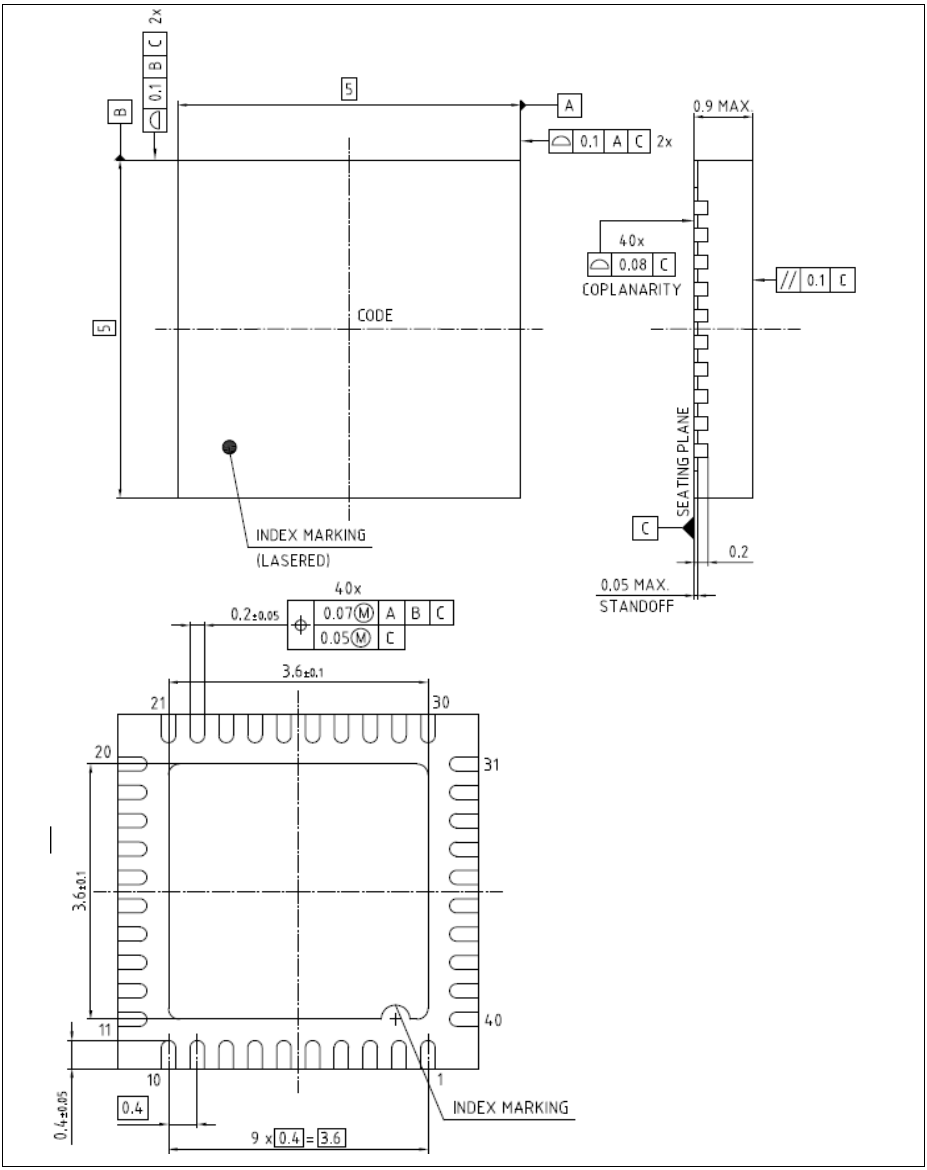

Figure 22 PG-VQFN-40-13

All dimensions in mm.

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG