Infineon Technologies - XMC1100T016X0032AAXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	11
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100t016x0032aaxuma1

Edition 2014-05

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XMC1100 Data Sheet

Revision History: V1.4 2014-05

Previous Version: V1.3	
Page	Subjects
Page 10	ADC channels of Table 2 is updated. Table 3 is added.
Page 10	Description for Chip Identification Number of Section 1.4 is updated.
Page 17	The pad type is corrected for P1.6 in Table 6.
Page 29	The t_{C12} , f_{C12}, t_{C10}, f_{C10}, t_{C8} and f_{C8} parameters are updated in Table 12.
Page 32	Figure 8 is added.
Page 33	The t_{SR} and t_{TSAL} parameters are updated in Table 13.
Page 36	Parameter name for t_{PSER} is updated. The $N_{WSFLASH}$ parameter and test condition for t_{RET} are added to Table 16.
Page 39	The min value for V_{DDPBO} parameter is added to Table 18. Footnote 1 is updated.
Page 41	The Δf_{LTT} parameter is added to Table 19.
Page 47	Figure 13 is added.

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1 Summary of Features

The XMC1100 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1100 series devices are designed for general purpose applications.

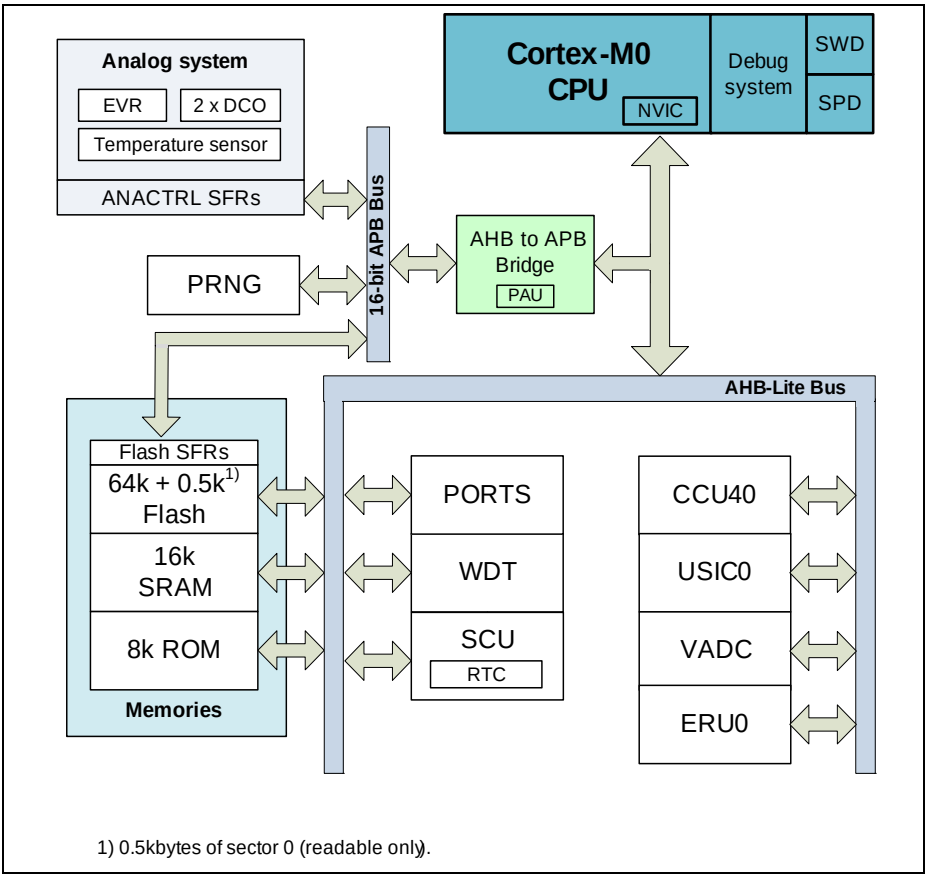

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M0 CPU
  - Most of 16-bit Thumb instruction set
  - Subset of 32-bit Thumb2 instruction set

  - High code density with 32-bit performance
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support
  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 64 kbytes on-chip Flash program and data memory

On-Chip Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- A/D Converters, up to 12 channels, includes a 12-bit analog to digital converter
- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times
- Temperature Sensor (TSE)

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set

Table 4 XMC1100 **Chip Identification Number**

Derivative	Value	Marking
XMC1100-T016F0008	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00003000 $101ED083_H$	AA
XMC1100-T016F0016	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 $101ED083_H$	AA
XMC1100-T016F0032	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 $101ED083_H$	AA
XMC1100-T016F0064	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 $101ED083_H$	AA
XMC1100-T016X0064	00011033 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 $101ED083_H$	AA
XMC1100-T038F0016	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 $101ED083_H$	AA
XMC1100-T038F0032	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 $101ED083_H$	AA
XMC1100-T038F0064	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 $101ED083_H$	AA
XMC1100-T038X0064	00011013 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 $101ED083_H$	AA
XMC1100-Q024F0008	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00003000 $101ED083_H$	AA
XMC1100-Q024F0016	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 $101ED083_H$	AA
XMC1100-Q024F0032	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 $101ED083_H$	AA
XMC1100-Q024F0064	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 $101ED083_H$	AA
XMC1100-Q040F0016	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 $101ED083_H$	AA
XMC1100-Q040F0032	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 $101ED083_H$	AA
XMC1100-Q040F0064	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 $101ED083_H$	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

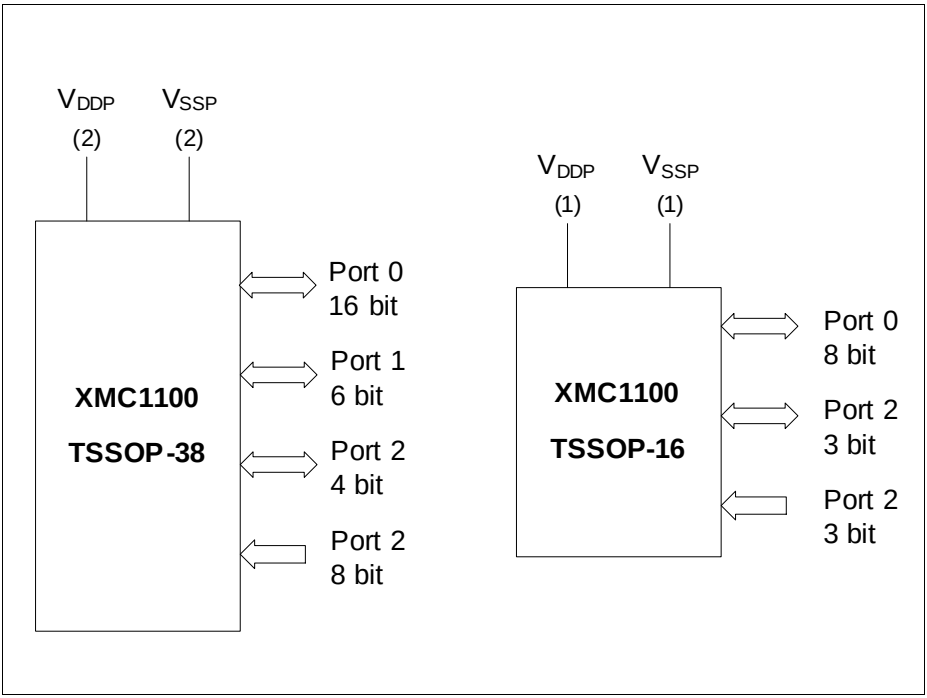

Figure 2 XMC1100 Logic Symbol for TSSOP-38 and TSSOP-16

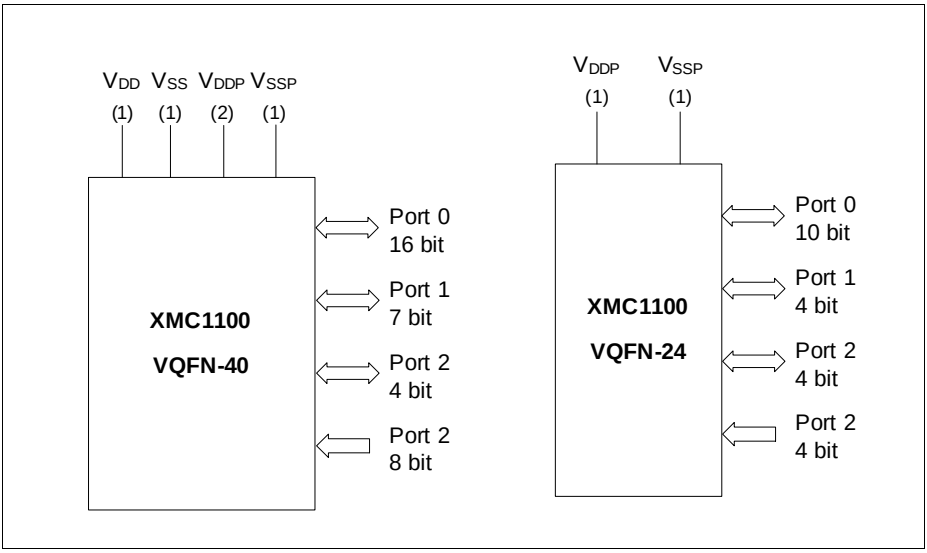

Figure 3 XMC1100 Logic Symbol for VQFN-24 and VQFN-40

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

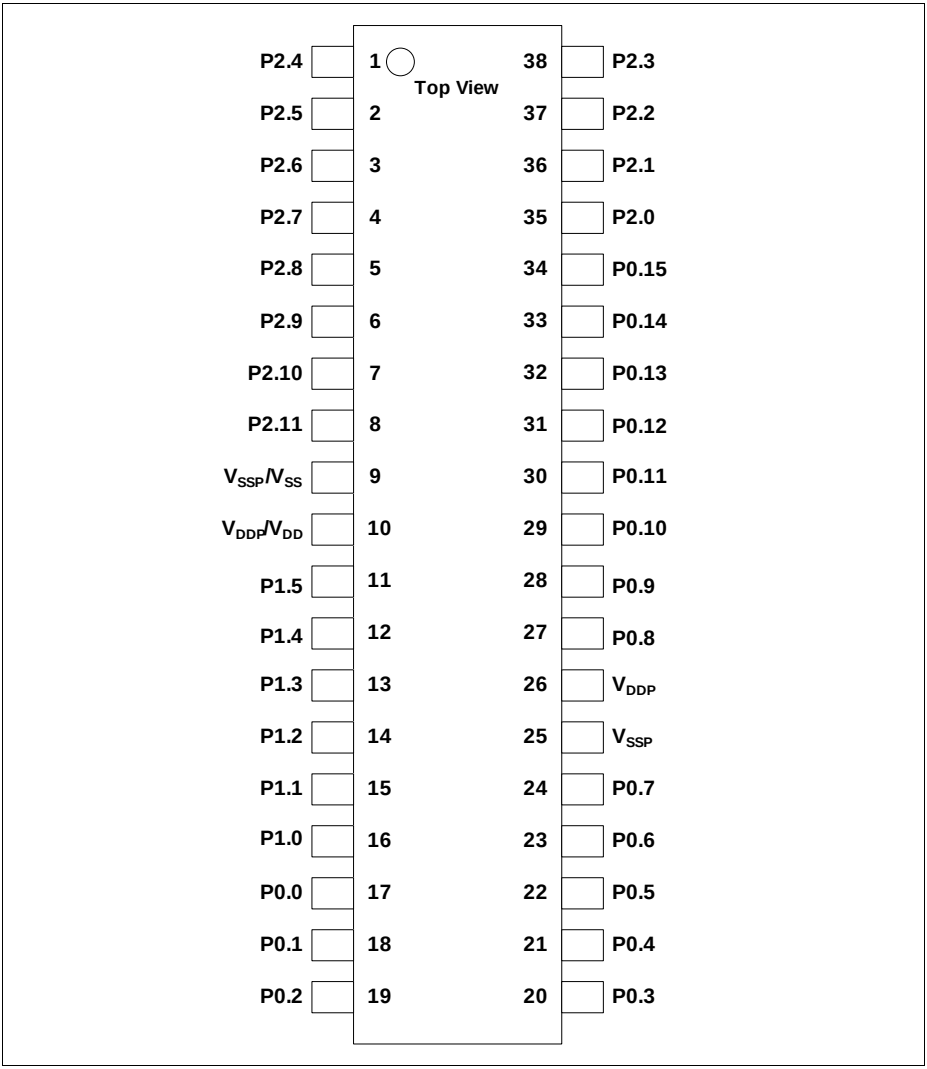

Figure 4 XMC1100 **PG-TSSOP-38 Pin Configuration** (top view)

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P0.13	38	32	22	-	STD_INOUT	
P0.14	39	33	23	13	STD_INOUT	
P0.15	40	34	24	14	STD_INOUT	
P1.0	22	16	14	-	High Current	
P1.1	21	15	13	-	High Current	
P1.2	20	14	12	-	High Current	
P1.3	19	13	11	-	High Current	
P1.4	18	12	-	-	High Current	
P1.5	17	11	-	-	High Current	
P1.6	16	-	-	-	STD_INOUT	
P2.0	1	35	1	15	STD_INOUT/AN	
P2.1	2	36	2	-	STD_INOUT/AN	
P2.2	3	37	3	-	STD_IN/AN	
P2.3	4	38	-	-	STD_IN/AN	
P2.4	5	1	-	-	STD_IN/AN	
P2.5	6	2	-	-	STD_IN/AN	
P2.6	7	3	4	16	STD_IN/AN	
P2.7	8	4	5	1	STD_IN/AN	
P2.8	9	5	5	1	STD_IN/AN	
P2.9	10	6	6	2	STD_IN/AN	
P2.10	11	7	7	3	STD_INOUT/AN	
P2.11	12	8	8	4	STD_INOUT/AN	
VSS	13	9	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage. VDD has to be supplied with the same voltage as VDDP

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 11 provides the characteristics of the input/output pins of the XMC1100.

Table 11 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
			–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
			–	0.32	V	I_{OL} = 10 mA (5 V)
			–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on high current pads	V_{OHP1}	CC	V_{DDP} - 0.32	–	V	I_{OH} = -6 mA (5 V)
			V_{DDP} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	0.19 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	0.7 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	–	0.08 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)[3)]

Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (TSSOP28/16, VQFN24)	I_{MVDD1}	SR	–	130	mA	3)
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	3)
Maximum current out of V_{SS} (TSSOP28/16, VQFN24)	I_{MVSS1}	SR	–	130	mA	3)
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	3)

1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Not subject to production test, verified by design/characterization.

4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.3.2 Output Rise/Fall Times

Table 17 provides the characteristics of the output rise/fall times in the XMC1100. **Figure 9** describes the rise time and fall time parameters.

Table 17 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on High Current Pad[1)2)]	t_{HCPR}, t_{HCPF}	–	9	ns	50 pF @ 5 V[3)]
		–	12	ns	50 pF @ 3.3 V[4)]
		–	25	ns	50 pF @ 1.8 V[5)]
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	12	ns	50 pF @ 5 V[6)]
		–	15	ns	50 pF @ 3.3 V[7)].
		–	31	ns	50 pF @ 1.8 V[8)].

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
4) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
7) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
8) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.

3.3.3 Power-Up and Supply Threshold Charcteristics

Table 18 provides the characteristics of the supply threshold in XMC1100.

Table 18 Power-Up and Supply Threshold Parameters (Operating Conditions apply) [1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/- 10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$ [2] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[3]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_ SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_ SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_ SELECT = 10_B
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
Start-up time from power-on reset	t_{SSW} SR	–	320	–	µs	Time to the first user code instruction[4]

1) Not all parameters are 100% tested, but are verified by design/characterisation.

2) A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.

3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

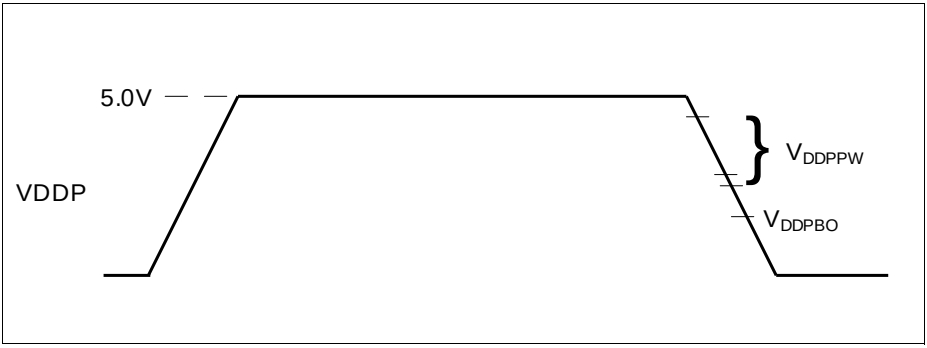

Figure 12 Supply Threshold Parameters

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 21 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	68	ns	C_L = 50 pF
		–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	–	–	ns	

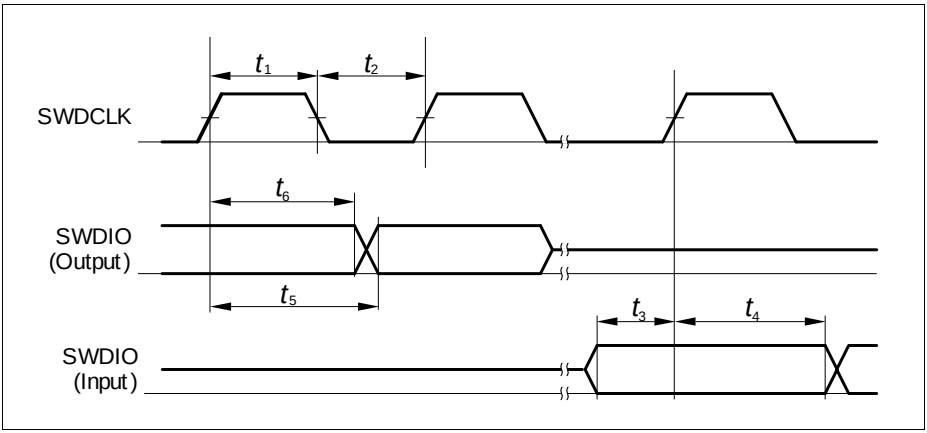

Figure 14 SWD Timing

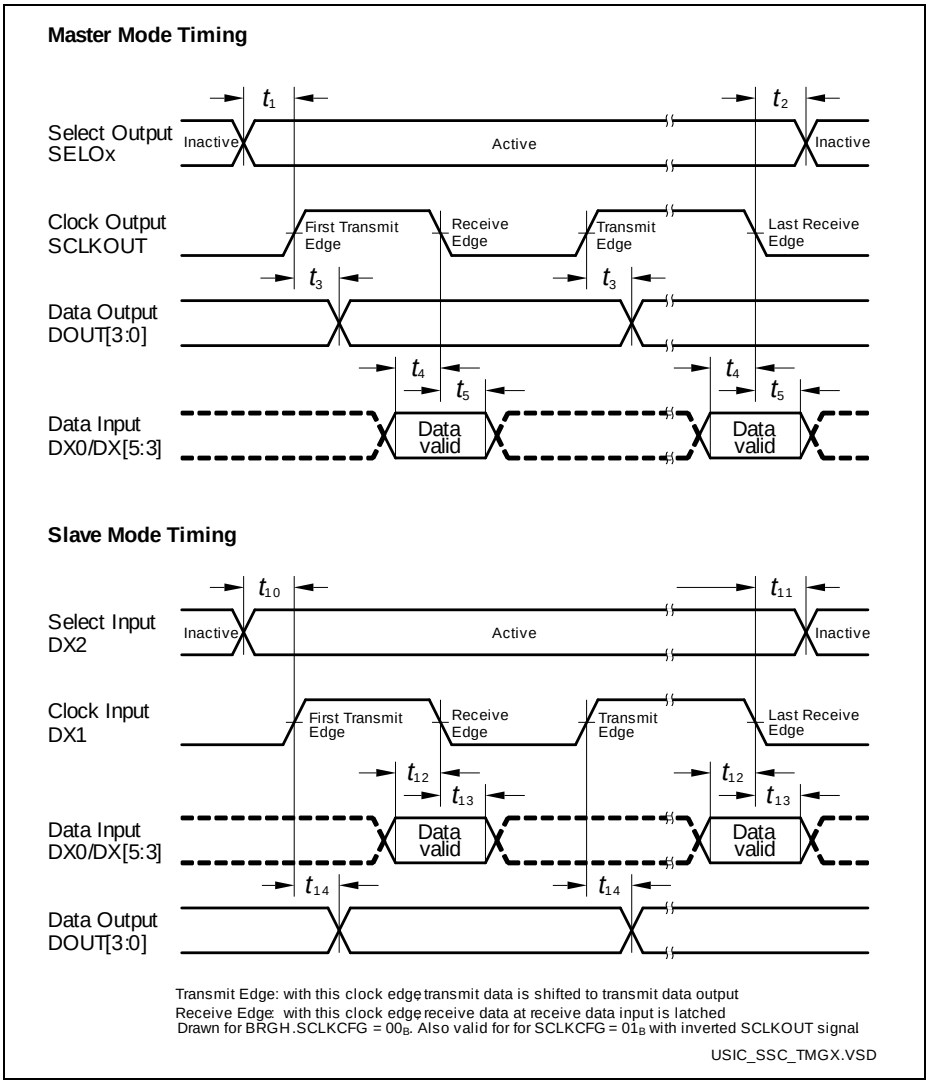

Figure 15 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3.3.7.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 25 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

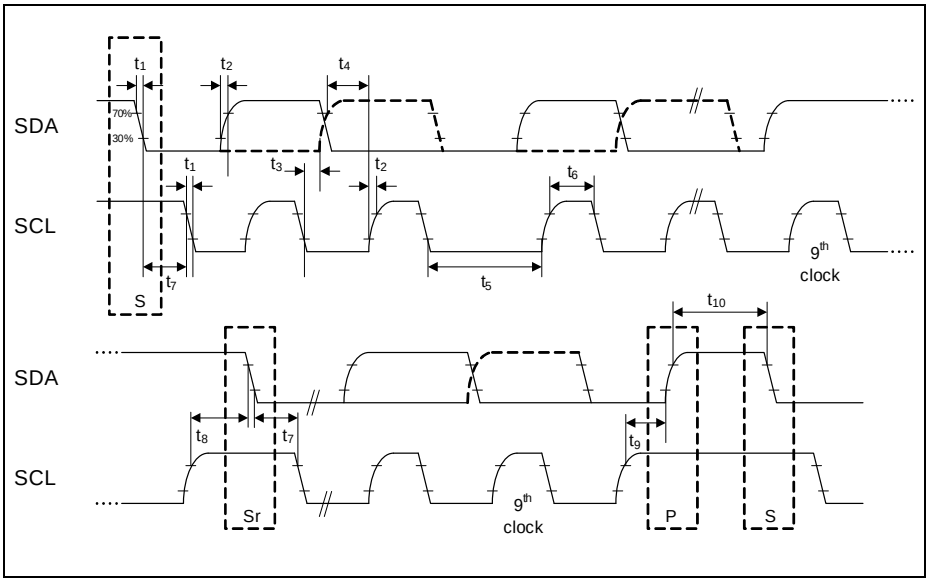

Figure 16 USIC IIC Stand and Fast Mode Timing

3.3.7.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 27 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$2/f_{MCLK}$	-	-	ns	$V_{DDP} \geq 3$ V
		$4/f_{MCLK}$	-	-	ns	$V_{DDP} < 3$ V
Clock HIGH	t_2 CC	0.35 x t_{1min}	-	-	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	0.15 x t_{1min}	ns	

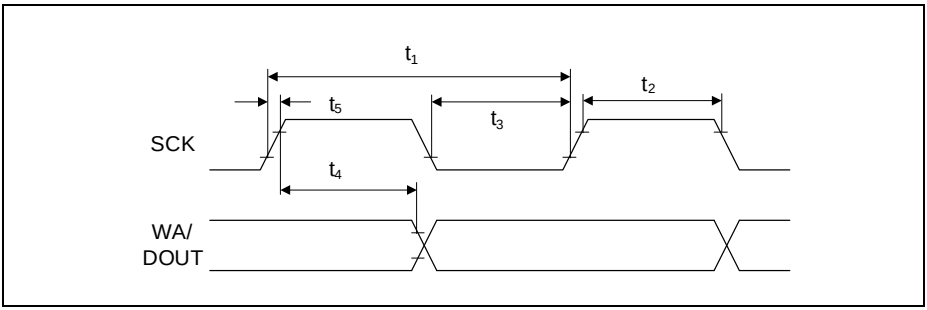

Figure 17 USIC IIS Master Transmitter Timing

Table 28 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	-	-	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	-	-	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

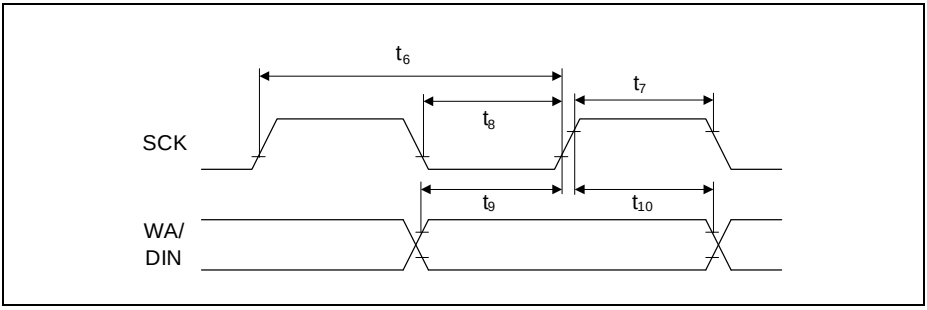

Figure 18 USIC IIS Slave Receiver Timing

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers