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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100t038f0032aaxuma1

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Summary of Features

- High code density with 32-bit performance
- Single cycle 32-bit hardware multiplier
- System timer (SysTick) for Operating System support
- Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 64 kbytes on-chip Flash program and data memory

On-Chip Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- A/D Converters, up to 12 channels, includes a 12-bit analog to digital converter
- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times
- Temperature Sensor (TSE)

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC1<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set

Summary of Features
Table 1 Synopsis of XMC1100 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1100-Q040F0032	PG-VQFN-40-13	32	16
XMC1100-Q040F0064	PG-VQFN-40-13	64	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC1100 Device Types¹⁾

Derivative	ADC channel
XMC1100-T016	6
XMC1100-T038	12
XMC1100-Q024	8
XMC1100-Q040	12

1) Features that are not included in this table are available in all the derivatives

Table 3 ADC Channels

Package	VADC0 G0	VADC0 G1
PG-TSSOP-16	CH0..CH5	–
PG-TSSOP-38	CH0..CH7	CH1, CH5 .. CH7
PG-VQFN-24	CH0..CH7	–
PG-VQFN-40	CH0..CH7	CH1, CH5 .. CH7

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 0F00_H (MSB) - 1000 0F1B_H (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 4 XMC1100 Chip Identification Number

Derivative	Value	Marking
XMC1100-T016F0008	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00003000 101ED083 _H	AA
XMC1100-T016F0016	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083 _H	AA
XMC1100-T016F0032	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083 _H	AA
XMC1100-T016F0064	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-T016X0064	00011033 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-T038F0016	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083 _H	AA
XMC1100-T038F0032	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083 _H	AA
XMC1100-T038F0064	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-T038X0064	00011013 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-Q024F0008	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00003000 101ED083 _H	AA
XMC1100-Q024F0016	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083 _H	AA
XMC1100-Q024F0032	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083 _H	AA
XMC1100-Q024F0064	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-Q040F0016	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083 _H	AA
XMC1100-Q040F0032	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083 _H	AA
XMC1100-Q040F0064	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA

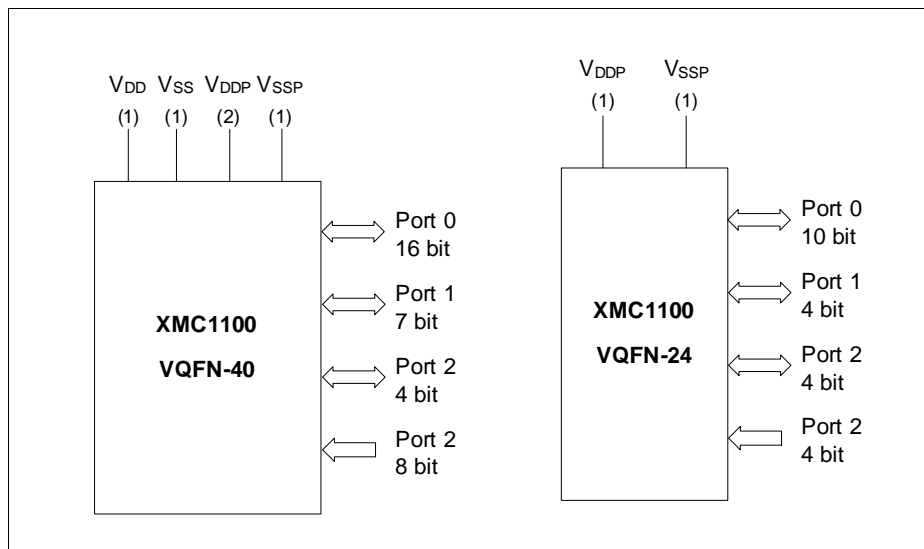


Figure 3 XMC1100 Logic Symbol for VQFN-24 and VQFN-40

Table 8 Port I/O Functions

Function	Outputs									Inputs								
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0. PDOU0		ERU0. GOUT0	CCU40.OUT0		USIC0_CH0. SELO0	USIC0_CH1. SELO0					CCU40.IN0C				USIC0_CH0. DX2A	USIC0_CH1. DX2A	
P0.1	ERU0. PDOU1		ERU0. GOUT1	CCU40.OUT1			SCU_VDROP					CCU40.IN1C						
P0.2	ERU0. PDOU2		ERU0. GOUT2	CCU40.OUT2		VADC0. EMUX02						CCU40.IN2C						
P0.3	ERU0. PDOU3		ERU0. GOUT3	CCU40.OUT3		VADC0. EMUX01						CCU40.IN3C						
P0.4				CCU40.OUT1		VADC0. EMUX00	WWDT. SERVICE_OU T											
P0.5				CCU40.OUT0														
P0.6				CCU40.OUT0		USIC0_CH1. MCLKOUT	USIC0_CH1. DOUT0					CCU40.IN0B				USIC0_CH1. DX0C		
P0.7				CCU40.OUT1		USIC0_CH0. SCLKOUT	USIC0_CH1. DOUT0					CCU40.IN1B				USIC0_CH1. DX1C	USIC0_CH1. DX0D	USIC0_CH1. DX1C
P0.8				CCU40.OUT2		USIC0_CH0. SCLKOUT	USIC0_CH1. SCLKOUT					CCU40.IN2B				USIC0_CH0. DX1B	USIC0_CH1. DX1B	
P0.9				CCU40.OUT3		USIC0_CH0. SELO0	USIC0_CH1. SELO0					CCU40.IN3B				USIC0_CH0. DX2B	USIC0_CH1. DX2B	
P0.10						USIC0_CH0. SELO1	USIC0_CH1. SELO1									USIC0_CH0. DX2C	USIC0_CH1. DX2C	
P0.11				USIC0_CH0. MCLKOUT		USIC0_CH0. SELO2	USIC0_CH1. SELO2									USIC0_CH0. DX2D	USIC0_CH1. DX2D	
P0.12						USIC0_CH0. SELO3						CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0. DX2E		
P0.13	WWDT. SERVICE_OU T					USIC0_CH0. SELO4										USIC0_CH0. DX2F		
P0.14						USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT									USIC0_CH0. DX0A	USIC0_CH0. DX1A	
P0.15						USIC0_CH0. DOUT0	USIC0_CH1. MCLKOUT									USIC0_CH0. DX0B		
P1.0		CCU40.OUT0					USIC0_CH0. DOUT0		USIC0_CH0. DOUT0		USIC0_CH0. HWIN0					USIC0_CH0. DX0C		
P1.1	VADC0. EMUX00	CCU40.OUT1				USIC0_CH0. DOUT0	USIC0_CH1. SELO0		USIC0_CH0. DOUT1		USIC0_CH0. HWIN1					USIC0_CH0. DX0D	USIC0_CH0. DX1D	USIC0_CH1. DX2E
P1.2	VADC0. EMUX01	CCU40.OUT2					USIC0_CH1. DOUT0		USIC0_CH0. DOUT2		USIC0_CH0. HWIN2					USIC0_CH1. DX0B		
P1.3	VADC0. EMUX02	CCU40.OUT3				USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT3		USIC0_CH0. HWIN3					USIC0_CH1. DX0A	USIC0_CH1. DX1A	
P1.4	VADC0. EMUX10	USIC0_CH1. SCLKOUT				USIC0_CH0. SELO0	USIC0_CH1. SELO1									USIC0_CH0. DX5E	USIC0_CH1. DX5E	
P1.5	VADC0. EMUX11	USIC0_CH0. DOUT0				USIC0_CH0. SELO1	USIC0_CH1. SELO2									USIC0_CH1. DX5F		

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1100.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1100 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**
Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1100 and must be regarded for a system design.
- **SR**
Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1100 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Cond ition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_S	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on any pin with respect to V_{SSP}	V_{IN}	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	whichever is lower
Voltage on any analog input pin with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	–
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma I_{IN} $	SR	–	–	50	mA	–
Analog comparator input voltage	V_{CM}	SR	-0.3	–	$V_{DDP} + 0.3$	V	

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 11 provides the characteristics of the input/output pins of the XMC1100.

Table 11 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	$I_{OL} = 11 \text{ mA}$ (5 V) $I_{OL} = 7 \text{ mA}$ (3.3 V)
			–	0.4	V	$I_{OL} = 5 \text{ mA}$ (5 V) $I_{OL} = 3.5 \text{ mA}$ (3.3 V)
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	$I_{OL} = 50 \text{ mA}$ (5 V) $I_{OL} = 25 \text{ mA}$ (3.3 V)
			–	0.32	V	$I_{OL} = 10 \text{ mA}$ (5 V)
			–	0.4	V	$I_{OL} = 5 \text{ mA}$ (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	$V_{DDP} - 1.0$	–	V	$I_{OH} = -10 \text{ mA}$ (5 V) $I_{OH} = -7 \text{ mA}$ (3.3 V)
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4.5 \text{ mA}$ (5 V) $I_{OH} = -2.5 \text{ mA}$ (3.3 V)
Output high voltage on high current pads	V_{OHP1}	CC	$V_{DDP} - 0.32$	–	V	$I_{OH} = -6 \text{ mA}$ (5 V)
			$V_{DDP} - 1.0$	–	V	$I_{OH} = -8 \text{ mA}$ (3.3 V)
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -4 \text{ mA}$ (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	$0.19 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	–	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ³⁾

Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (TSSOP28/16, VQFN24)	I_{MVDD1}	SR	–	130	mA	³⁾
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	³⁾
Maximum current out of V_{SS} (TSSOP28/16, VQFN24)	I_{MVSS1}	SR	–	130	mA	³⁾
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	³⁾

- 1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 2) An additional error current (I_{INL}) will flow if an overload current flows through an adjacent pin.
- 3) Not subject to production test, verified by design/characterization.
- 4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Analog to Digital Converters (ADC)

Table 12 shows the Analog to Digital Converter (ADC) characteristics.

Table 12 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	1.8	–	3.0	V	SHSCFG.AREF = 11 _B
		3.0	–	5.5	V	SHSCFG.AREF = 10 _B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00 _B
Analog input voltage range	V_{AIN} SR	$V_{SSP} - 0.05$	–	$V_{DDP} + 0.05$	V	
Auxiliary analog reference ground (SH0-CH0, SH1-CH0)	V_{REFGND} SR	$V_{SSP} - 0.05$	–	$V_{DDP} + 0.05$	V	
Internal reference voltage (full scale value)	V_{REFINT} CC	4.82	5	5.18	V	-40°C - 105°C
		4.9	5	5.1	V	0°C - 85°C ¹⁾
Switched capacitance of an analog input ¹⁾	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00 _B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01 _B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10 _B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11 _B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	¹⁾
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	¹⁾

Electrical Parameter
Table 12 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC	1			–	GNCTRxz.GAINy = 00 _B (unity gain)
		3			–	GNCTRxz.GAINy = 01 _B (gain g1)
		6			–	GNCTRxz.GAINy = 10 _B (gain g2)
		12			–	GNCTRxz.GAINy = 11 _B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	$V_{DDP} = 5.0$ V
		3	–	–	1 / f_{ADC}	$V_{DDP} = 3.3$ V
		30	–	–	1 / f_{ADC}	$V_{DDP} = 1.8$ V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	μs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC	9			1 / f_{ADC}	2)
Conversion time in 12-bit mode	t_{C12} CC	20			1 / f_{ADC}	2)
Maximum sample rate in 12-bit mode ³⁾	f_{C12} CC	–	–	$f_{ADC} / 42.5$	–	1 sample pending
		–	–	$f_{ADC} / 62.5$	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC	18			1 / f_{ADC}	2)
Maximum sample rate in 10-bit mode ³⁾	f_{C10} CC	–	–	$f_{ADC} / 40.5$	–	1 sample pending
		–	–	$f_{ADC} / 58.5$	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC	16			1 / f_{ADC}	2)

3.2.3 Temperature Sensor Characteristics

Table 13 Temperature Sensor Characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy ²⁾	T_{TSAL} CC	–	+/-20	–	°C	$T_J = -40\text{ °C}$ (calibrated)
		–	+/-12	–	°C	$T_J = -25\text{ °C}$ (calibrated)
		-5	–	5	°C	$T_J = 0\text{ °C}$
		-2	–	2	°C	$T_J = 25\text{ °C}$ (calibrated)
		-4	–	4	°C	$T_J = 70\text{ °C}$
		-2	–	2	°C	$T_J = 115\text{ °C}$ (calibrated)

1) Not subject to production test, verified by design/characterization.

2) The temperature sensor accuracy is independent of the supply voltage.

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 21 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	—	500000	ns	—
SWDCLK low time	t_2 SR	50	—	500000	ns	—
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	—	—	ns	—
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	—	—	ns	—
SWDIO output valid time after SWDCLK rising edge	t_5 CC	—	—	68	ns	$C_L = 50$ pF
		—	—	62	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	—	—	ns	

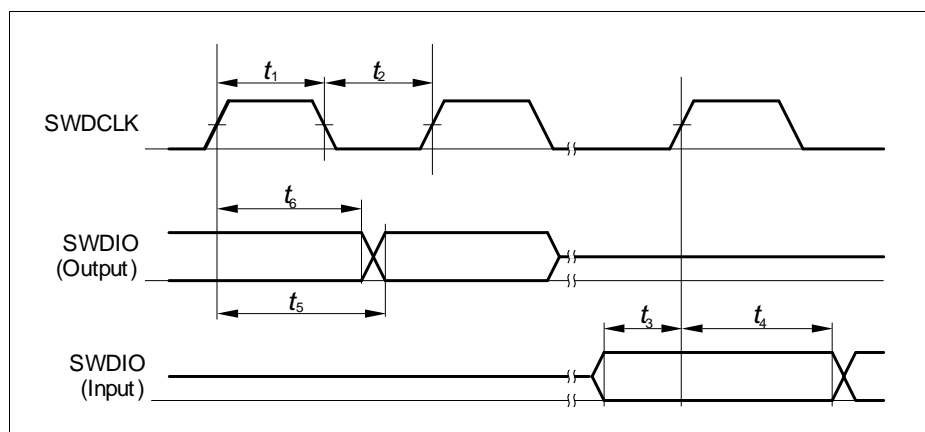


Figure 14 SWD Timing

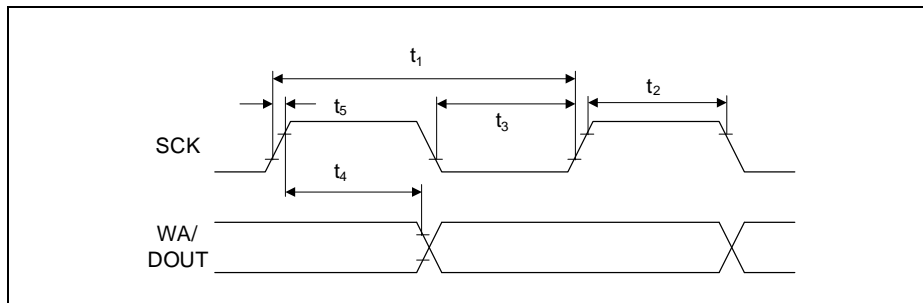


Figure 17 USIC IIS Master Transmitter Timing

Table 28 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	$0.35 \times t_{6min}$	-	-	ns	
Clock Low	t_8 SR	$0.35 \times t_{6min}$	-	-	ns	
Set-up time	t_9 SR	$0.2 \times t_{6min}$	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

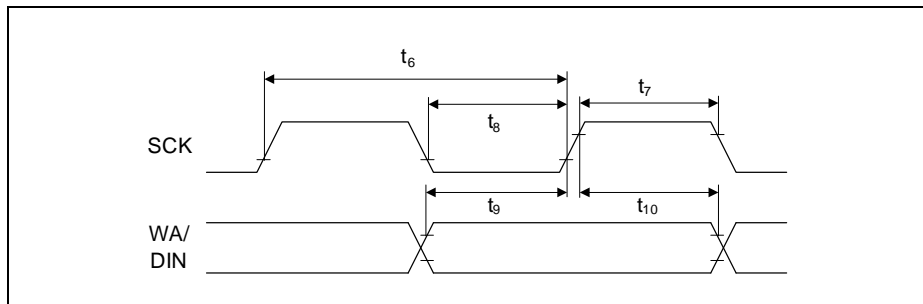


Figure 18 USIC IIS Slave Receiver Timing

4 Package and Reliability

The XMC1100 is a member of the XMC1000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 29 provides the thermal characteristics of the packages used in XMC1100.

Table 29 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8 ¹⁾
		-	70.3	K/W	PG-TSSOP-38-9 ¹⁾
		-	46.0	K/W	PG-VQFN-24-19 ¹⁾
		-	38.4	K/W	PG-VQFN-40-13 ¹⁾

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP} , independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1100 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$ ” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$$P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}} \text{ (switching current and leakage current).}$$

The static external power consumption caused by the output drivers is defined as

$$P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}} - V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

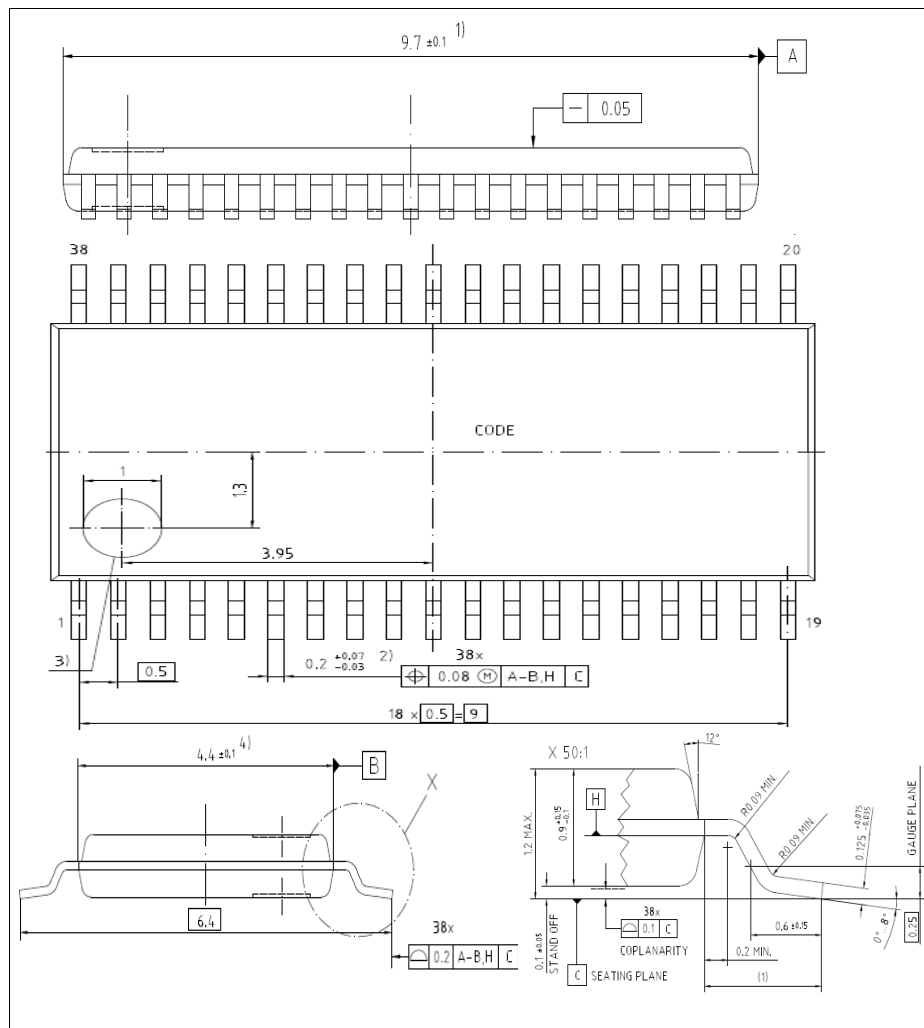


Figure 19 PG-TSSOP-38-9

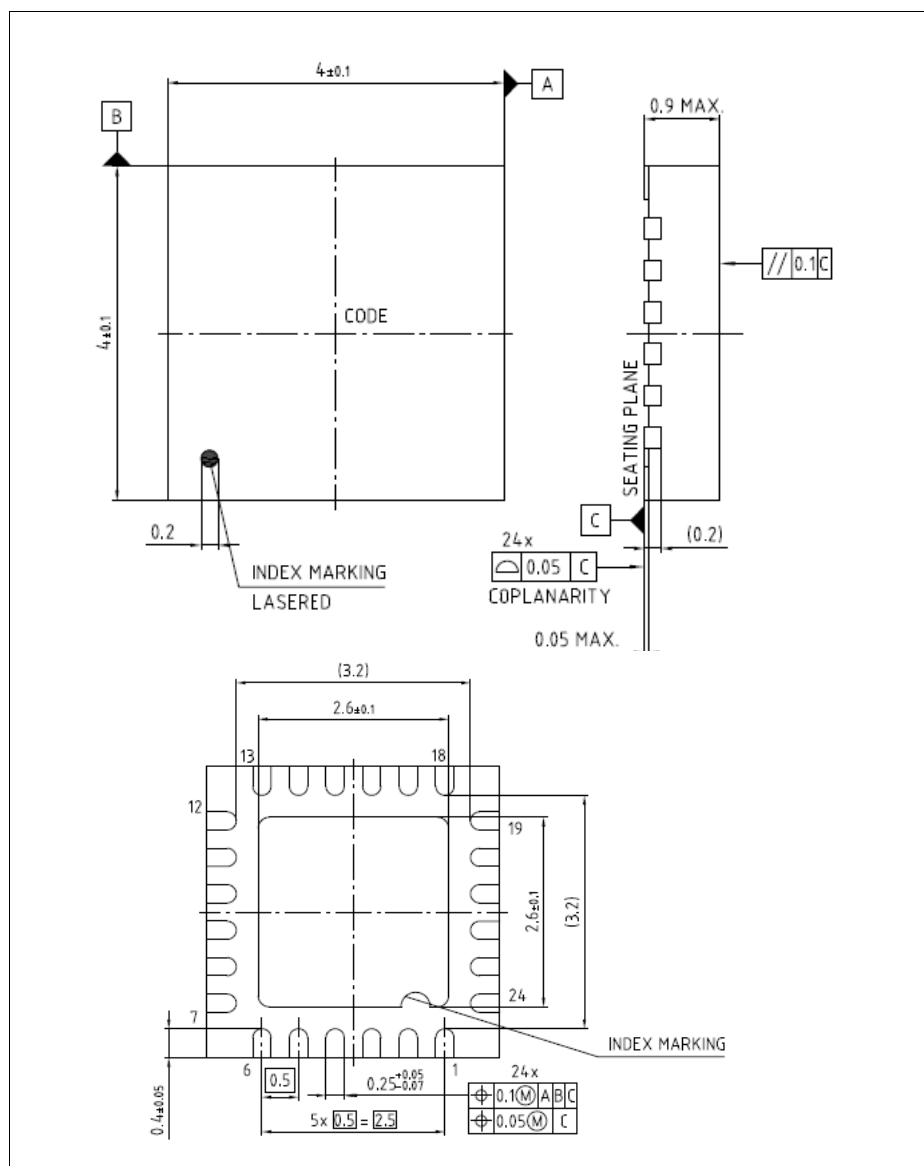


Figure 21 PG-VQFN-24-19