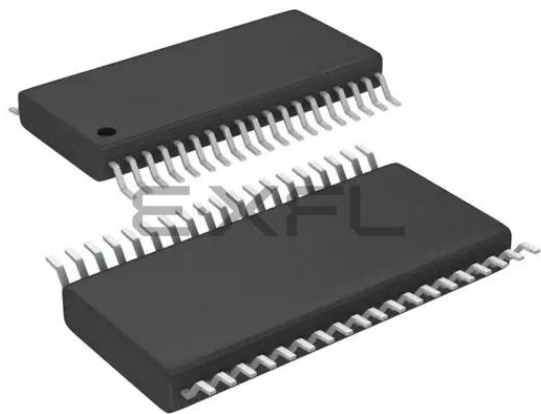




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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100t038f0064aaxuma1

XMC1100

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM[®] Cortex[™]-M0
32-bit processor core

Data Sheet

V1.4 2014-05

Microcontrollers

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1 Summary of Features

The XMC1100 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1100 series devices are designed for general purpose applications.

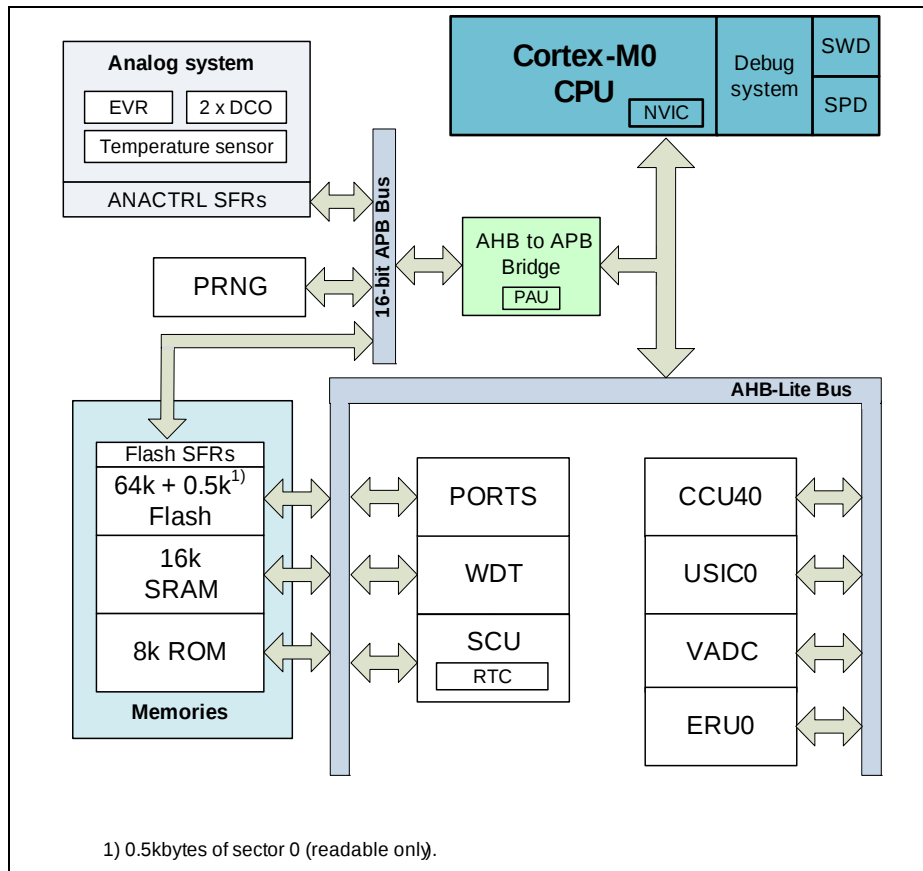


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
 - High Performance 32-bit ARM Cortex-M0 CPU
 - Most of 16-bit Thumb instruction set
 - Subset of 32-bit Thumb2 instruction set

Table 4 XMC1100 Chip Identification Number

Derivative	Value	Marking
XMC1100-T016F0008	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00003000 101ED083 _H	AA
XMC1100-T016F0016	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083 _H	AA
XMC1100-T016F0032	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083 _H	AA
XMC1100-T016F0064	00011032 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-T016X0064	00011033 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-T038F0016	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083 _H	AA
XMC1100-T038F0032	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083 _H	AA
XMC1100-T038F0064	00011012 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-T038X0064	00011013 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-Q024F0008	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00003000 101ED083 _H	AA
XMC1100-Q024F0016	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083 _H	AA
XMC1100-Q024F0032	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083 _H	AA
XMC1100-Q024F0064	00011062 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA
XMC1100-Q040F0016	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00005000 101ED083 _H	AA
XMC1100-Q040F0032	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00009000 101ED083 _H	AA
XMC1100-Q040F0064	00011042 01CF00FF 00001F37 00000000 00000B00 00001000 00011000 101ED083 _H	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

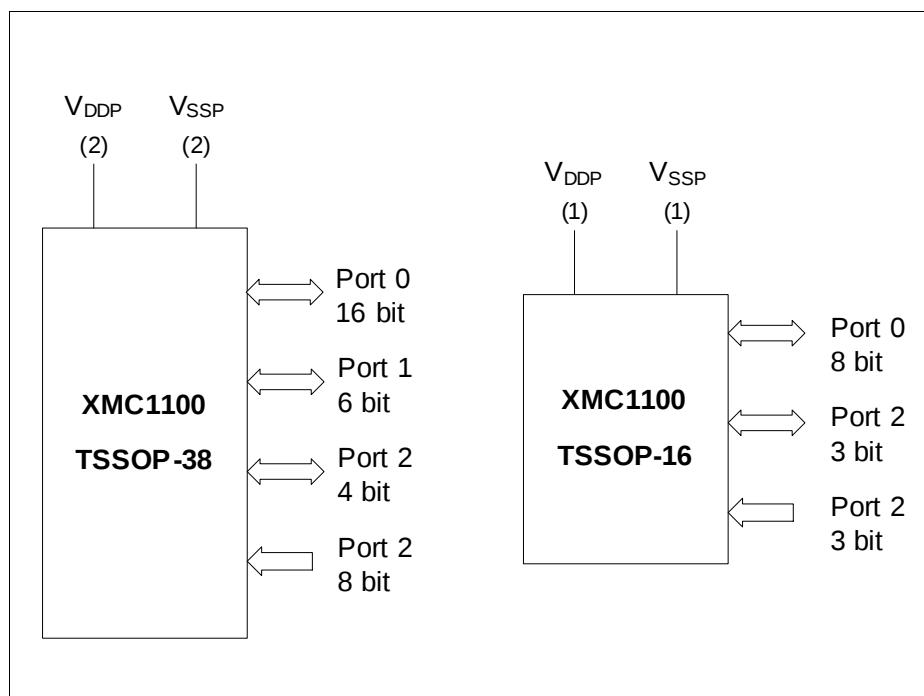


Figure 2 XMC1100 Logic Symbol for TSSOP-38 and TSSOP-16

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the "Function" column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The "Pad Type" indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	15	7	STD_INOUT	
P0.1	24	18	-	-	STD_INOUT	
P0.2	25	19	-	-	STD_INOUT	
P0.3	26	20	-	-	STD_INOUT	
P0.4	27	21	-	-	STD_INOUT	
P0.5	28	22	16	8	STD_INOUT	
P0.6	29	23	17	9	STD_INOUT	
P0.7	30	24	18	10	STD_INOUT	
P0.8	33	27	19	11	STD_INOUT	
P0.9	34	28	20	12	STD_INOUT	
P0.10	35	29	-	-	STD_INOUT	
P0.11	36	30	-	-	STD_INOUT	
P0.12	37	31	21	-	STD_INOUT	

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOC.R.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 8 Port I/O Functions

Function	Outputs									Inputs								
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0. PDOU0		ERU0. GOUT0	CCU40.OUT0		USIC0_CH0. SELO0	USIC0_CH1. SELO0					CCU40.IN0C				USIC0_CH0. DX2A	USIC0_CH1. DX2A	
P0.1	ERU0. PDOU1		ERU0. GOUT1	CCU40.OUT1			SCU_VDROP					CCU40.IN1C						
P0.2	ERU0. PDOU2		ERU0. GOUT2	CCU40.OUT2		VADC0. EMUX02						CCU40.IN2C						
P0.3	ERU0. PDOU3		ERU0. GOUT3	CCU40.OUT3		VADC0. EMUX01						CCU40.IN3C						
P0.4				CCU40.OUT1		VADC0. EMUX00	WWDT. SERVICE_OU T											
P0.5				CCU40.OUT0														
P0.6				CCU40.OUT0		USIC0_CH1. MCLKOUT	USIC0_CH1. DOUT0					CCU40.IN0B				USIC0_CH1. DX0C		
P0.7				CCU40.OUT1		USIC0_CH0. SCLKOUT	USIC0_CH1. DOUT0					CCU40.IN1B				USIC0_CH0. DX1C	USIC0_CH1. DX0D	USIC0_CH1. DX1C
P0.8				CCU40.OUT2		USIC0_CH0. SCLKOUT	USIC0_CH1. SCLKOUT					CCU40.IN2B				USIC0_CH0. DX1B	USIC0_CH1. DX1B	
P0.9				CCU40.OUT3		USIC0_CH0. SELO0	USIC0_CH1. SELO0					CCU40.IN3B				USIC0_CH0. DX2B	USIC0_CH1. DX2B	
P0.10						USIC0_CH0. SELO1	USIC0_CH1. SELO1									USIC0_CH0. DX2C	USIC0_CH1. DX2C	
P0.11				USIC0_CH0. MCLKOUT		USIC0_CH0. SELO2	USIC0_CH1. SELO2									USIC0_CH0. DX2D	USIC0_CH1. DX2D	
P0.12						USIC0_CH0. SELO3						CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0. DX2E		
P0.13	WWDT. SERVICE_OU T					USIC0_CH0. SELO4										USIC0_CH0. DX2F		
P0.14						USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT									USIC0_CH0. DX0A	USIC0_CH0. DX1A	
P0.15						USIC0_CH0. DOUT0	USIC0_CH1. MCLKOUT									USIC0_CH0. DX0B		
P1.0		CCU40.OUT0					USIC0_CH0. DOUT0		USIC0_CH0. DOUT0		USIC0_CH0. HWIN0					USIC0_CH0. DX0C		
P1.1	VADC0. EMUX00	CCU40.OUT1				USIC0_CH0. DOUT0	USIC0_CH1. SELO0		USIC0_CH0. DOUT1		USIC0_CH0. HWIN1					USIC0_CH0. DX0D	USIC0_CH0. DX1D	USIC0_CH1. DX2E
P1.2	VADC0. EMUX01	CCU40.OUT2					USIC0_CH1. DOUT0		USIC0_CH0. DOUT2		USIC0_CH0. HWIN2					USIC0_CH1. DX0B		
P1.3	VADC0. EMUX02	CCU40.OUT3				USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT3		USIC0_CH0. HWIN3					USIC0_CH1. DX0A	USIC0_CH1. DX1A	
P1.4	VADC0. EMUX10	USIC0_CH1. SCLKOUT				USIC0_CH0. SELO0	USIC0_CH1. SELO1									USIC0_CH0. DX5E	USIC0_CH1. DX5E	
P1.5	VADC0. EMUX11	USIC0_CH0. DOUT0				USIC0_CH0. SELO1	USIC0_CH1. SELO2									USIC0_CH1. DX5F		

Table 8 Port I/O Functions (cont'd)

Function	Outputs									Inputs							
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input
P1.6	VADC0. EMUX12	USIC0_CH1.D OUT0		USIC0_CH0.S CLKOUT		USIC0_CH0.S ELO2	USIC0_CH1.S ELO3							USIC0_CH0.D XSF			
P2.0	ERU0. PDOUT3	CCU40.OUT0	ERU0. GOUT3			USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT						VADC0. G0CH5		ERU0.0B0	USIC0_CH0. DX1E	USIC0_CH0. DX2F
P2.1	ERU0. PDOUT2	CCU40.OUT1	ERU0. GOUT2			USIC0_CH0. DOUT0	USIC0_CH1. SCLKOUT						VADC0. G0CH6		ERU0.1B0	USIC0_CH0. DX3A	USIC0_CH1. DX4A
P2.2													VADC0. G0CH7		ERU0.0B1 DX3A	USIC0_CH0. DX4A	USIC0_CH1. DX5A
P2.3													VADC0. G1CH5		ERU0.1B1	USIC0_CH0. DX5B	USIC0_CH1. DX3C
P2.4													VADC0. G1CH6		ERU0.0A1	USIC0_CH0. DX3B	USIC0_CH0. DX4B
P2.5													VADC0. G1CH7		ERU0.1A1	USIC0_CH0. DX5D	USIC0_CH1. DX3E
P2.6													VADC0. G0CH0		ERU0.2A1	USIC0_CH0. DX3E	USIC0_CH0. DX4E
P2.7													VADC0. G1CH1		ERU0.3A1	USIC0_CH0. DX5C	USIC0_CH1. DX3D
P2.8													VADC0. G0CH1	VADC0. G1CH0	ERU0.3B1	USIC0_CH0. DX3D	USIC0_CH0. DX4D
P2.9													VADC0. G0CH2	VADC0. G1CH4	ERU0.3B0	USIC0_CH0. DX5A	USIC0_CH1. DX3B
P2.10	ERU0. PDOUT1	CCU40.OUT2	ERU0. GOUT1				USIC0_CH1. DOUT0						VADC0. G0CH3	VADC0. G1CH2	ERU0.2B0	USIC0_CH0. DX3C	USIC0_CH0. DX4C
P2.11	ERU0. PDOUT0	CCU40.OUT3	ERU0. GOUT0			USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0						VADC0. G0CH4	VADC0. G1CH3	ERU0.2B1	USIC0_CH1. DX0E	USIC0_CH1. DX1E

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_S	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on any pin with respect to V_{SSP}	V_{IN}	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	whichever is lower
Voltage on any analog input pin with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	–
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma I_{IN} $	SR	–	–	50	mA	–
Analog comparator input voltage	V_{CM}	SR	-0.3	–	$V_{DDP} + 0.3$	V	

3.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1100. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 10 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage ¹⁾	V_{DDP} SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK} CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK} CC	–	–	66.4	MHz	Peripherals clock

1) See also the Supply Monitoring thresholds, [Chapter 3.3.3](#).

Electrical Parameter
Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	$0.85 \times V_{DDP}$	—	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ³⁾
Input Hysteresis ¹⁾	HYS	CC	$0.08 \times V_{DDP}$	—	V	CMOS Mode (5 V), Standard Hysteresis
			$0.03 \times V_{DDP}$	—	V	CMOS Mode (3.3 V), Standard Hysteresis
			$0.02 \times V_{DDP}$	—	V	CMOS Mode (2.2 V), Standard Hysteresis
			$0.5 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(5 V), Large Hysteresis
			$0.4 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(3.3 V), Large Hysteresis
			$0.2 \times V_{DDP}$	$0.65 \times V_{DDP}$	V	CMOS Mode(2.2 V), Large Hysteresis
Pull-up resistor on port pins	R_{PUP}	CC	20	50	kohm	$V_{IN} = V_{SSP}$
Pull-down resistor on port pins	R_{PDP}	CC	20	50	kohm	$V_{IN} = V_{DDP}$
Input leakage current ²⁾	I_{OZP}	CC	-1	1	μA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105^\circ\text{C}$
Overload current on any pin	I_{OVP}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma I_{OV} $	SR	—	25	mA	³⁾
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	—	0.3	V	⁴⁾
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	—
Maximum current per high current pins	I_{MP1A}	SR	-10	50	mA	—

Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (TSSOP28/16, VQFN24)	I_{MVDD1}	SR	–	130	mA	³⁾
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	³⁾
Maximum current out of V_{SS} (TSSOP28/16, VQFN24)	I_{MVSS1}	SR	–	130	mA	³⁾
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	³⁾

- 1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
- 3) Not subject to production test, verified by design/characterization.
- 4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Analog to Digital Converters (ADC)

Table 12 shows the Analog to Digital Converter (ADC) characteristics.

Table 12 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	1.8	–	3.0	V	SHSCFG.AREF = 11 _B
		3.0	–	5.5	V	SHSCFG.AREF = 10 _B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00 _B
Analog input voltage range	V_{AIN} SR	$V_{SSP} - 0.05$	–	$V_{DDP} + 0.05$	V	
Auxiliary analog reference ground (SH0-CH0, SH1-CH0)	V_{REFGND} SR	$V_{SSP} - 0.05$	–	$V_{DDP} + 0.05$	V	
Internal reference voltage (full scale value)	V_{REFINT} CC	4.82	5	5.18	V	-40°C - 105°C
		4.9	5	5.1	V	0°C - 85°C ¹⁾
Switched capacitance of an analog input ¹⁾	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00 _B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01 _B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10 _B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11 _B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	¹⁾
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	¹⁾

3.3 AC Parameters

3.3.1 Testing Waveforms

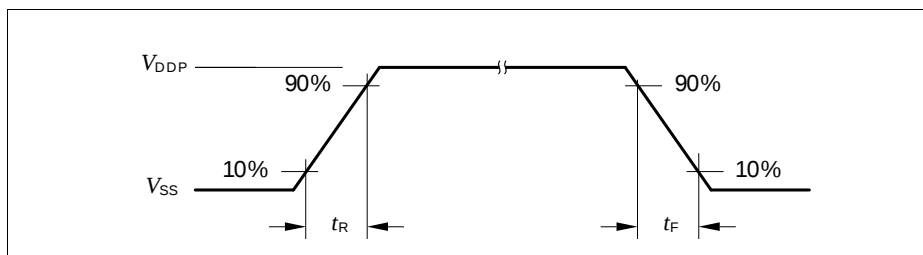


Figure 9 Rise/Fall Time Parameters

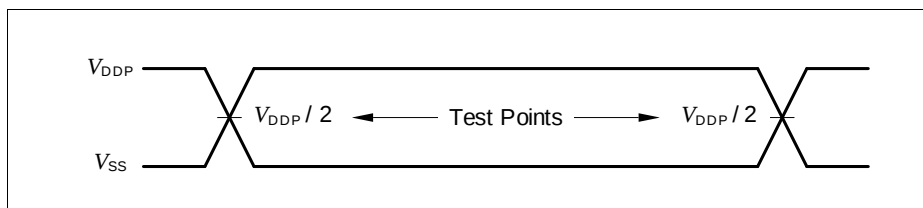


Figure 10 Testing Waveform, Output Delay

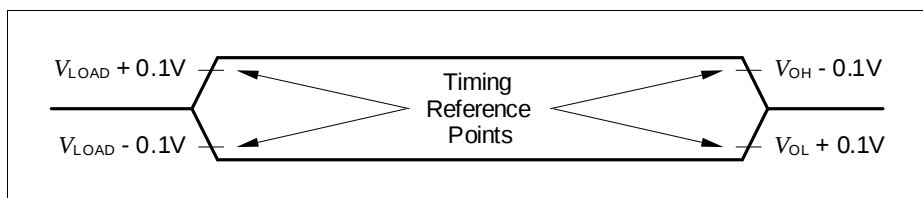


Figure 11 Testing Waveform, Output High Impedance

3.3.3 Power-Up and Supply Threshold Characteristics

Table 18 provides the characteristics of the supply threshold in XMC1100.

Table 18 Power-Up and Supply Threshold Parameters (Operating Conditions apply) ¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	$V_{DDP}/S_{VDDPrise}$	–	10^7	μs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/ μs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/ μs	Slope during fast transient within +/- 10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/ μs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$ ²⁾ SR	0	–	0.25	V/ μs	Slope during supply falling out of the +/-10% limits ³⁾
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00 _B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01 _B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10 _B
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
Start-up time from power-on reset	t_{SSW} SR	–	320	–	μs	Time to the first user code instruction ⁴⁾

1) Not all parameters are 100% tested, but are verified by design/characterisation.

2) A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 21 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	—	500000	ns	—
SWDCLK low time	t_2 SR	50	—	500000	ns	—
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	—	—	ns	—
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	—	—	ns	—
SWDIO output valid time after SWDCLK rising edge	t_5 CC	—	—	68	ns	$C_L = 50$ pF
		—	—	62	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	—	—	ns	

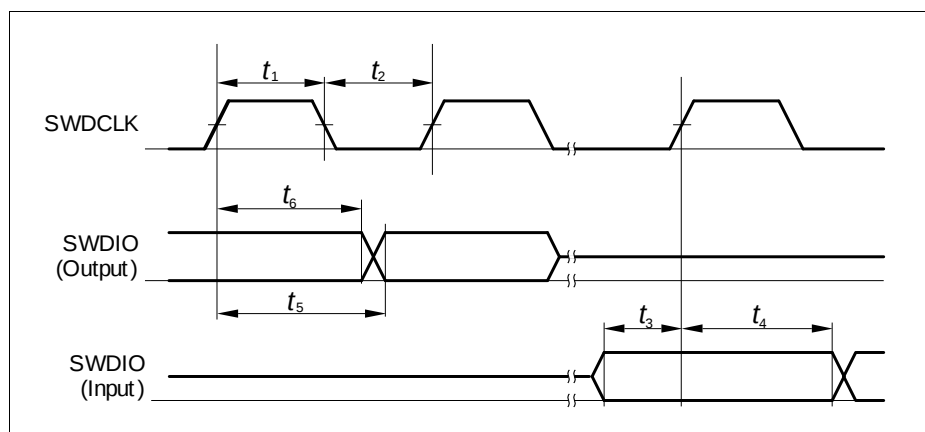


Figure 14 SWD Timing

3.3.6 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is $0.75 \mu s$. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles ($0.69 \mu s$).

Table 22 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time ¹⁾	Remark
8 MHz	4	1 to 5	6 to 12	$0.69 \mu s$	The other closest option ($0.81 \mu s$) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with $0.5 + (\text{max. number of } 0_B \text{ sample clocks})$

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is $\pm 5\%$
- Effective decision time is between $0.69 \mu s$ and $0.75 \mu s$ (calculated with nominal sample frequency)

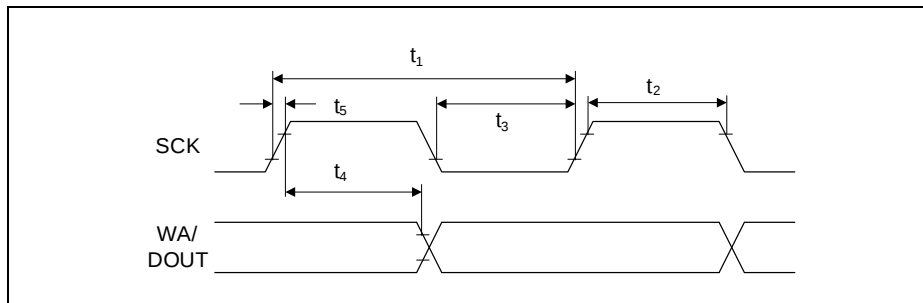


Figure 17 USIC IIS Master Transmitter Timing

Table 28 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	$0.35 \times t_{6min}$	-	-	ns	
Clock Low	t_8 SR	$0.35 \times t_{6min}$	-	-	ns	
Set-up time	t_9 SR	$0.2 \times t_{6min}$	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

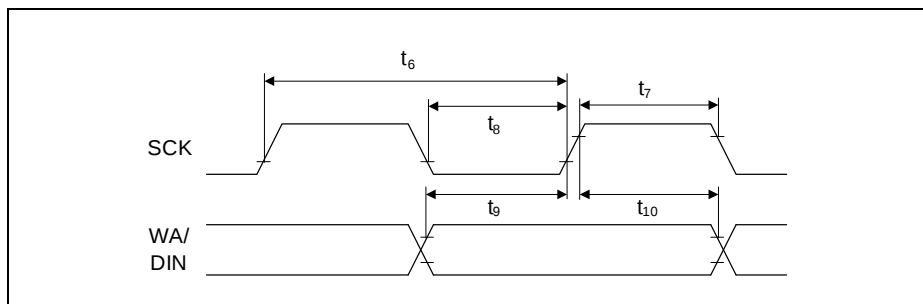


Figure 18 USIC IIS Slave Receiver Timing

4.2 Package Outlines

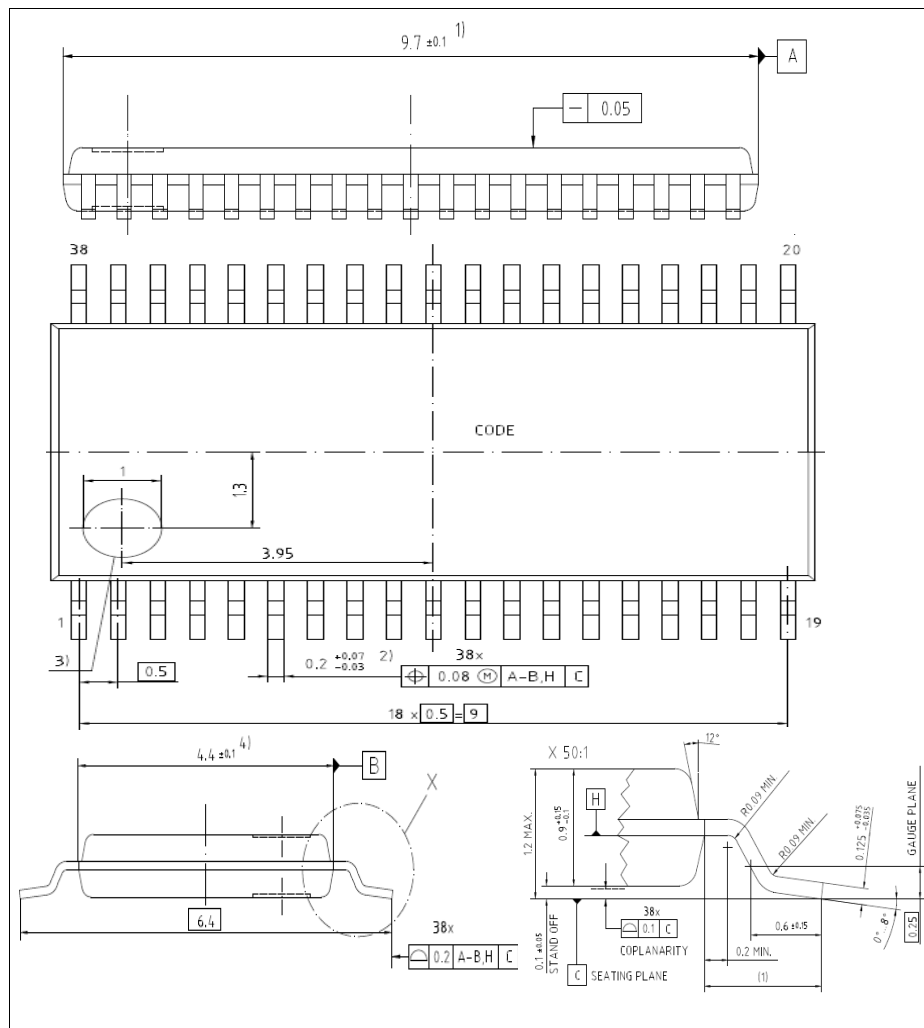


Figure 19 **PG-TSSOP-38-9**