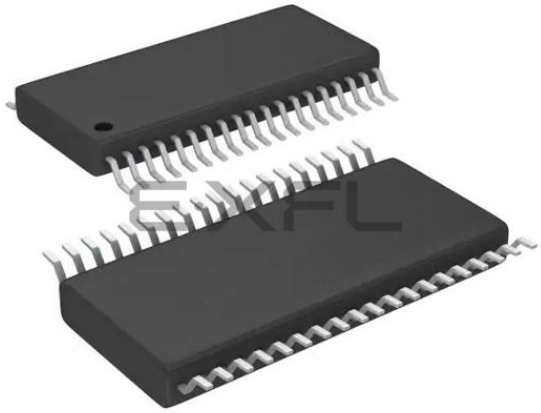
Infineon Technologies - XMC1100T038X0064AAXUMA1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1100t038x0064aaxuma1

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1100 series devices.

The document describes the characteristics of a superset of the XMC1100 series devices. For simplicity, the various device types are referred to by the collective term XMC1100 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

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1 Summary of Features

The XMC1100 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1100 series devices are designed for general purpose applications.

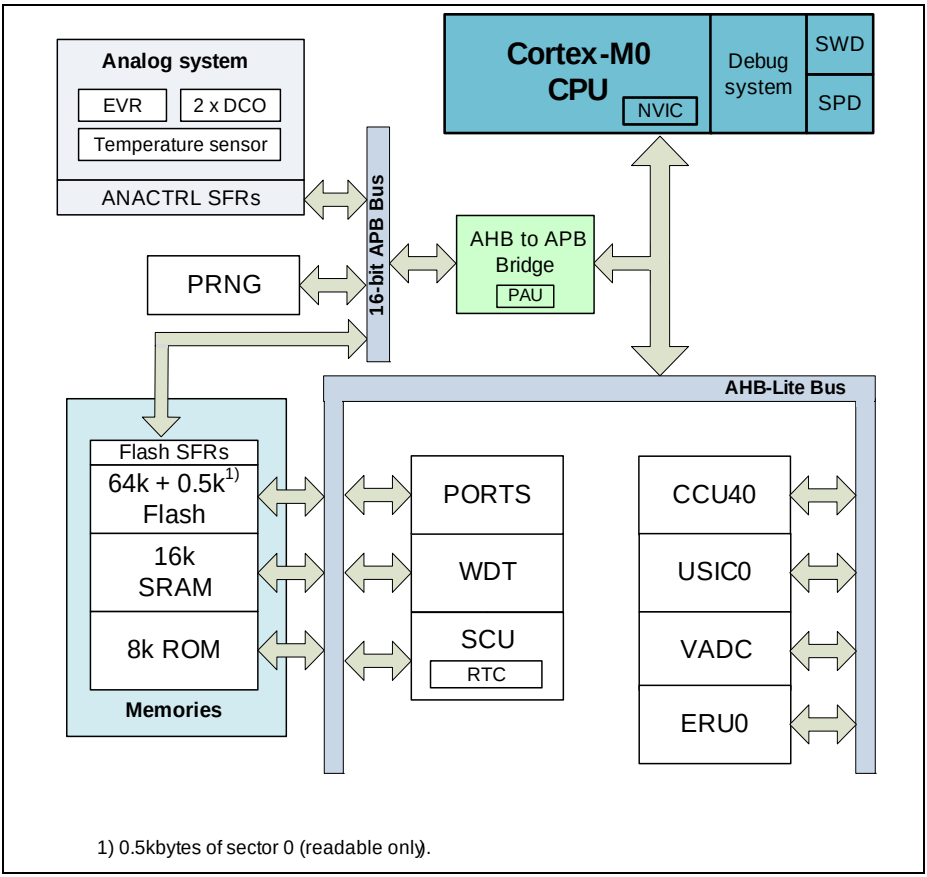

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M0 CPU
  - Most of 16-bit Thumb instruction set
  - Subset of 32-bit Thumb2 instruction set

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  - High code density with 32-bit performance
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support
  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 64 kbytes on-chip Flash program and data memory

On-Chip Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- A/D Converters, up to 12 channels, includes a 12-bit analog to digital converter
- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times
- Temperature Sensor (TSE)

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set

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- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1100 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1100 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1100** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XMC1100 Device Types

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1100-T016F0008	PG-TSSOP-16-8	8	16
XMC1100-T016F0016	PG-TSSOP-16-8	16	16
XMC1100-T016F0032	PG-TSSOP-16-8	32	16
XMC1100-T016F0064	PG-TSSOP-16-8	64	16
XMC1100-T016X0064	PG-TSSOP-16-8	64	16
XMC1100-T038F0016	PG-TSSOP-38-9	16	16
XMC1100-T038F0032	PG-TSSOP-38-9	32	16
XMC1100-T038F0064	PG-TSSOP-38-9	64	16
XMC1100-T038X0064	PG-TSSOP-38-9	64	16
XMC1100-Q024F0008	PG-VQFN-24-19	8	16
XMC1100-Q024F0016	PG-VQFN-24-19	16	16
XMC1100-Q024F0032	PG-VQFN-24-19	32	16
XMC1100-Q024F0064	PG-VQFN-24-19	64	16
XMC1100-Q040F0016	PG-VQFN-40-13	16	16

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Table 1 Synopsis of XMC1100 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1100-Q040F0032	PG-VQFN-40-13	32	16
XMC1100-Q040F0064	PG-VQFN-40-13	64	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC1100 Device Types[1)]

Derivative	ADC channel
XMC1100-T016	6
XMC1100-T038	12
XMC1100-Q024	8
XMC1100-Q040	12

1) Features that are not included in this table are available in all the derivatives

Table 3 ADC Channels

Package	VADC0 G0	VADC0 G1
PG-TSSOP-16	CH0..CH5	–
PG-TSSOP-38	CH0..CH7	CH1, CH5 .. CH7
PG-VQFN-24	CH0..CH7	–
PG-VQFN-40	CH0..CH7	CH1, CH5 .. CH7

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

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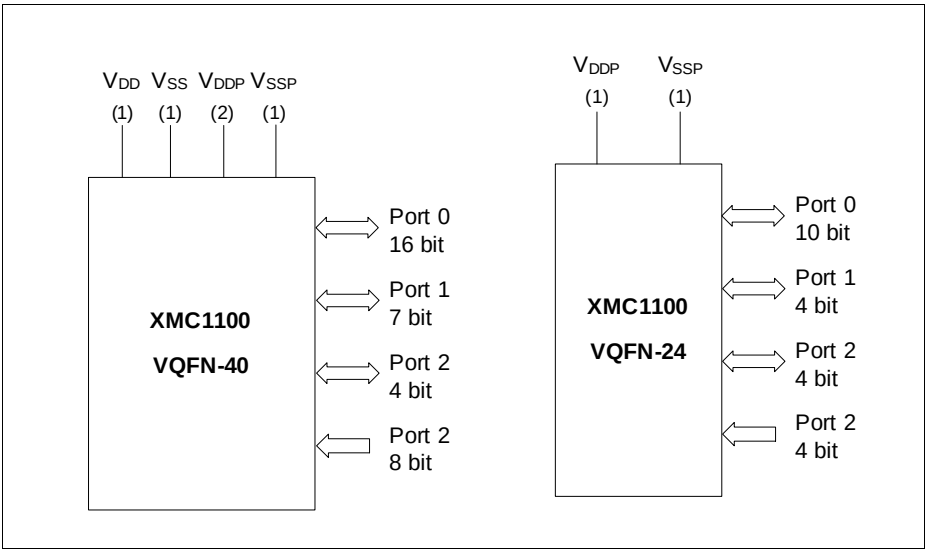

Figure 3 XMC1100 Logic Symbol for VQFN-24 and VQFN-40

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2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

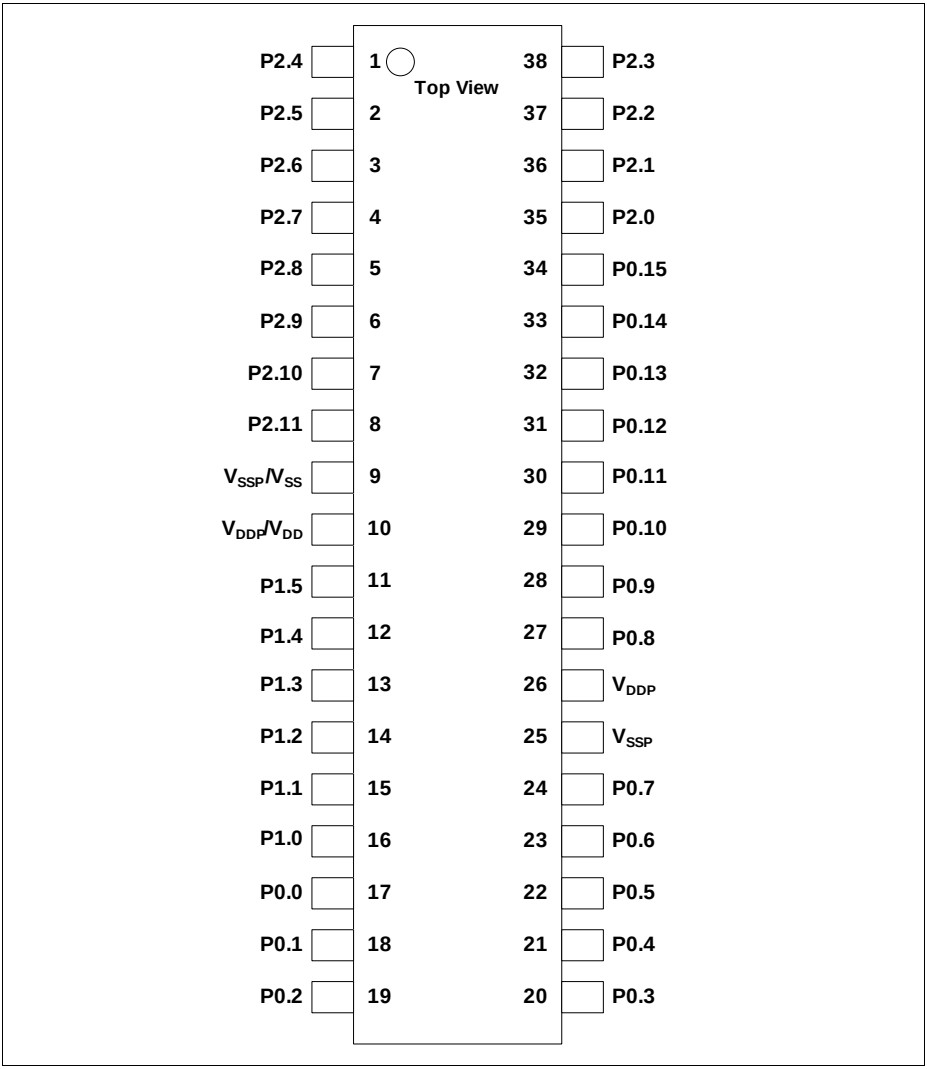

Figure 4 XMC1100 **PG-TSSOP-38 Pin Configuration** (top view)

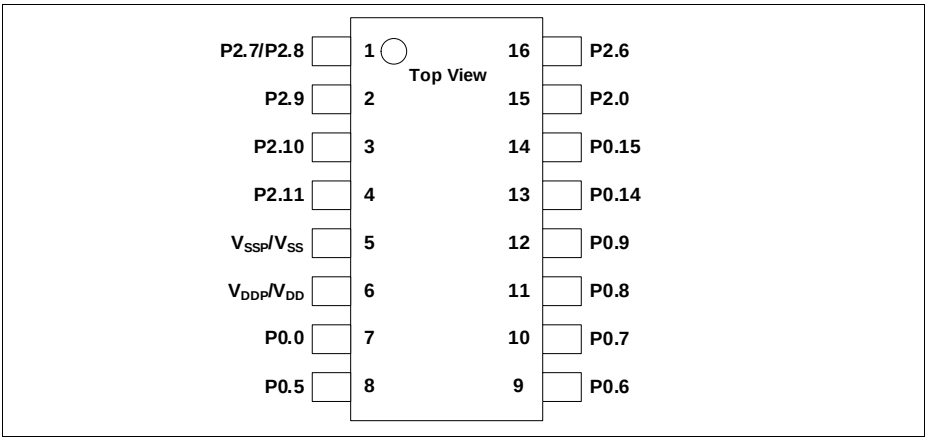

Figure 5 XMC1100 **PG-TSSOP-16 Pin Configuration** (top view)

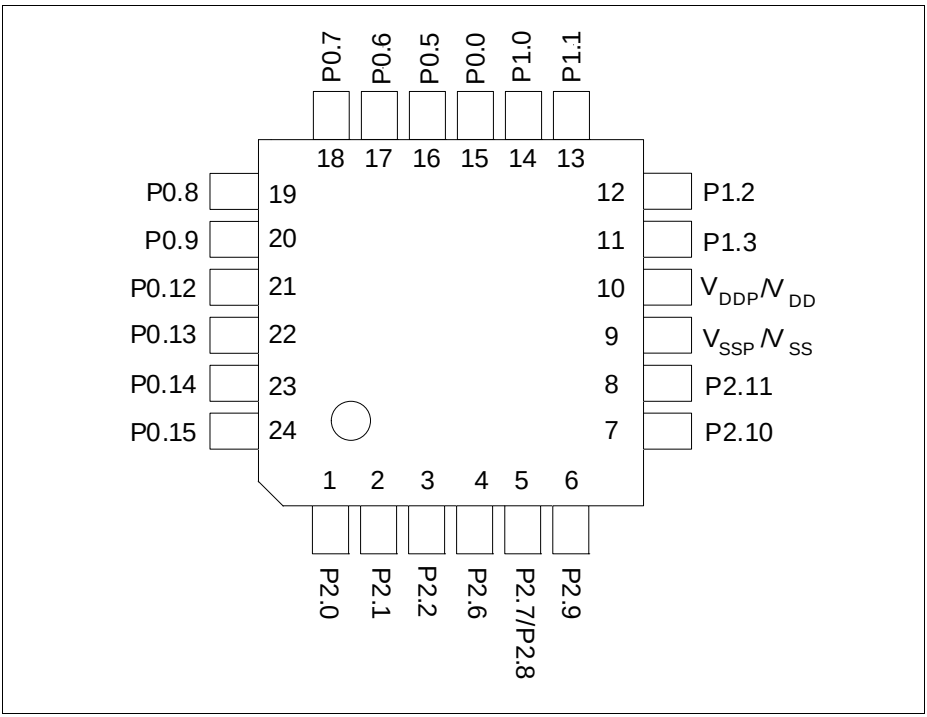

Figure 6 XMC1100 **PG-VQFN-24 Pin Configuration** (top view)

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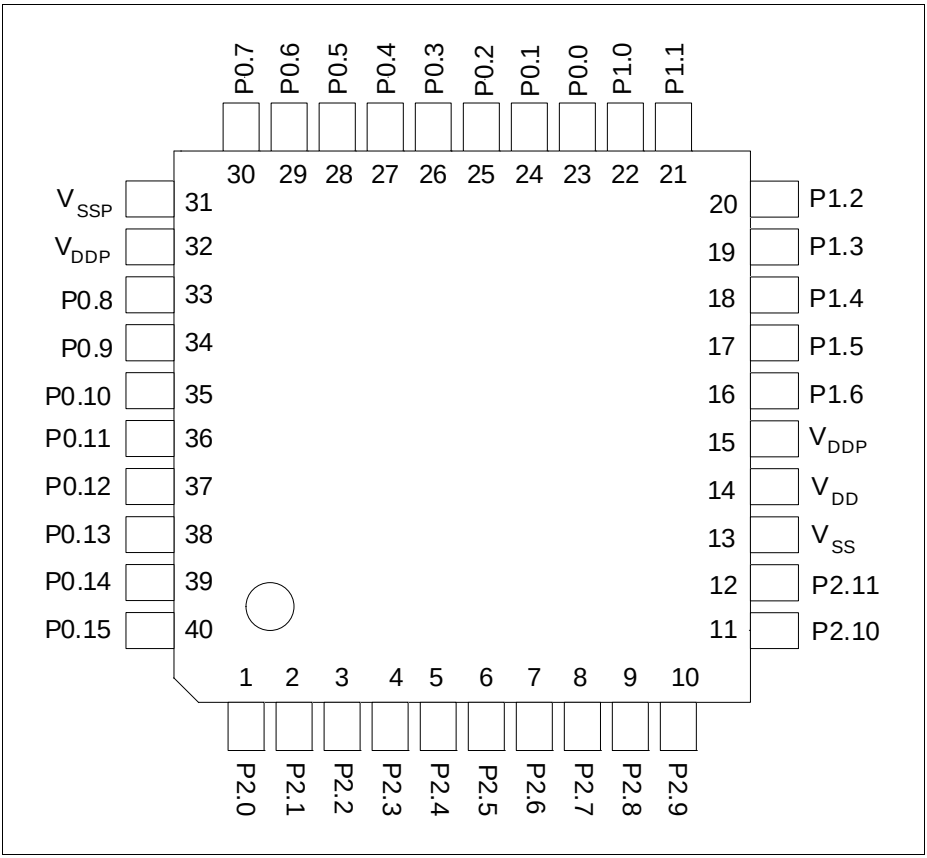

Figure 7 XMC1100 **PG-VQFN-40 Pin Configuration** (top view)

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	VQFN 24	TSSOP 16	Pad Type	Notes
P0.13	38	32	22	-	STD_INOUT	
P0.14	39	33	23	13	STD_INOUT	
P0.15	40	34	24	14	STD_INOUT	
P1.0	22	16	14	-	High Current	
P1.1	21	15	13	-	High Current	
P1.2	20	14	12	-	High Current	
P1.3	19	13	11	-	High Current	
P1.4	18	12	-	-	High Current	
P1.5	17	11	-	-	High Current	
P1.6	16	-	-	-	STD_INOUT	
P2.0	1	35	1	15	STD_INOUT/AN	
P2.1	2	36	2	-	STD_INOUT/AN	
P2.2	3	37	3	-	STD_IN/AN	
P2.3	4	38	-	-	STD_IN/AN	
P2.4	5	1	-	-	STD_IN/AN	
P2.5	6	2	-	-	STD_IN/AN	
P2.6	7	3	4	16	STD_IN/AN	
P2.7	8	4	5	1	STD_IN/AN	
P2.8	9	5	5	1	STD_IN/AN	
P2.9	10	6	6	2	STD_IN/AN	
P2.10	11	7	7	3	STD_INOUT/AN	
P2.11	12	8	8	4	STD_INOUT/AN	
VSS	13	9	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage. VDD has to be supplied with the same voltage as VDDP

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3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_S	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on any pin with respect to V_{SSP}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Voltage on any analog input pin with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	–
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	SR	–	–	50	mA	–
Analog comparator input voltage	V_{CM}	SR	-0.3	–	V_{DDP} + 0.3	V	

Table 11 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (TSSOP28/16, VQFN24)	I_{MVDD1}	SR	–	130	mA	3)
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	3)
Maximum current out of V_{SS} (TSSOP28/16, VQFN24)	I_{MVSS1}	SR	–	130	mA	3)
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	3)

1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

3) Not subject to production test, verified by design/characterization.

4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

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3.2.2 Analog to Digital Converters (ADC)

Table 12 shows the Analog to Digital Converter (ADC) characteristics.

Table 12 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	1.8	–	3.0	V	SHSCFG.AREF = 11_B
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground (SH0-CH0, SH1-CH0)	V_{REFGND} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Internal reference voltage (full scale value)	V_{REFINT} CC	4.82	5	5.18	V	-40°C - 105°C
		4.9	5	5.1	V	0°C - 85°C [1]
Switched capacitance of an analog input[1]	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	[1]
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	[1]

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3.3 AC Parameters

3.3.1 Testing Waveforms

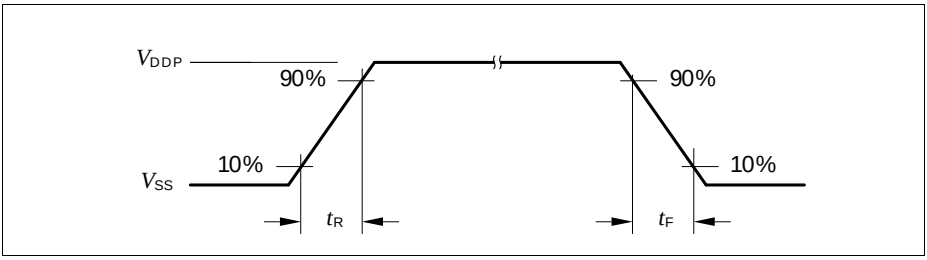

Figure 9 Rise/Fall Time Parameters

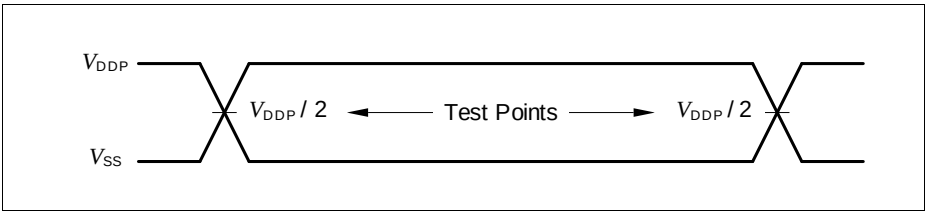

Figure 10 Testing Waveform, Output Delay

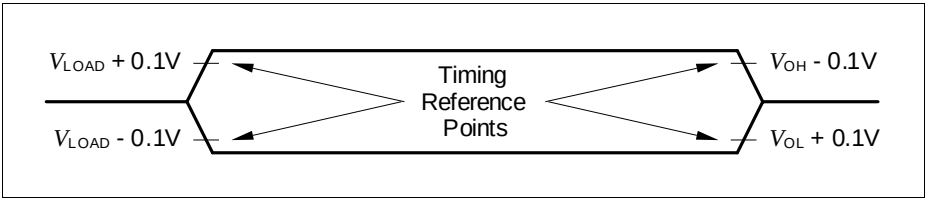

Figure 11 Testing Waveform, Output High Impedance

3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

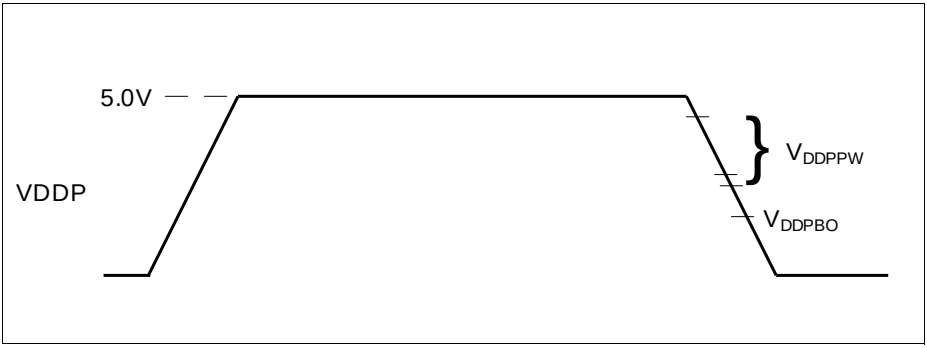

Figure 12 Supply Threshold Parameters

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 21 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	68	ns	C_L = 50 pF
		–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	–	–	ns	

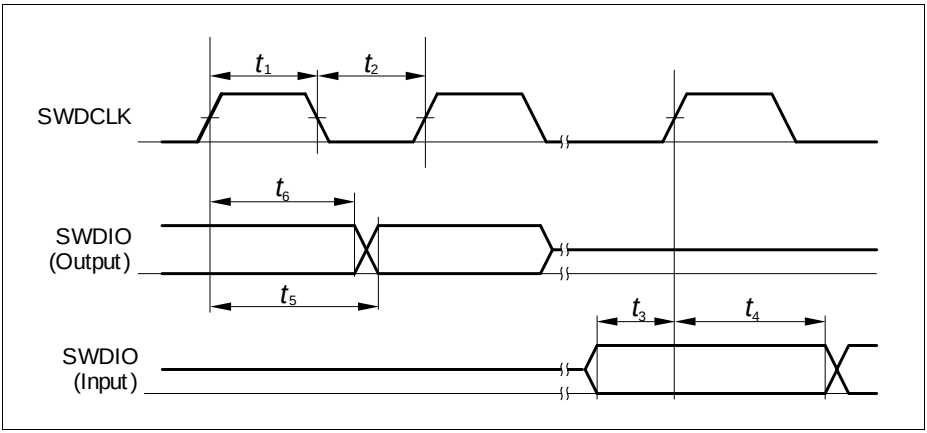

Figure 14 SWD Timing

4 Package and Reliability

The XMC1100 is a member of the XMC1000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 29 provides the thermal characteristics of the packages used in XMC1100.

Table 29 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8[1)]
		-	70.3	K/W	PG-TSSOP-38-9[1)]
		-	46.0	K/W	PG-VQFN-24-19[1)]
		-	38.4	K/W	PG-VQFN-40-13[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1100 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

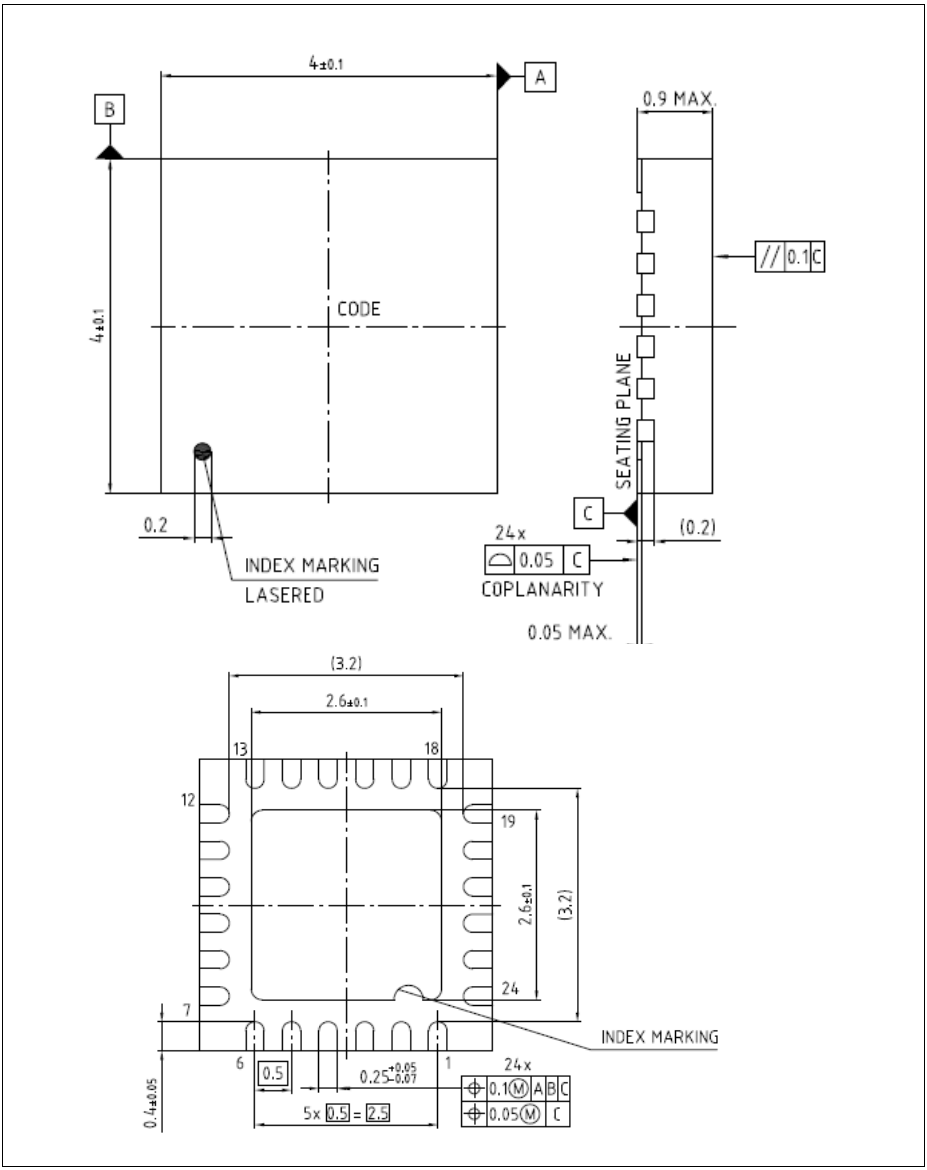

Figure 21 PG-VQFN-24-19

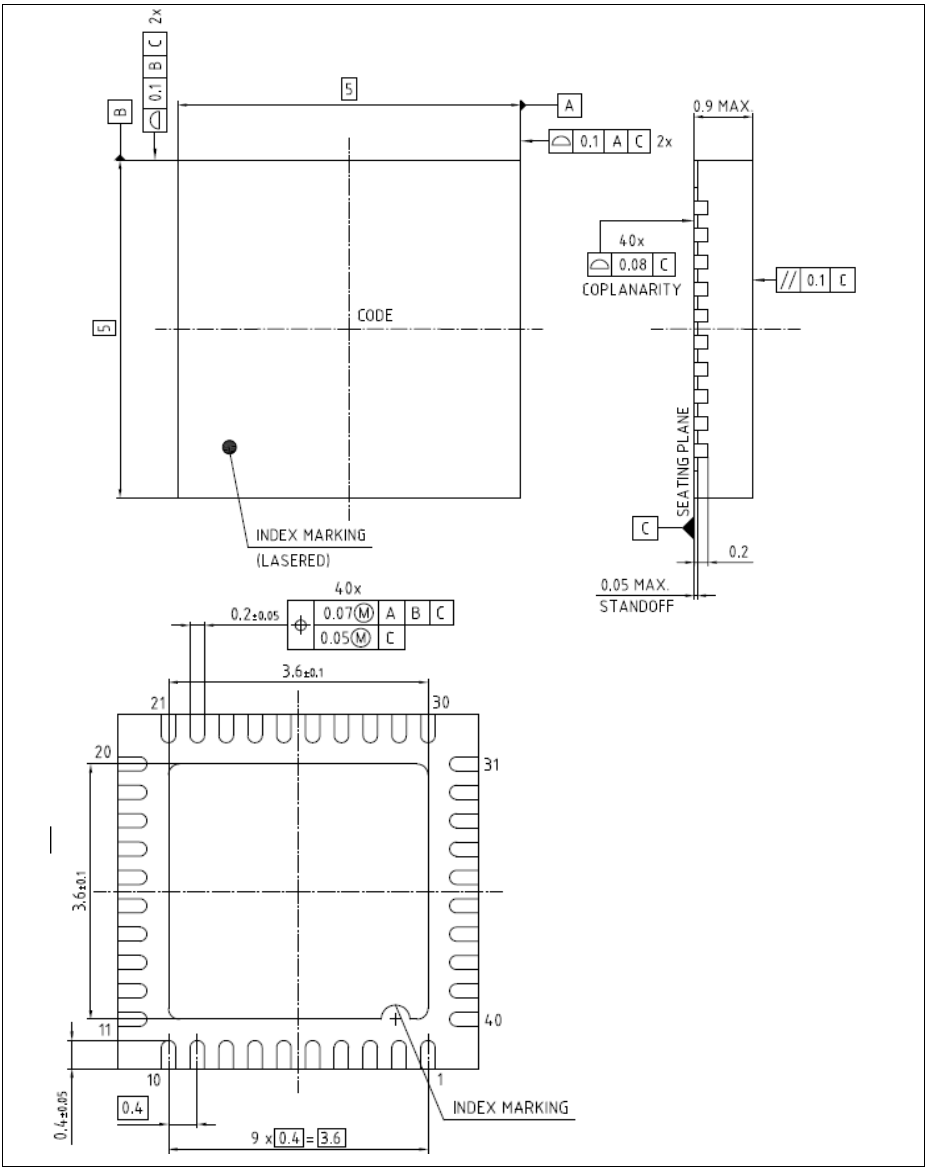

Figure 22 PG-VQFN-40-13

All dimensions in mm.

5 Quality Declaration

Table 30 shows the characteristics of the quality parameters in the XMC1100.

Table 30 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020C

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