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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 18432 |
| Number of I/O | 96 |
| Number of Gates | 60000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-FPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3p060-1fg144t |

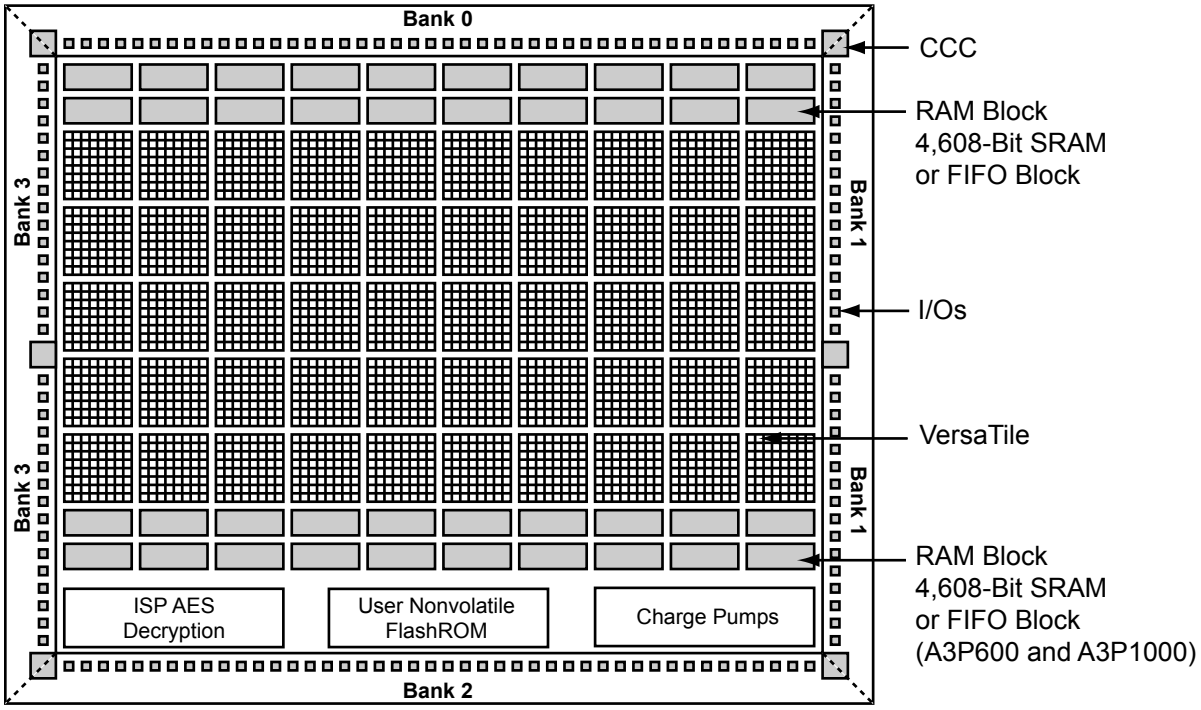


***Figure 1-2 •*** **Automotive ProASIC3 Device Architecture Overview with Four I/O Banks (A3P600 and A3P1000)**

## *VersaTiles*

The Automotive ProASIC3 core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The Automotive ProASIC3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-3 for VersaTile configurations.

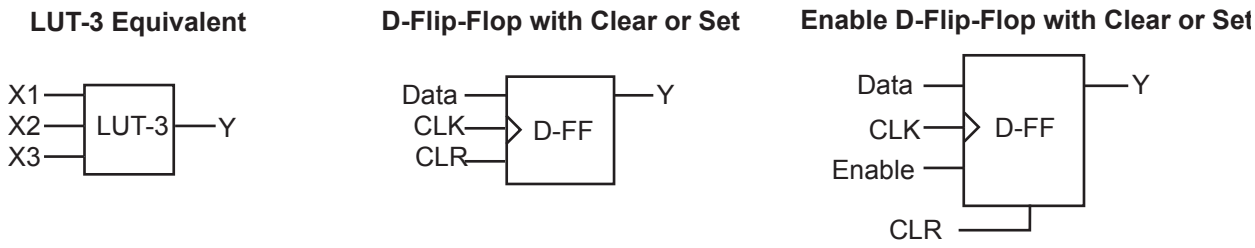


***Figure 1-3 •*** **VersaTile Configurations**

# Calculating Power Dissipation

## Quiescent Supply Current

**Table 2-6 • Quiescent Supply Current Characteristics**

| | A3P060 | A3P125 | A3P250 | A3P1000 |
|---|---|---|---|---|
| Typical (25°C) | 2 mA | 2 mA | 3 mA | 8 mA |
| Maximum (Automotive Grade 1) – 135°C | 53 mA | 53 mA | 106 mA | 265 mA |
| Maximum (Automotive Grade 2) – 115°C | 26 mA | 26 mA | 53 mA | 131 mA |

*Note: IDD Includes VCC, VPUMP, VCCI, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-7 and Table 2-10 on page 2-8.*

## Power per I/O Pin

**Table 2-7 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Advanced I/O Banks**

| | VMV (V) | Static Power PDC2 (mW)[1] | Dynamic Power PAC9 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 3.3 | – | 16.69 |
| 2.5 V LVCMOS | 2.5 | – | 5.12 |
| 1.8 V LVCMOS | 1.8 | – | 2.13 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.45 |
| 3.3 V PCI | 3.3 | – | 18.11 |
| 3.3 V PCI-X | 3.3 | – | 18.11 |
| **Differential** | | | |
| LVDS | 2.5 | 2.26 | 1.20 |
| LVPECL | 3.3 | 5.72 | 1.87 |

*Notes:*

1. *$P_{DC2}$ is the static power (where applicable) measured on VMV.*
2. *$P_{AC9}$ is the total dynamic power measured on $V_{CC}$ and VMV.*

### Total Static Power Consumption—$P_{STAT}$

$$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

### Total Dynamic Power Consumption—$P_{DYN}$

$$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

### Global Clock Contribution—$P_{CLOCK}$

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Automotive ProASIC3 FPGA Fabric User's Guide*.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the *Automotive ProASIC3 FPGA Fabric User's Guide*.

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

### Sequential Cells Contribution—$P_{S\text{-}CELL}$

$$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

### Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

### Routing Net Contribution—$P_{NET}$

$$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

### I/O Input Buffer Contribution—$P_{INPUTS}$

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-12 on page 2-11.

$F_{CLK}$ is the global clock signal frequency.

**Table 2-13 • Enable Rate Guidelines Recommended for Power Calculation**

| Component | Definition | Guideline |
|---|---|---|
| $\beta_1$ | I/O output buffer enable rate | 100% |
| $\beta_2$ | RAM enable rate for read operations | 12.5% |
| $\beta_3$ | RAM enable rate for write operations | 12.5% |

# User I/O Characteristics

## Timing Model

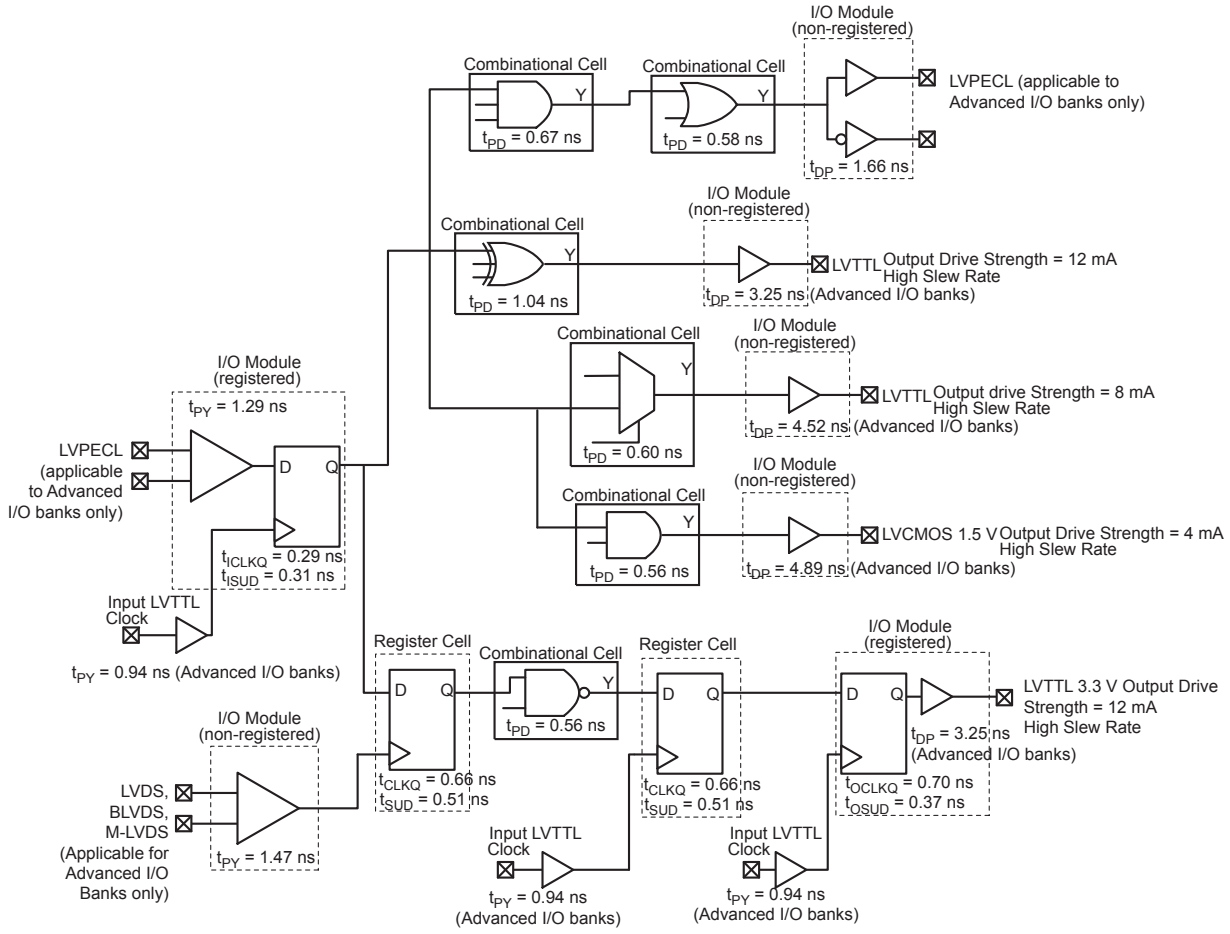


**Figure 2-3 • Timing Model**
**Operating Conditions: –1 Speed, Automotive Grade 2 Temp. Range ($T_J$ = 115°C), Worst Case VCC = 1.425 V**

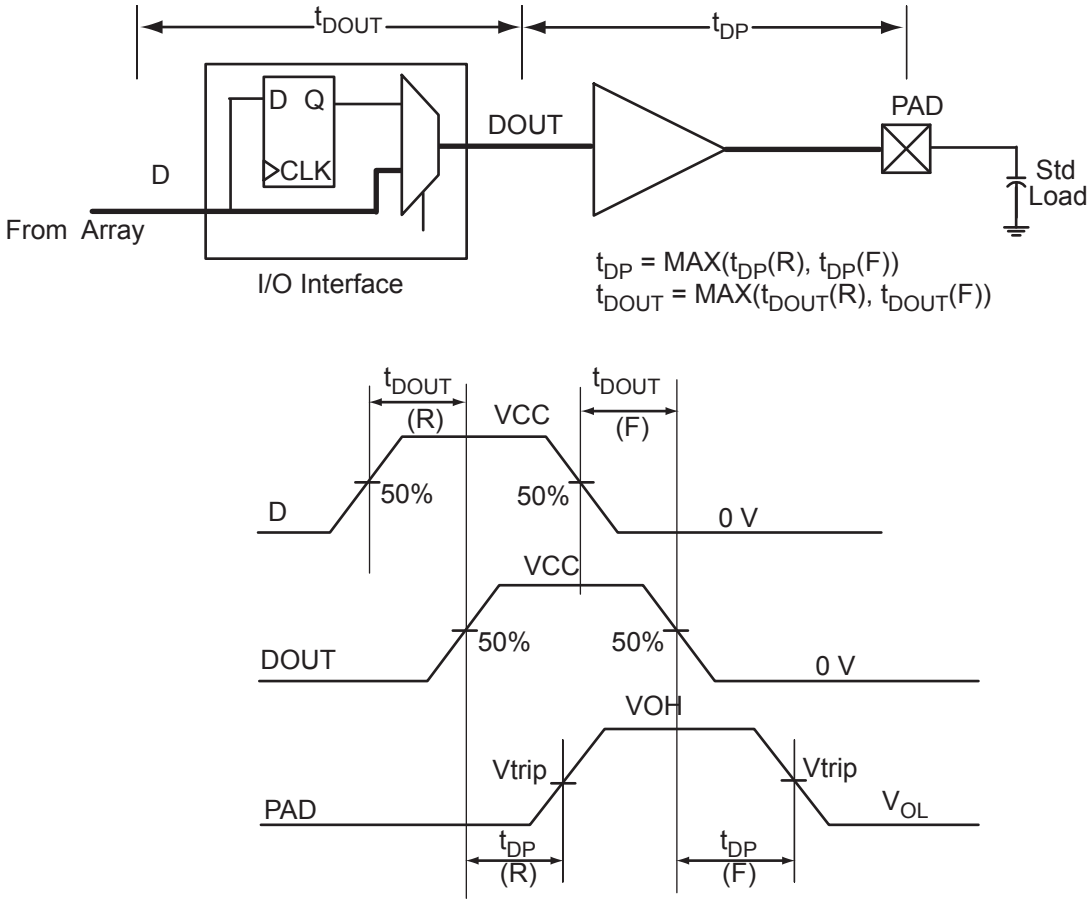


***Figure 2-5 •*** **Output Buffer Model and Delays (example)**

**Table 2-19 • I/O AC Parameter Definitions**

| Parameter | Parameter Definition |
|---|---|
| $t_{DP}$ | Data-to-Pad delay through the Output Buffer |
| $t_{PY}$ | Pad-to-Data delay through the Input Buffer |
| $t_{DOUT}$ | Data–to–Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable–to–Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer–to–Data delay through the I/O interface |
| $t_{HZ}$ | Enable-to-Pad delay through the Output Buffer—High to Z |
| $t_{ZH}$ | Enable-to-Pad delay through the Output Buffer—Z to High |
| $t_{LZ}$ | Enable-to-Pad delay through the Output Buffer—Low to Z |
| $t_{ZL}$ | Enable-to-Pad delay through the Output Buffer—Z to Low |
| $t_{ZHS}$ | Enable-to-Pad delay through the Output Buffer with delayed enable—Z to High |
| $t_{ZLS}$ | Enable-to-Pad delay through the Output Buffer with delayed enable—Z to Low |

**Table 2-20 • Summary of I/O Timing Characteristics—Software Default Settings**
**–1 Speed Grade, Automotive-Case Conditions: $T_J$ = 115°C, Worst Case VCC = 1.425 V**
**Worst Case VCCI = 3.0 V**
**Advanced I/O Banks**

| I/O Standard | Drive Strength (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | High | 35 pF | – | 0.53 | 3.25 | 0.04 | 0.94 | 0.38 | 3.31 | 1.51 | 2.96 | 1.88 | 5.37 | 2.71 | ns |
| 2.5 V LVCMOS | 12 mA | High | 35 pF | – | 0.53 | 3.28 | 0.04 | 1.19 | 0.38 | 3.34 | 3.16 | 1.77 | 1.80 | 5.39 | 5.22 | ns |
| 1.8 V LVCMOS | 12 mA | High | 35 pF | – | 0.53 | 3.25 | 0.04 | 1.12 | 0.38 | 1.89 | 1.63 | 3.41 | 3.75 | 3.06 | 2.82 | ns |
| 1.5 V LVCMOS | 12 mA | High | 35 pF | – | 0.53 | 3.75 | 0.04 | 1.32 | 0.38 | 2.18 | 1.91 | 3.63 | 3.87 | 3.35 | 3.11 | ns |
| 3.3 V PCI | Per PCI spec | High | 10 pF | 25 [2] | 0.53 | 2.12 | 0.04 | 0.78 | 0.38 | 1.23 | 0.91 | 2.57 | 2.96 | 2.41 | 2.11 | ns |
| 3.3 V PCI-X | Per PCI-X spec | High | 10 pF | 25 [2] | 0.53 | 2.47 | 0.04 | 0.77 | 0.38 | 1.23 | 0.91 | 2.57 | 2.96 | 2.41 | 2.11 | ns |
| LVDS | 24 mA | High | – | – | 0.53 | 1.68 | 0.04 | 1.47 | – | – | – | – | – | – | – | ns |
| LVPECL | 24 mA | High | – | – | 0.53 | 1.66 | 0.04 | 1.29 | – | – | – | – | – | – | – | ns |

*Notes:*

1. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-48 for connectivity. This resistor is not required during normal operation.*

**Table 2-58 • 1.8 V LVCMOS Low Slew**
**Automotive-Case Conditions: $T_J$ = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.64 | 17.36 | 0.05 | 1.45 | 0.46 | 15.78 | 17.36 | 1.53 | 0.87 | 18.28 | 19.864 | ns |
| | -1 | 0.55 | 14.77 | 0.04 | 1.23 | 0.39 | 13.42 | 14.77 | 1.54 | 0.87 | 15.55 | 16.897 | ns |
| 4 mA | STD | 0.64 | 11.71 | 0.05 | 1.45 | 0.46 | 11.64 | 11.71 | 1.78 | 1.48 | 14.14 | 14.214 | ns |
| | -1 | 0.55 | 9.96 | 0.04 | 1.23 | 0.39 | 9.90 | 9.96 | 1.78 | 1.48 | 12.03 | 12.091 | ns |
| 6 mA | STD | 0.64 | 9.00 | 0.05 | 1.45 | 0.46 | 9.17 | 8.77 | 1.95 | 1.77 | 11.67 | 11.267 | ns |
| | -1 | 0.55 | 7.66 | 0.04 | 1.23 | 0.39 | 7.80 | 7.46 | 1.95 | 1.77 | 9.92 | 9.585 | ns |
| 8 mA | STD | 0.64 | 8.39 | 0.05 | 1.45 | 0.46 | 8.54 | 8.16 | 1.99 | 1.85 | 11.04 | 10.66 | ns |
| | -1 | 0.55 | 7.14 | 0.04 | 1.23 | 0.39 | 7.27 | 6.94 | 1.99 | 1.85 | 9.40 | 9.068 | ns |
| 12 mA | STD | 0.64 | 8.15 | 0.05 | 1.45 | 0.46 | 8.09 | 8.15 | 2.05 | 2.14 | 10.59 | 10.654 | ns |
| | -1 | 0.55 | 6.94 | 0.04 | 1.23 | 0.39 | 6.88 | 6.94 | 2.05 | 2.14 | 9.01 | 9.063 | ns |
| 16 mA | STD | 0.64 | 8.15 | 0.05 | 1.45 | 0.46 | 8.09 | 8.15 | 2.05 | 2.14 | 10.59 | 10.654 | ns |
| | -1 | 0.55 | 6.94 | 0.04 | 1.23 | 0.39 | 6.88 | 6.94 | 2.05 | 2.14 | 9.01 | 9.063 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

**Table 2-59 • 1.8 V LVCMOS High Slew**
**Automotive-Case Conditions: $T_J$ = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Plus I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.64 | 13.26 | 0.05 | 1.36 | 0.46 | 9.75 | 12.67 | 1.24 | 0.82 | 12.26 | 15.17 | ns |
| | -1 | 0.55 | 11.28 | 0.04 | 1.16 | 0.39 | 8.30 | 10.78 | 1.24 | 0.83 | 10.43 | 12.905 | ns |
| 4 mA | STD | 0.64 | 7.73 | 0.05 | 1.36 | 0.46 | 6.13 | 7.25 | 1.46 | 1.41 | 8.63 | 9.749 | ns |
| | -1 | 0.55 | 6.58 | 0.04 | 1.16 | 0.39 | 5.21 | 6.17 | 1.46 | 1.41 | 7.34 | 8.293 | ns |
| 6 mA | STD | 0.64 | 4.97 | 0.05 | 1.36 | 0.46 | 4.29 | 4.54 | 1.62 | 1.68 | 6.79 | 7.039 | ns |
| | -1 | 0.55 | 4.23 | 0.04 | 1.16 | 0.39 | 3.65 | 3.86 | 1.62 | 1.68 | 5.78 | 5.987 | ns |
| 8 mA | STD | 0.64 | 4.39 | 0.05 | 1.36 | 0.46 | 4.29 | 4.54 | 1.62 | 1.68 | 6.79 | 7.039 | ns |
| | -1 | 0.55 | 3.73 | 0.04 | 1.16 | 0.39 | 3.65 | 3.86 | 1.62 | 1.68 | 5.78 | 5.987 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

**Table 2-70 • 1.5 V LVCMOS High Slew**
**Automotive-Case Conditions: $T_J$ = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Plus I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.64 | 8.76 | 0.05 | 1.59 | 0.46 | 7.63 | 9.35 | 1.87 | 1.50 | 10.13 | 11.851 | ns |
| | -1 | 0.55 | 7.45 | 0.04 | 1.35 | 0.39 | 6.49 | 7.95 | 1.87 | 1.50 | 8.62 | 10.081 | ns |
| 4 mA | STD | 0.64 | 5.41 | 0.05 | 1.59 | 0.46 | 5.42 | 5.94 | 2.07 | 1.84 | 7.92 | 8.442 | ns |
| | -1 | 0.55 | 4.60 | 0.04 | 1.35 | 0.39 | 4.61 | 5.05 | 2.07 | 1.85 | 6.74 | 7.181 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

**Table 2-71 • 1.5 V LVCMOS Low Slew**
**Automotive-Case Conditions: $T_J$ = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Plus I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.64 | 13.51 | 0.05 | 1.45 | 0.46 | 14.32 | 14.29 | 1.88 | 1.43 | 16.82 | 16.794 | ns |
| | -1 | 0.55 | 11.49 | 0.04 | 1.23 | 0.39 | 12.18 | 12.16 | 1.88 | 1.43 | 14.31 | 14.286 | ns |
| 4 mA | STD | 0.64 | 10.38 | 0.05 | 1.45 | 0.46 | 11.40 | 10.67 | 2.07 | 1.77 | 13.90 | 13.175 | ns |
| | -1 | 0.55 | 8.83 | 0.04 | 1.23 | 0.39 | 9.70 | 9.08 | 2.07 | 1.77 | 11.82 | 11.207 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

**Table 2-72 • 1.5 V LVCMOS High Slew**
**Automotive-Case Conditions: $T_J$ = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.63 | 9.05 | 0.05 | 1.56 | 0.45 | 7.38 | 9.05 | 1.81 | 1.45 | 9.80 | 11.47 | ns |
| | -1 | 0.53 | 7.70 | 0.04 | 1.32 | 0.38 | 6.28 | 7.70 | 1.81 | 1.45 | 8.34 | 9.75 | ns |
| 4 mA | STD | 0.63 | 5.75 | 0.05 | 1.56 | 0.45 | 5.25 | 5.75 | 2.00 | 1.78 | 7.67 | 8.17 | ns |
| | -1 | 0.53 | 4.89 | 0.04 | 1.32 | 0.38 | 4.46 | 4.89 | 2.00 | 1.78 | 6.52 | 6.95 | ns |
| 6 mA | STD | 0.63 | 5.05 | 0.05 | 1.56 | 0.45 | 4.92 | 5.05 | 2.04 | 1.87 | 7.34 | 7.47 | ns |
| | -1 | 0.53 | 4.29 | 0.04 | 1.32 | 0.38 | 4.19 | 4.29 | 2.04 | 1.87 | 6.24 | 6.35 | ns |
| 8 mA | STD | 0.63 | 4.41 | 0.05 | 1.56 | 0.45 | 2.18 | 1.91 | 4.27 | 4.55 | 3.35 | 3.11 | ns |
| | -1 | 0.53 | 3.75 | 0.04 | 1.32 | 0.38 | 2.18 | 1.91 | 3.63 | 3.87 | 3.35 | 3.11 | ns |
| 12 mA | STD | 0.63 | 4.41 | 0.05 | 1.56 | 0.45 | 2.18 | 1.91 | 4.27 | 4.55 | 3.35 | 3.11 | ns |
| | -1 | 0.53 | 3.75 | 0.04 | 1.32 | 0.38 | 2.18 | 1.91 | 3.63 | 3.87 | 3.35 | 3.11 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

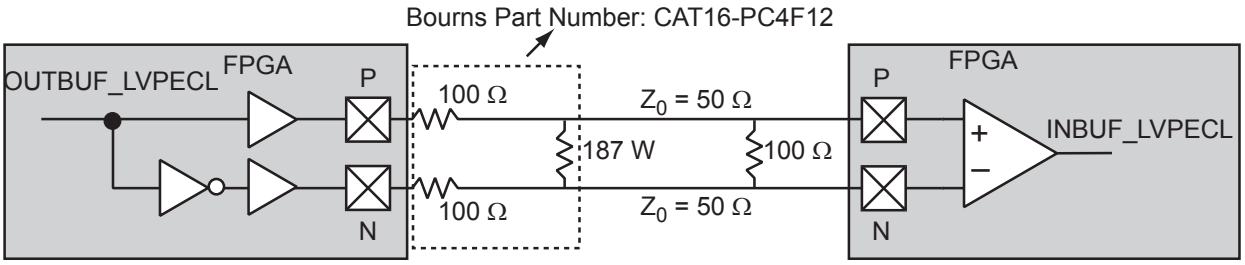


***Figure 2-14 •*** **LVPECL Circuit Diagram and Board-Level Implementation**

***Table 2-86 •*** **Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| VCCI | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| VOL | Output Low Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| VOH | Output High Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VIL, VIH | Input Low, Input High Voltages | 0 | 3.6 | 0 | 3.6 | 0 | 3.6 | V |
| VODIFF | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| VOCM | Output Common-Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| VICM | Input Common-Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| VIDIFF | Input Differential Voltage | 300 | | 300 | | 300 | | mV |

***Table 2-87 •*** **AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) |
|---|---|---|
| 1.64 | 1.94 | Cross point |

*Note: *Measuring point = Vtrip. See Table 2-18 on page 2-17 for a complete table of trip points.*

## Timing Characteristics

***Table 2-88 •*** **LVPECL**
**Automotive-Case Conditions: $T_J$ = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.64 | 2.01 | 0.05 | 1.57 | ns |
| –1 | 0.55 | 1.71 | 0.04 | 1.34 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

***Table 2-89 •*** **LVPECL**
**Automotive-Case Conditions: $T_J$ = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.63 | 1.95 | 0.05 | 1.52 | ns |
| –1 | 0.53 | 1.66 | 0.04 | 1.29 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

**Table 2-97 • Output Enable Register Propagation Delays**
**Automotive-Case Conditions: $T_J$ = 115°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 0.53 | 0.62 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 0.37 | 0.44 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | 0.00 | ns |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | 0.52 | 0.61 | ns |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | 0.00 | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 0.79 | 0.93 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 0.79 | 0.93 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.27 | 0.31 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.27 | 0.31 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.25 | 0.30 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.25 | 0.30 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.41 | 0.48 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.37 | 0.43 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

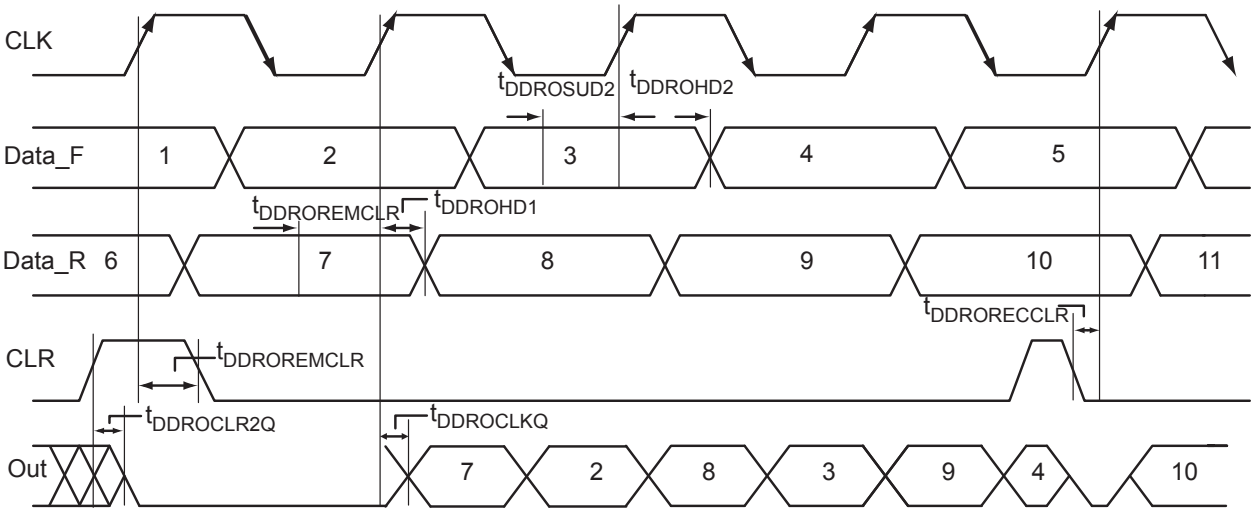


***Figure 2-23 •*** **Output DDR Timing Diagram**

## *Timing Characteristics*

***Table 2-102 •*** **Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 135°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 0.85 | 1.00 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.46 | 0.54 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.46 | 0.54 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 0.97 | 1.15 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.27 | 0.32 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.25 | 0.30 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR | 0.41 | 0.48 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR | 0.37 | 0.43 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 309 | 263 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

**Table 2-103 • Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 115°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 0.84 | 0.98 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.45 | 0.53 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.45 | 0.53 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 0.96 | 1.12 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.27 | 0.31 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.25 | 0.30 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR | 0.41 | 0.48 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR | 0.37 | 0.43 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 309 | 263 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

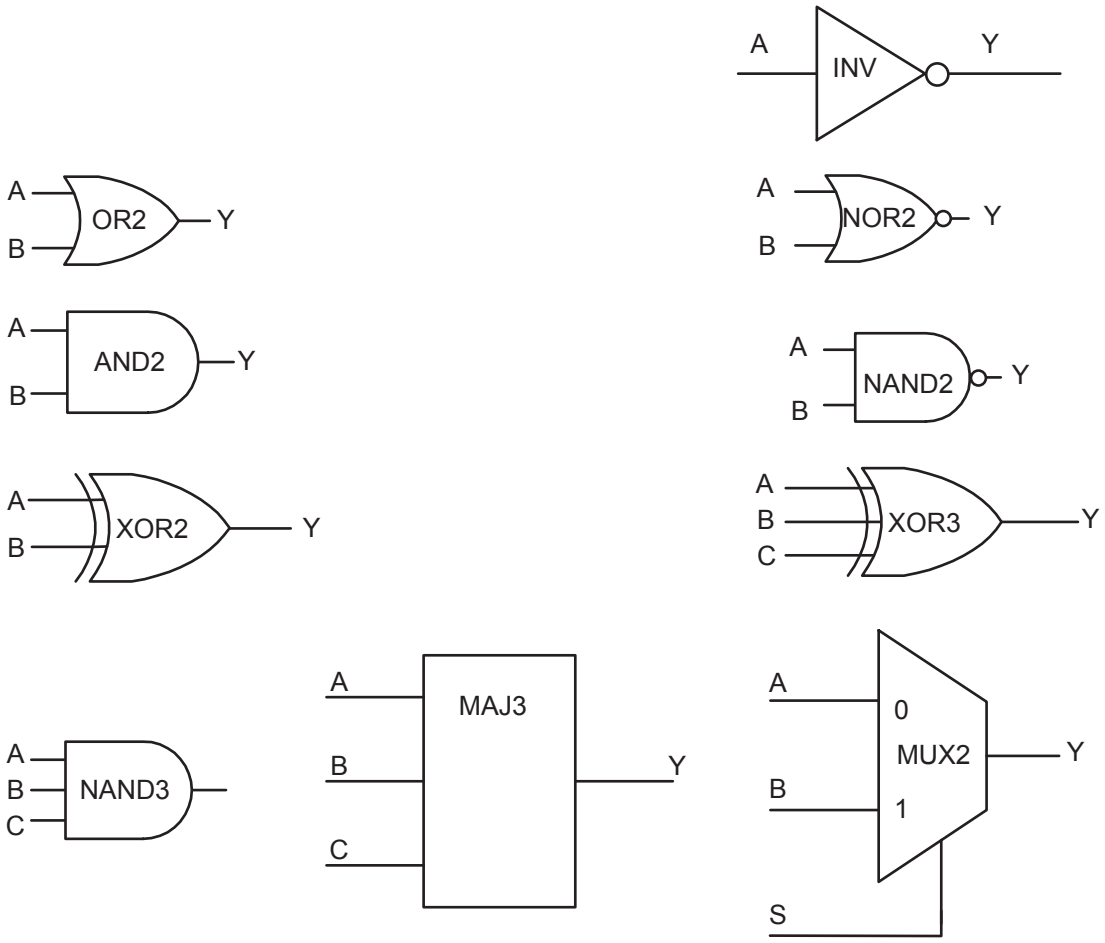


***Figure 2-24 •*** **Sample of Combinatorial Cells**

## Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-80. Table 2-114 on page 2-79 to Table 2-125 on page 2-97 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

### Timing Characteristics

**Table 2-108 • A3P060 Global Resource**
**Commercial-Case Conditions: $T_J$ = 135°C, VCC = 1.425 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.87 | 1.16 | 1.02 | 1.37 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.86 | 1.20 | 1.01 | 1.42 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.80 | | 0.94 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.98 | | 1.15 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.35 | | 0.41 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

**Table 2-109 • A3P060 Global Resource**
**Commercial-Case Conditions: $T_J$ = 115°C, VCC = 1.425 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.85 | 1.13 | 1.00 | 1.33 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.84 | 1.18 | 0.99 | 1.38 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.80 | | 0.94 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.98 | | 1.15 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.34 | | 0.40 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

| VQ100 | |
|---|---|
| Pin Number | A3P250 Function |
| 1 | GND |
| 2 | GAA2/IO118UDB3 |
| 3 | IO118VDB3 |
| 4 | GAB2/IO117UDB3 |
| 5 | IO117VDB3 |
| 6 | GAC2/IO116UDB3 |
| 7 | IO116VDB3 |
| 8 | IO112PSB3 |
| 9 | GND |
| 10 | GFB1/IO109PDB3 |
| 11 | GFB0/IO109NDB3 |
| 12 | VCOMPLF |
| 13 | GFA0/IO108NPB3 |
| 14 | VCCPLF |
| 15 | GFA1/IO108PPB3 |
| 16 | GFA2/IO107PSB3 |
| 17 | VCC |
| 18 | VCCIB3 |
| 19 | GFC2/IO105PSB3 |
| 20 | GEC1/IO100PDB3 |
| 21 | GEC0/IO100NDB3 |
| 22 | GEA1/IO98PDB3 |
| 23 | GEA0/IO98NDB3 |
| 24 | VMV3 |
| 25 | GNDQ |
| 26 | GEA2/IO97RSB2 |
| 27 | GEB2/IO96RSB2 |
| 28 | GEC2/IO95RSB2 |
| 29 | IO93RSB2 |
| 30 | IO92RSB2 |
| 31 | IO91RSB2 |
| 32 | IO90RSB2 |
| 33 | IO88RSB2 |
| 34 | IO86RSB2 |

| VQ100 | |
|---|---|
| Pin Number | A3P250 Function |
| 35 | IO85RSB2 |
| 36 | IO84RSB2 |
| 37 | VCC |
| 38 | GND |
| 39 | VCCIB2 |
| 40 | IO77RSB2 |
| 41 | IO74RSB2 |
| 42 | IO71RSB2 |
| 43 | GDC2/IO63RSB2 |
| 44 | GDB2/IO62RSB2 |
| 45 | GDA2/IO61RSB2 |
| 46 | GNDQ |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV2 |
| 51 | GND |
| 52 | VPUMP |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | VJTAG |
| 57 | GDA1/IO60USB1 |
| 58 | GDC0/IO58VDB1 |
| 59 | GDC1/IO58UDB1 |
| 60 | IO52NDB1 |
| 61 | GCB2/IO52PDB1 |
| 62 | GCA1/IO50PDB1 |
| 63 | GCA0/IO50NDB1 |
| 64 | GCC0/IO48NDB1 |
| 65 | GCC1/IO48PDB1 |
| 66 | VCCIB1 |
| 67 | GND |
| 68 | VCC |

| VQ100 | |
|---|---|
| Pin Number | A3P250 Function |
| 69 | IO43NDB1 |
| 70 | GBC2/IO43PDB1 |
| 71 | GBB2/IO42PSB1 |
| 72 | IO41NDB1 |
| 73 | GBA2/IO41PDB1 |
| 74 | VMV1 |
| 75 | GNDQ |
| 76 | GBA1/IO40RSB0 |
| 77 | GBA0/IO39RSB0 |
| 78 | GBB1/IO38RSB0 |
| 79 | GBB0/IO37RSB0 |
| 80 | GBC1/IO36RSB0 |
| 81 | GBC0/IO35RSB0 |
| 82 | IO29RSB0 |
| 83 | IO27RSB0 |
| 84 | IO25RSB0 |
| 85 | IO23RSB0 |
| 86 | IO21RSB0 |
| 87 | VCCIB0 |
| 88 | GND |
| 89 | VCC |
| 90 | IO15RSB0 |
| 91 | IO13RSB0 |
| 92 | IO11RSB0 |
| 93 | GAC1/IO05RSB0 |
| 94 | GAC0/IO04RSB0 |
| 95 | GAB1/IO03RSB0 |
| 96 | GAB0/IO02RSB0 |
| 97 | GAA1/IO01RSB0 |
| 98 | GAA0/IO00RSB0 |
| 99 | GNDQ |
| 100 | VMV0 |

| QN132 | |
|---|---|
| Pin Number | A3P250 Function |
| A1 | GAB2/IO117UPB3 |
| A2 | IO117VPB3 |
| A3 | VCCIB3 |
| A4 | GFC1/IO110PDB3 |
| A5 | GFB0/IO109NPB3 |
| A6 | VCCPLF |
| A7 | GFA1/IO108PPB3 |
| A8 | GFC2/IO105PPB3 |
| A9 | IO103NDB3 |
| A10 | VCC |
| A11 | GEA1/IO98PPB3 |
| A12 | GEA0/IO98NPB3 |
| A13 | GEC2/IO95RSB2 |
| A14 | IO91RSB2 |
| A15 | VCC |
| A16 | IO90RSB2 |
| A17 | IO87RSB2 |
| A18 | IO85RSB2 |
| A19 | IO82RSB2 |
| A20 | IO76RSB2 |
| A21 | IO70RSB2 |
| A22 | VCC |
| A23 | GDB2/IO62RSB2 |
| A24 | TDI |
| A25 | TRST |
| A26 | GDC1/IO58UDB1 |
| A27 | VCC |
| A28 | IO54NDB1 |
| A29 | IO52NDB1 |
| A30 | GCA2/IO51PPB1 |
| A31 | GCA0/IO50NPB1 |
| A32 | GCB1/IO49PDB1 |
| A33 | IO47NSB1 |
| A34 | VCC |
| A35 | IO41NPB1 |
| A36 | GBA2/IO41PPB1 |

| QN132 | |
|---|---|
| Pin Number | A3P250 Function |
| A37 | GBB1/IO38RSB0 |
| A38 | GBC0/IO35RSB0 |
| A39 | VCCIB0 |
| A40 | IO28RSB0 |
| A41 | IO22RSB0 |
| A42 | IO18RSB0 |
| A43 | IO14RSB0 |
| A44 | IO11RSB0 |
| A45 | IO07RSB0 |
| A46 | VCC |
| A47 | GAC1/IO05RSB0 |
| A48 | GAB0/IO02RSB0 |
| B1 | IO118VDB3 |
| B2 | GAC2/IO116UDB3 |
| B3 | GND |
| B4 | GFC0/IO110NDB3 |
| B5 | VCOMPLF |
| B6 | GND |
| B7 | GFB2/IO106PSB3 |
| B8 | IO103PDB3 |
| B9 | GND |
| B10 | GEB0/IO99NDB3 |
| B11 | VMV3 |
| B12 | GEB2/IO96RSB2 |
| B13 | IO92RSB2 |
| B14 | GND |
| B15 | IO89RSB2 |
| B16 | IO86RSB2 |
| B17 | GND |
| B18 | IO78RSB2 |
| B19 | IO72RSB2 |
| B20 | GND |
| B21 | GNDQ |
| B22 | TMS |
| B23 | TDO |
| B24 | GDC0/IO58VDB1 |

| QN132 | |
|---|---|
| Pin Number | A3P250 Function |
| B25 | GND |
| B26 | IO54PDB1 |
| B27 | GCB2/IO52PDB1 |
| B28 | GND |
| B29 | GCB0/IO49NDB1 |
| B30 | GCC1/IO48PDB1 |
| B31 | GND |
| B32 | GBB2/IO42PDB1 |
| B33 | VMV1 |
| B34 | GBA0/IO39RSB0 |
| B35 | GBC1/IO36RSB0 |
| B36 | GND |
| B37 | IO26RSB0 |
| B38 | IO21RSB0 |
| B39 | GND |
| B40 | IO13RSB0 |
| B41 | IO08RSB0 |
| B42 | GND |
| B43 | GAC0/IO04RSB0 |
| B44 | GNDQ |
| C1 | GAA2/IO118UDB3 |
| C2 | IO116VDB3 |
| C3 | VCC |
| C4 | GFB1/IO109PPB3 |
| C5 | GFA0/IO108NPB3 |
| C6 | GFA2/IO107PSB3 |
| C7 | IO105NPB3 |
| C8 | VCCIB3 |
| C9 | GEB1/IO99PDB3 |
| C10 | GNDQ |
| C11 | GEA2/IO97RSB2 |
| C12 | IO94RSB2 |
| C13 | VCCIB2 |
| C14 | IO88RSB2 |
| C15 | IO84RSB2 |
| C16 | IO80RSB2 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| G13 | GCC1/IO91PPB1 |
| G14 | IO90NPB1 |
| G15 | IO88PDB1 |
| G16 | IO88NDB1 |
| H1 | GFB0/IO208NPB3 |
| H2 | GFA0/IO207NDB3 |
| H3 | GFB1/IO208PPB3 |
| H4 | VCOMPLF |
| H5 | GFC0/IO209NPB3 |
| H6 | VCC |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | GCC0/IO91NPB1 |
| H13 | GCB1/IO92PPB1 |
| H14 | GCA0/IO93NPB1 |
| H15 | IO96NPB1 |
| H16 | GCB0/IO92NPB1 |
| J1 | GFA2/IO206PSB3 |
| J2 | GFA1/IO207PDB3 |
| J3 | VCCPLF |
| J4 | IO205NDB3 |
| J5 | GFB2/IO205PDB3 |
| J6 | VCC |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO95PPB1 |
| J13 | GCA1/IO93PPB1 |
| J14 | GCC2/IO96PPB1 |
| J15 | IO100PPB1 |
| J16 | GCA2/IO94PSB1 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| K1 | GFC2/IO204PDB3 |
| K2 | IO204NDB3 |
| K3 | IO203NDB3 |
| K4 | IO203PDB3 |
| K5 | VCCIB3 |
| K6 | VCC |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | VCC |
| K12 | VCCIB1 |
| K13 | IO95NPB1 |
| K14 | IO100NPB1 |
| K15 | IO102NDB1 |
| K16 | IO102PDB1 |
| L1 | IO202NDB3 |
| L2 | IO202PDB3 |
| L3 | IO196PPB3 |
| L4 | IO193PPB3 |
| L5 | VCCIB3 |
| L6 | GND |
| L7 | VCC |
| L8 | VCC |
| L9 | VCC |
| L10 | VCC |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | GDB0/IO112NPB1 |
| L14 | IO106NDB1 |
| L15 | IO106PDB1 |
| L16 | IO107PDB1 |
| M1 | IO197NSB3 |
| M2 | IO196NPB3 |
| M3 | IO193NPB3 |
| M4 | GEC0/IO190NPB3 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| M5 | VMV3 |
| M6 | VCCIB2 |
| M7 | VCCIB2 |
| M8 | IO147RSB2 |
| M9 | IO136RSB2 |
| M10 | VCCIB2 |
| M11 | VCCIB2 |
| M12 | VMV2 |
| M13 | IO110NDB1 |
| M14 | GDB1/IO112PPB1 |
| M15 | GDC1/IO111PDB1 |
| M16 | IO107NDB1 |
| N1 | IO194PSB3 |
| N2 | IO192PPB3 |
| N3 | GEC1/IO190PPB3 |
| N4 | IO192NPB3 |
| N5 | GNDQ |
| N6 | GEA2/IO187RSB2 |
| N7 | IO161RSB2 |
| N8 | IO155RSB2 |
| N9 | IO141RSB2 |
| N10 | IO129RSB2 |
| N11 | IO124RSB2 |
| N12 | GNDQ |
| N13 | IO110PDB1 |
| N14 | VJTAG |
| N15 | GDC0/IO111NDB1 |
| N16 | GDA1/IO113PDB1 |
| P1 | GEB1/IO189PDB3 |
| P2 | GEB0/IO189NDB3 |
| P3 | VMV2 |
| P4 | IO179RSB2 |
| P5 | IO171RSB2 |
| P6 | IO165RSB2 |
| P7 | IO159RSB2 |
| P8 | IO151RSB2 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| P9 | IO137RSB2 |
| P10 | IO134RSB2 |
| P11 | IO128RSB2 |
| P12 | VMV1 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO113NDB1 |
| R1 | GEA1/IO188PDB3 |
| R2 | GEA0/IO188NDB3 |
| R3 | IO184RSB2 |
| R4 | GEC2/IO185RSB2 |
| R5 | IO168RSB2 |
| R6 | IO163RSB2 |
| R7 | IO157RSB2 |
| R8 | IO149RSB2 |
| R9 | IO143RSB2 |
| R10 | IO138RSB2 |
| R11 | IO131RSB2 |
| R12 | IO125RSB2 |
| R13 | GDB2/IO115RSB2 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO183RSB2 |
| T3 | GEB2/IO186RSB2 |
| T4 | IO172RSB2 |
| T5 | IO170RSB2 |
| T6 | IO164RSB2 |
| T7 | IO158RSB2 |
| T8 | IO153RSB2 |
| T9 | IO142RSB2 |
| T10 | IO135RSB2 |
| T11 | IO130RSB2 |
| T12 | GDC2/IO116RSB2 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| T13 | IO120RSB2 |
| T14 | GDA2/IO114RSB2 |
| T15 | TMS |
| T16 | GND |

| Revision | Changes | Page |
|---|---|---|
| Revision 2 (continued) | The "Pin Descriptions and Packaging" chapter has been added (SAR 34767), | 3-1 |
| | The "VQ100" pin table for A3P125 has been added (SAR 37944). | 4-3 |
| | Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34767). | 4-1 |
| July 2010 | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Automotive ProASIC3 Device Status" table on page II indicates the status for each device in the device family. | N/A |

| Revision | Changes | Page |
|---|---|---|
| **Revision 1 (Dec 2009)** Product Brief v1.1 | The QNG132 package was added to the "Automotive ProASIC3 Product Family" table, "I/Os Per Package" table, "Automotive ProASIC3 Ordering Information", and "Temperature Grade Offerings". | I – IV |
| Packaging v1.1 | Pin tables for A3P125 and A3P250 were added for the "QN132" package. | 4-6 |