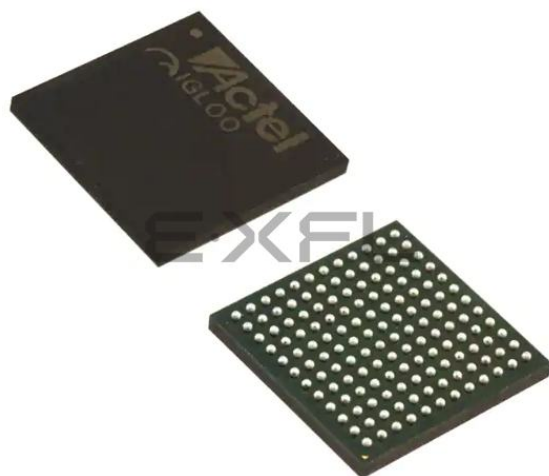




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

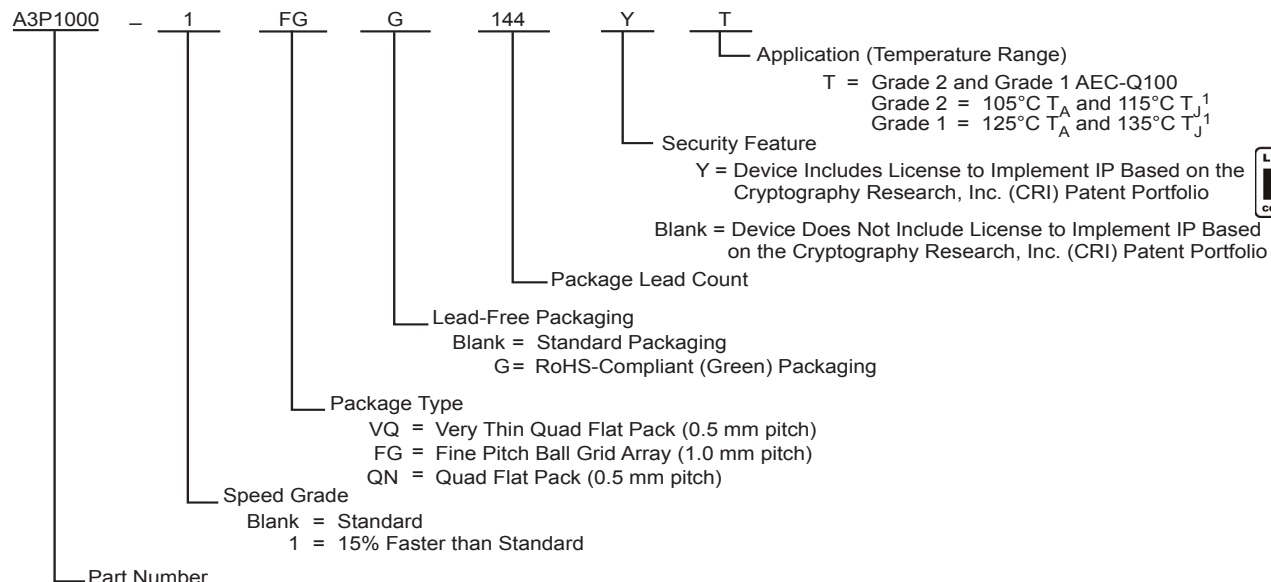
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	96
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p060-1fgg144t

Automotive ProASIC3 Ordering Information



Automotive ProASIC3 Devices

A3P060	= 60,000 System Gates
A3P125	= 125,000 System Gates
A3P250	= 250,000 System Gates
A3P1000	= 1,000,000 System Gates

Notes:

- T_A = Ambient temperature and T_J = Junction temperature.
- Minimum order quantities apply. Contact your local Microsemi SoC Products Group sales office for details.

Temperature Grade Offerings

Package	A3P060	A3P125	A3P250	A3P1000
VQ100	C, I, T	C, I, T	C, I, T	–
FG144	C, I, T	C, I, T	C, I, T	C, I, T
FG256	–	–	C, I, T	C, I, T
FG484	–	–	–	C, I, T
QNG132	–	C, I, T	C, I, T	–

Notes:

1. C = Commercial temperature range: 0°C to 70°C
2. I = Industrial temperature range: –40°C to 85°C
3. T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100
 Grade 2 = 105°C T_A and 115°C T_J
 Grade 1 = 125°C T_A and 135°C T_J
4. Specifications for Commercial and Industrial grade devices can be found in the [ProASIC3 Flash Family FPGAs datasheet](#).

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
T (Grade 1 and Grade 2), Commercial, Industrial	3	3

Notes:

1. T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100
 Grade 2 = 105°C T_A and 115°C T_J
 Grade 1 = 125°C T_A and 135°C T_J
2. Specifications for Commercial and Industrial grade devices can be found in the [ProASIC3 Flash Family FPGAs datasheet](#).

Contact your local Microsemi SoC Products Group representative for device availability:
<http://www.microsemi.com/soc/contact/default.aspx>.

Advanced Architecture

The proprietary Automotive ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The Automotive ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM memory
- Extensive CCCs and PLLs
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the Automotive ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

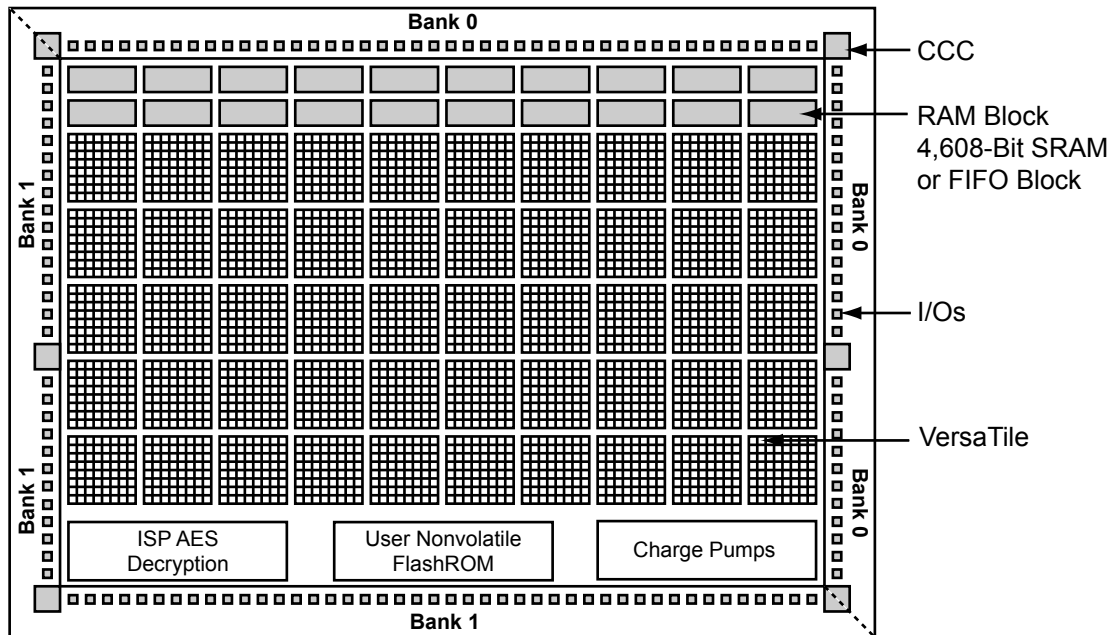


Figure 1-1 • Automotive ProASIC3 Device Architecture Overview with Two I/O Banks (A3P060 and A3P125)

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{20.5^{\circ}\text{C/W}} = 1.951 \text{ W}$$

EQ 2

Table 2-4 • Package Thermal Resistivities

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Units
				Still Air	200 ft./min.	500 ft./min.	
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	°C/W
Fine Pitch Ball Grid Array (FBGA)	See note*	144	3.8	26.9	22.9	21.5	°C/W
	See note*	256	3.8	26.6	22.8	21.5	°C/W
	See note*	484	3.2	20.5	17.0	15.9	°C/W
	A3P1000	144	6.3	31.6	26.2	24.2	°C/W
	A3P1000	256	6.6	28.1	24.4	22.7	°C/W
	A3P1000	484	8.0	23.3	19.0	16.7	°C/W

Note: *This information applies to all ProASIC3 devices except the A3P1000. Detailed device/package thermal information will be available in future revisions of the datasheet.

Temperature and Voltage Derating Factors

Table 2-5 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 115^{\circ}\text{C}$, $V_{CC} = 1.425 \text{ V}$)

Array Voltage V_{CC} (V)	−40°C	0°C	25°C	70°C	85°C	115°C	125°C	135°C
1.425	0.83	0.88	0.90	0.95	0.97	1.00	1.01	1.02
1.5	0.79	0.83	0.85	0.90	0.92	0.95	0.96	0.97
1.575	0.76	0.80	0.82	0.87	0.88	0.91	0.93	0.94

Power Consumption of Various Internal Resources

Table 2-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices

Parameter	Definition	Device Specific Dynamic Power (μW/MHz)			
		A3P1000	A3P250	A3P125	A3P060
PAC1	Clock contribution of a Global Rib	14.50	11.00	11.00	9.30
PAC2	Clock contribution of a Global Spine	2.48	1.58	0.81	0.81
PAC3	Clock contribution of a VersaTile row	0.81			
PAC4	Clock contribution of a VersaTile used as a sequential module	0.12			
PAC5	First contribution of a VersaTile used as a sequential module	0.07			
PAC6	Second contribution of a VersaTile used as a sequential module	0.29			
PAC7	Contribution of a VersaTile used as a combinatorial module	0.29			
PAC8	Average contribution of a routing net	0.70			
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-7 on page 2-6 .			
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-7 and Table 2-10 on page 2-8 .			
PAC11	Average contribution of a RAM block during a read operation	25.00			
PAC12	Average contribution of a RAM block during a write operation	30.00			
PAC13	Static PLL contribution	2.55 mW			
PAC14	Dynamic contribution for PLL	2.60			

Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-12 on page 2-11](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-13 on page 2-12](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-13 on page 2-12](#). The calculation should be repeated for each clock domain defined in the design.

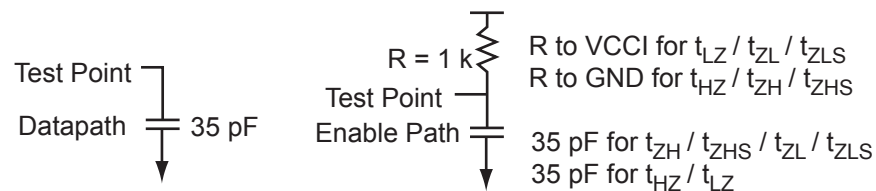
Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.


Figure 2-7 • AC Loading
Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	1.4	35

Note: *Measuring point = V_{trip} . See [Table 2-18 on page 2-17](#) for a complete table of trip points.

Timing Characteristics

Table 2-46 • 2.5 V LVCMOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.69	0.05	1.45	0.46	8.76	9.69	1.48	1.25	11.26	12.187	ns
	-1	0.55	8.24	0.04	1.23	0.39	7.45	8.24	1.48	1.25	9.58	10.367	ns
6 mA	STD	0.64	5.78	0.05	1.45	0.46	5.63	5.78	1.68	1.62	8.13	8.277	ns
	-1	0.55	4.91	0.04	1.23	0.39	4.79	4.91	1.69	1.63	6.92	7.04	ns
12 mA	STD	0.64	3.98	0.05	1.45	0.46	4.05	3.84	1.82	1.86	6.55	6.338	ns
	-1	0.55	3.39	0.04	1.23	0.39	3.45	3.27	1.83	1.86	5.58	5.392	ns
16 mA	STD	0.64	3.75	0.05	1.45	0.46	1.85	1.69	3.76	3.97	3.06	2.926	ns
	-1	0.55	3.19	0.04	1.23	0.39	1.85	1.69	3.20	3.38	3.06	2.929	ns
24 mA	STD	0.64	3.45	0.05	1.45	0.46	1.70	1.35	3.84	4.47	2.92	2.585	ns
	-1	0.55	2.94	0.04	1.23	0.39	1.71	1.35	3.27	3.80	2.92	2.586	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-47 • 2.5 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	12.12	0.05	1.45	0.46	12.54	12.74	1.48	1.19	15.04	15.243	ns
	-1	0.55	10.31	0.04	1.23	0.39	10.67	10.84	1.48	1.20	12.80	12.966	ns
6 mA	STD	0.64	8.24	0.05	1.45	0.46	9.07	8.74	1.68	1.57	11.57	11.237	ns
	-1	0.55	7.01	0.04	1.23	0.39	7.71	7.43	1.69	1.57	9.84	9.559	ns
12 mA	STD	0.64	6.91	0.05	1.45	0.46	7.04	6.62	1.82	1.80	9.54	9.117	ns
	-1	0.55	5.88	0.04	1.23	0.39	5.99	5.63	1.83	1.80	8.11	7.756	ns
16 mA	STD	0.64	6.44	0.05	1.45	0.46	6.56	6.18	1.86	1.86	9.06	8.678	ns
	-1	0.55	5.48	0.04	1.23	0.39	5.58	5.26	1.86	1.86	7.71	7.382	ns
24 mA	STD	0.64	6.16	0.05	1.45	0.46	6.15	6.16	1.90	2.10	8.65	8.657	ns
	-1	0.55	5.24	0.04	1.23	0.39	5.23	5.24	1.90	2.10	7.36	7.364	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-48 • 2.5 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.26	0.05	1.45	0.46	8.28	9.26	1.24	1.12	10.78	11.756	ns
	-1	0.55	7.87	0.04	1.23	0.39	7.05	7.87	1.24	1.13	9.17	10	ns
6 mA	STD	0.64	5.43	0.05	1.45	0.46	5.19	5.43	1.43	1.47	7.69	7.926	ns
	-1	0.55	4.62	0.04	1.23	0.39	4.42	4.62	1.43	1.47	6.55	6.743	ns
12 mA	STD	0.64	3.59	0.05	1.45	0.46	3.65	3.51	1.56	1.69	6.15	6.012	ns
	-1	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.114	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-49 • 2.5 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	12.12	0.05	1.45	0.46	11.89	12.12	1.25	1.08	14.39	14.622	ns
	-1	0.55	10.31	0.04	1.23	0.39	10.12	10.31	1.25	1.08	12.24	12.438	ns
6 mA	STD	0.64	8.24	0.05	1.45	0.46	8.39	8.23	1.43	1.42	10.89	10.73	ns
	-1	0.55	7.01	0.04	1.23	0.39	7.14	7.00	1.43	1.42	9.26	9.128	ns
12 mA	STD	0.64	6.30	0.05	1.45	0.46	6.41	6.16	1.56	1.63	8.91	8.656	ns
	-1	0.55	5.35	0.04	1.23	0.39	5.45	5.24	1.56	1.63	7.58	7.364	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-90 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{iCLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{iSUD}	Data Setup Time for the Input Data Register	C, A
t_{iHD}	Data Hold Time for the Input Data Register	C, A
t_{iSUE}	Enable Setup Time for the Input Data Register	B, A
t_{iHE}	Enable Hold Time for the Input Data Register	B, A
t_{iPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-15 on page 2-53 for more information.

Table 2-95 • Output Data Register Propagation Delays
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.70	0.82	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.37	0.44	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.52	0.61	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.96	1.12	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.96	1.12	ns
t_{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.41	0.48	ns
t_{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Output Enable Register

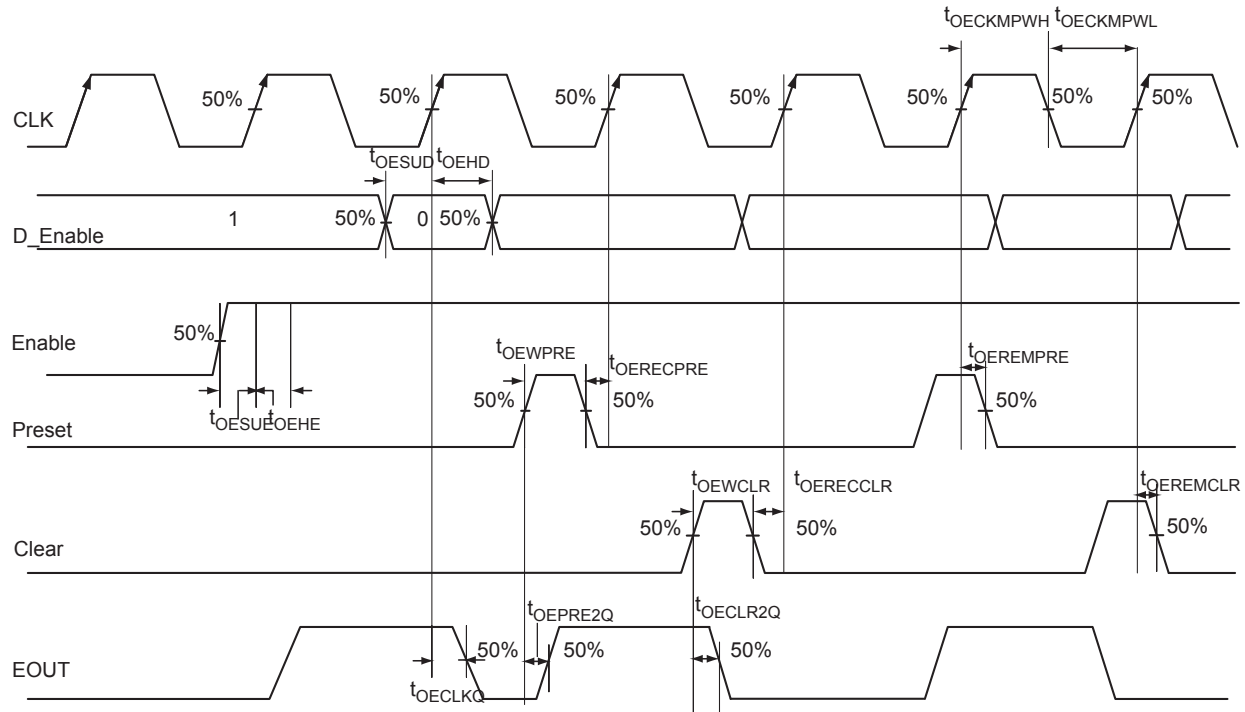


Figure 2-19 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-96 • Output Enable Register Propagation Delays

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.54	0.64	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.38	0.45	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.53	0.62	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.32	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.32	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OEWPRES}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

DDR Module Specifications

Input DDR Module

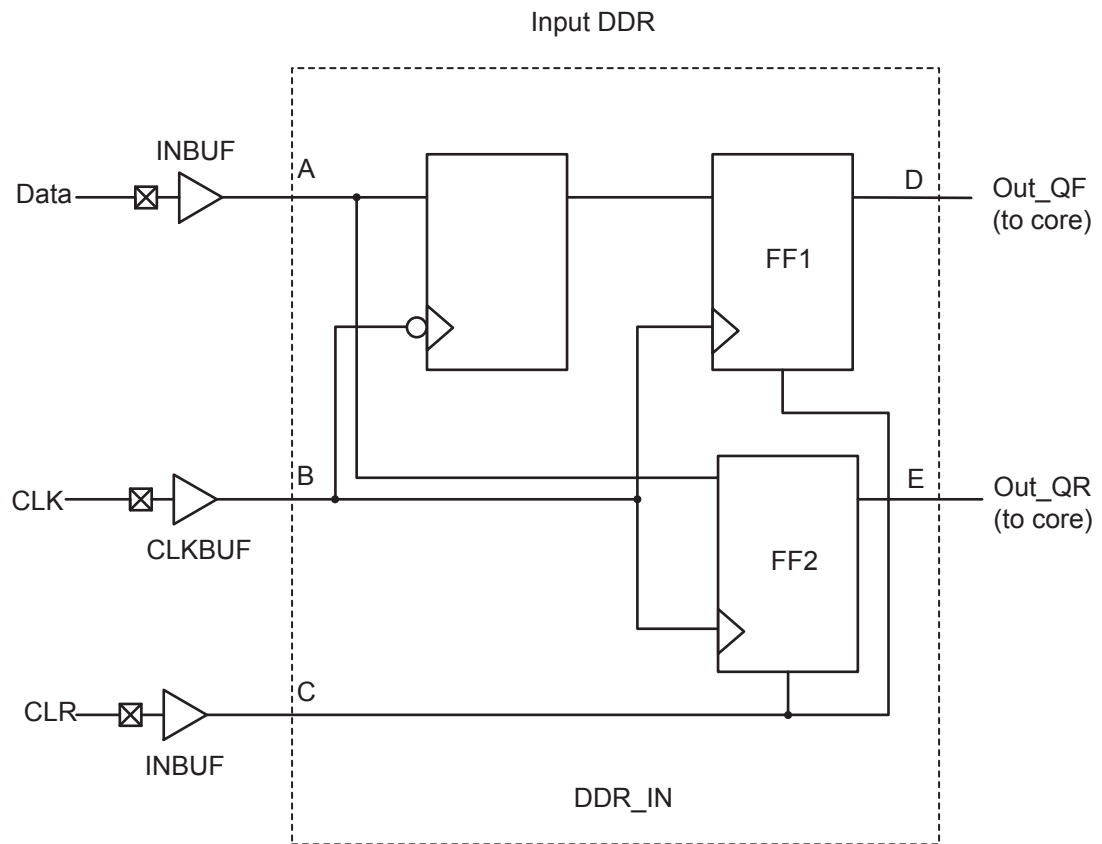


Figure 2-20 • Input DDR Timing Model

Table 2-98 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t_{DDRCLKQ1}	Clock-to-Out Out_QR	B, D
t_{DDRCLKQ2}	Clock-to-Out Out_QF	B, E
t_{DDRISUD}	Data Setup Time of DDR Input	A, B
$t_{\text{DDR IHD}}$	Data Hold Time of DDR Input	A, B
$t_{\text{DDRICLR2Q1}}$	Clear-to-Out Out_QR	C, D
$t_{\text{DDRICLR2Q2}}$	Clear-to-Out Out_QF	C, E
$t_{\text{DDRIREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRIRECCLR}}$	Clear Recovery	C, B

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [Fusion](#), [IGLOO/e](#) and [ProASIC3/E Macro Library Guide](#).

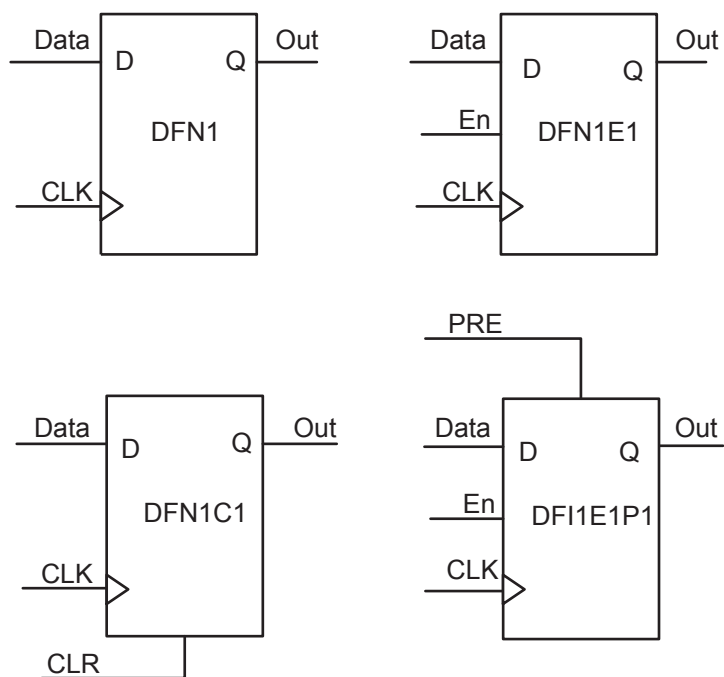


Figure 2-26 • Sample of Sequential Cells

Table 2-110 • A3P125 Global Resource
Commercial-Case Conditions: $T_J = 135^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.93	1.22	1.09	1.43	ns
t_{RCKH}	Input High Delay for Global Clock	0.92	1.26	1.08	1.49	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35		0.41	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-111 • A3P125 Global Resource
Commercial-Case Conditions: $T_J = 115^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.90	1.19	1.06	1.40	ns
t_{RCKH}	Input High Delay for Global Clock	0.90	1.23	1.05	1.45	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.34		0.40	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

VQ100	
Pin Number	A3P060 Function
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1

VQ100	
Pin Number	A3P060 Function
35	IO62RSB1
36	IO61RSB1
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC

VQ100	
Pin Number	A3P060 Function
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

FG144	
Pin Number	A3P1000 Function
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG484	
Pin Number	A3P1000 Function
E21	NC
E22	IO84PDB1
F1	NC
F2	IO215PDB3
F3	IO215NDB3
F4	IO224NDB3
F5	IO225NDB3
F6	VMV3
F7	IO11RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO25RSB0
F11	IO36RSB0
F12	IO42RSB0
F13	IO49RSB0
F14	IO56RSB0
F15	GBC0/IO72RSB0
F16	IO62RSB0
F17	VMV0
F18	IO78NDB1
F19	IO81NDB1
F20	IO82PPB1
F21	NC
F22	IO84NDB1
G1	IO214NDB3
G2	IO214PDB3
G3	NC
G4	IO222NDB3
G5	IO222PDB3
G6	GAC2/IO223PDB3
G7	IO223NDB3
G8	GNDQ
G9	IO23RSB0
G10	IO29RSB0
G11	IO33RSB0
G12	IO46RSB0

FG484	
Pin Number	A3P1000 Function
G13	IO52RSB0
G14	IO60RSB0
G15	GNDQ
G16	IO80NDB1
G17	GBB2/IO79PDB1
G18	IO79NDB1
G19	IO82NPB1
G20	IO85PDB1
G21	IO85NDB1
G22	NC
H1	NC
H2	NC
H3	V _{CC}
H4	IO217PDB3
H5	IO218PDB3
H6	IO221NDB3
H7	IO221PDB3
H8	VMV0
H9	V _{CCI} B0
H10	V _{CCI} B0
H11	IO38RSB0
H12	IO47RSB0
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO80PDB1
H17	IO83PPB1
H18	IO86PPB1
H19	IO87PDB1
H20	VCC
H21	NC
H22	NC
J1	IO212NDB3
J2	IO212PDB3
J3	NC
J4	IO217NDB3

FG484	
Pin Number	A3P1000 Function
J5	IO218NDB3
J6	IO216PDB3
J7	IO216NDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO83NPB1
J17	IO86NPB1
J18	IO90PPB1
J19	IO87NDB1
J20	NC
J21	IO89PDB1
J22	IO89NDB1
K1	IO211PDB3
K2	IO211NDB3
K3	NC
K4	IO210PPB3
K5	IO213NDB3
K6	IO213PDB3
K7	GFC1/IO209PPB3
K8	VCCIB3
K9	V _{CC}
K10	GND
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO91PPB1
K17	IO90NPB1
K18	IO88PDB1

FG484	
Pin Number	A3P1000 Function
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2

FG484	
Pin Number	A3P1000 Function
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1

FG484	
Pin Number	A3P1000 Function
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC

FG484	
Pin Number	A3P1000 Function
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	IO181RSB2
AA5	IO178RSB2
AA6	IO175RSB2
AA7	IO169RSB2
AA8	IO166RSB2
AA9	IO160RSB2
AA10	IO152RSB2
AA11	IO146RSB2
AA12	IO139RSB2
AA13	IO133RSB2
AA14	NC
AA15	NC
AA16	IO122RSB2
AA17	IO119RSB2
AA18	IO117RSB2
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	IO180RSB2
AB5	IO176RSB2
AB6	IO173RSB2

FG484	
Pin Number	A3P1000 Function
AB7	IO167RSB2
AB8	IO162RSB2
AB9	IO156RSB2
AB10	IO150RSB2
AB11	IO145RSB2
AB12	IO144RSB2
AB13	IO132RSB2
AB14	IO127RSB2
AB15	IO126RSB2
AB16	IO123RSB2
AB17	IO121RSB2
AB18	IO118RSB2
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND