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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

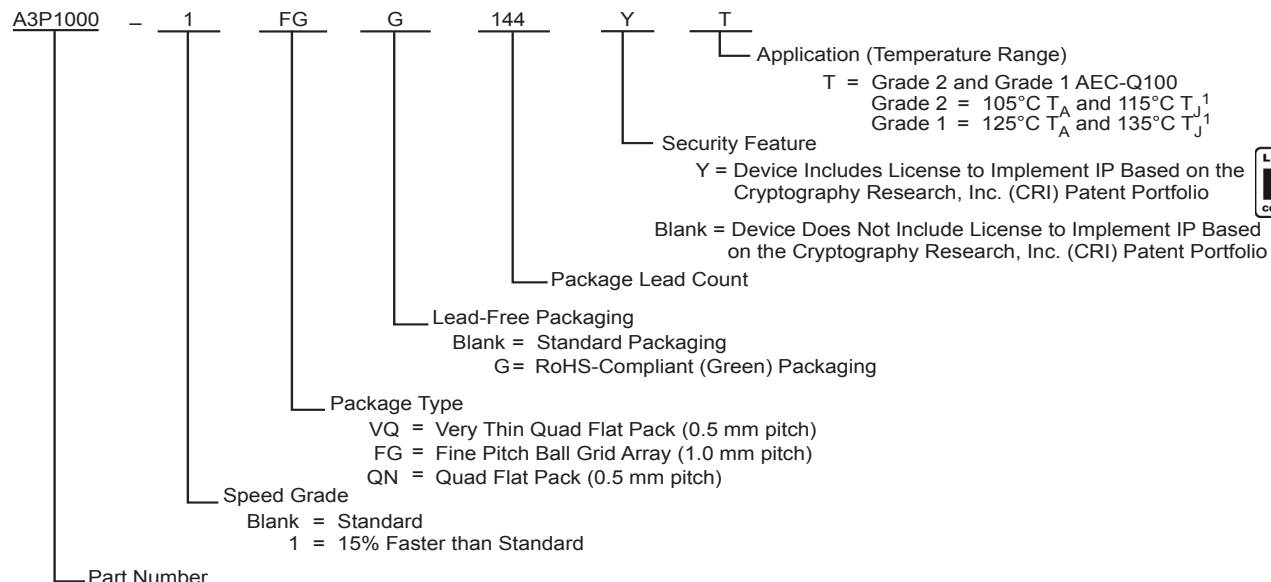
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	96
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p060-fg144t

Automotive ProASIC3 Ordering Information



Automotive ProASIC3 Devices

A3P060	= 60,000 System Gates
A3P125	= 125,000 System Gates
A3P250	= 250,000 System Gates
A3P1000	= 1,000,000 System Gates

Notes:

- T_A = Ambient temperature and T_J = Junction temperature.
- Minimum order quantities apply. Contact your local Microsemi SoC Products Group sales office for details.

Calculating Power Dissipation

Quiescent Supply Current

Table 2-6 • Quiescent Supply Current Characteristics

	A3P060	A3P125	A3P250	A3P1000
Typical (25°C)	2 mA	2 mA	3 mA	8 mA
Maximum (Automotive Grade 1) – 135°C	53 mA	53 mA	106 mA	265 mA
Maximum (Automotive Grade 2) – 115°C	26 mA	26 mA	53 mA	131 mA

Note: I_{DD} includes V_{CC} , V_{PUMP} , V_{CCI} , and V_{MV} currents. Values do not include I/O static contribution, which is shown in Table 2-7 and Table 2-10 on page 2-8.

Power per I/O Pin

Table 2-7 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings ¹
Applicable to Advanced I/O Banks

	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.69
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

- P_{DC2} is the static power (where applicable) measured on VMV.
- P_{AC9} is the total dynamic power measured on V_{CC} and VMV.

Table 2-10 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹
Applicable to Standard Plus I/O Banks

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. PDC3 is the static power (where applicable) measured on VMV.
3. PAC10 is the total dynamic power measured on VCCI and VMV.

Power Consumption of Various Internal Resources

Table 2-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices

Parameter	Definition	Device Specific Dynamic Power (μW/MHz)			
		A3P1000	A3P250	A3P125	A3P060
PAC1	Clock contribution of a Global Rib	14.50	11.00	11.00	9.30
PAC2	Clock contribution of a Global Spine	2.48	1.58	0.81	0.81
PAC3	Clock contribution of a VersaTile row	0.81			
PAC4	Clock contribution of a VersaTile used as a sequential module	0.12			
PAC5	First contribution of a VersaTile used as a sequential module	0.07			
PAC6	Second contribution of a VersaTile used as a sequential module	0.29			
PAC7	Contribution of a VersaTile used as a combinatorial module	0.29			
PAC8	Average contribution of a routing net	0.70			
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-7 on page 2-6 .			
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-7 and Table 2-10 on page 2-8 .			
PAC11	Average contribution of a RAM block during a read operation	25.00			
PAC12	Average contribution of a RAM block during a write operation	30.00			
PAC13	Static PLL contribution	2.55 mW			
PAC14	Dynamic contribution for PLL	2.60			

Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-12 on page 2-11](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-13 on page 2-12](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-13 on page 2-12](#). The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

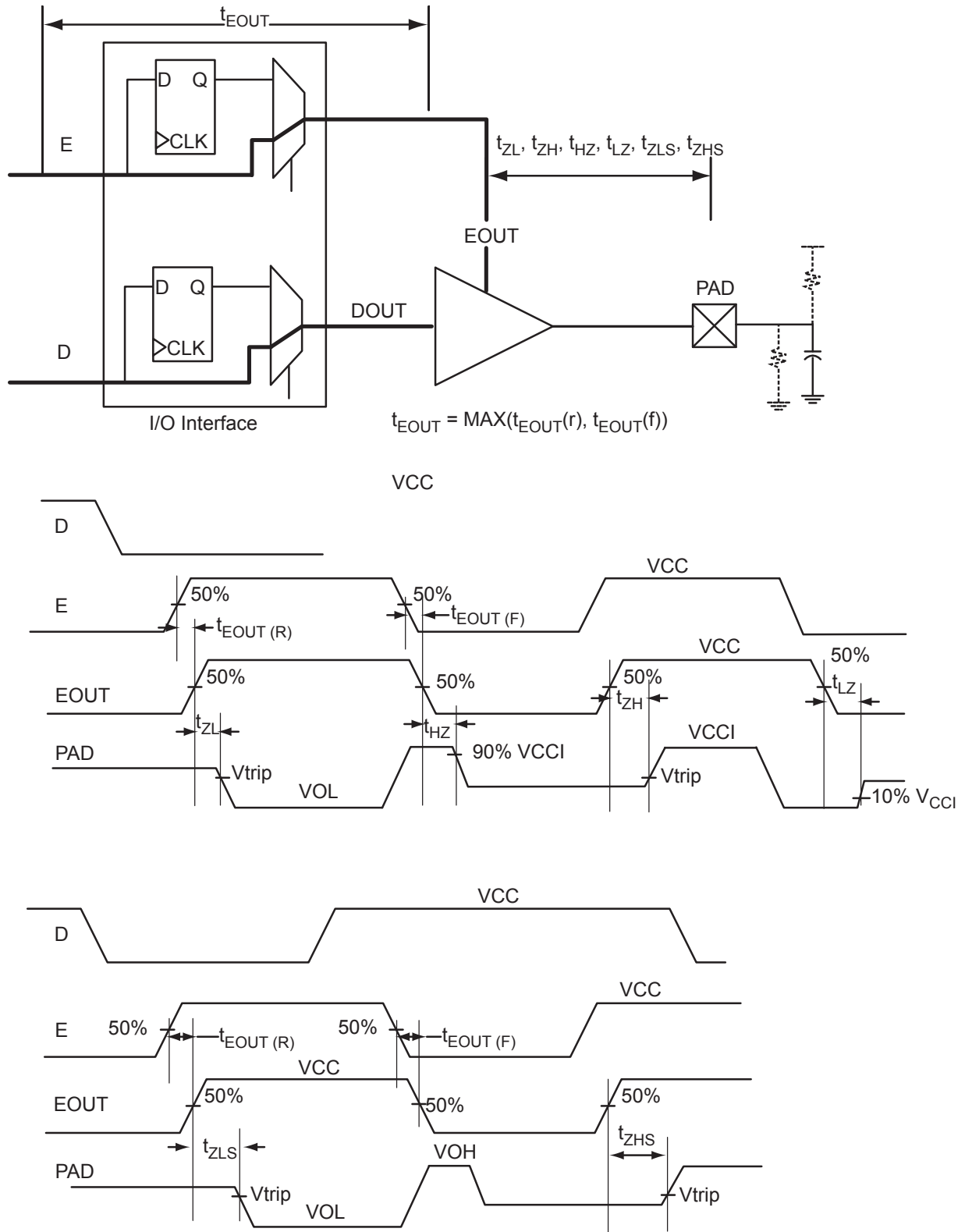


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (example)

Table 2-41 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	7.79	0.05	1.08	0.45	7.94	6.80	1.22	1.23	7.94	6.80	ns
	-1	0.55	6.85	0.04	0.95	0.39	6.98	5.98	1.26	1.27	6.98	5.98	ns
6 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
8 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
12 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns
16 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-42 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	10.47	0.05	1.08	0.45	10.66	9.11	1.22	1.16	10.66	9.11	ns
	-1	0.55	9.21	0.04	0.95	0.39	9.38	8.01	1.26	1.20	9.38	8.01	ns
6 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
8 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
12 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns
16 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-43 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	−0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	−0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	−0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	−0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-44 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max., mA ¹	Max., mA ¹	μA ²	μA ²
2 mA	−0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	−0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	−0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

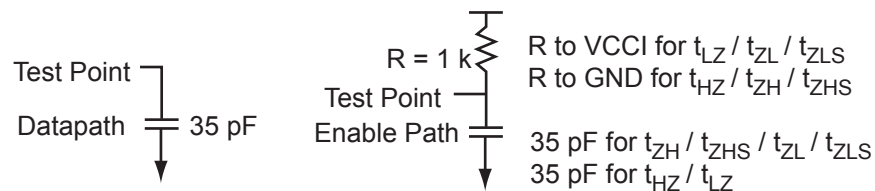


Figure 2-8 • AC Loading

Table 2-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	35

Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.

Table 2-48 • 2.5 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.26	0.05	1.45	0.46	8.28	9.26	1.24	1.12	10.78	11.756	ns
	-1	0.55	7.87	0.04	1.23	0.39	7.05	7.87	1.24	1.13	9.17	10	ns
6 mA	STD	0.64	5.43	0.05	1.45	0.46	5.19	5.43	1.43	1.47	7.69	7.926	ns
	-1	0.55	4.62	0.04	1.23	0.39	4.42	4.62	1.43	1.47	6.55	6.743	ns
12 mA	STD	0.64	3.59	0.05	1.45	0.46	3.65	3.51	1.56	1.69	6.15	6.012	ns
	-1	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.114	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-49 • 2.5 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	12.12	0.05	1.45	0.46	11.89	12.12	1.25	1.08	14.39	14.622	ns
	-1	0.55	10.31	0.04	1.23	0.39	10.12	10.31	1.25	1.08	12.24	12.438	ns
6 mA	STD	0.64	8.24	0.05	1.45	0.46	8.39	8.23	1.43	1.42	10.89	10.73	ns
	-1	0.55	7.01	0.04	1.23	0.39	7.14	7.00	1.43	1.42	9.26	9.128	ns
12 mA	STD	0.64	6.30	0.05	1.45	0.46	6.41	6.16	1.56	1.63	8.91	8.656	ns
	-1	0.55	5.35	0.04	1.23	0.39	5.45	5.24	1.56	1.63	7.58	7.364	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-64 • 1.8 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	16.80	0.05	1.40	0.45	14.60	16.01	1.20	0.77	17.02	18.43	ns
	-1	0.53	14.29	0.04	1.19	0.38	12.42	13.62	1.20	0.77	14.48	15.68	ns
4 mA	STD	0.63	11.33	0.05	1.40	0.45	10.53	10.71	1.42	1.31	12.95	13.13	ns
	-1	0.53	9.64	0.04	1.19	0.38	8.96	9.11	1.42	1.31	11.01	11.17	ns
6 mA	STD	0.63	8.71	0.05	1.40	0.45	8.19	7.92	1.57	1.57	10.61	10.34	ns
	-1	0.53	7.41	0.04	1.19	0.38	6.97	6.74	1.57	1.57	9.03	8.79	ns
8 mA	STD	0.63	8.12	0.05	1.40	0.45	8.19	7.92	1.57	1.57	10.61	10.34	ns
	-1	0.53	6.90	0.04	1.19	0.38	6.97	6.74	1.57	1.57	9.03	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-65 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA^2	μA^2
2 mA	-0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	16	13	10	10
4 mA	-0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	33	25	10	10
6 mA	-0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	39	32	10	10
8 mA	-0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	55	66	10	10
12 mA	-0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	55	66	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-95 • Output Data Register Propagation Delays
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.70	0.82	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.37	0.44	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.52	0.61	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.96	1.12	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.96	1.12	ns
t_{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.41	0.48	ns
t_{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-100 • Input DDR Propagation Delays
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.33	0.38	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.46	0.54	ns
t_{DDRISUD}	Data Setup for Input DDR	0.34	0.40	ns
t_{DDRILD}	Data Hold for Input DDR	0.00	0.00	ns
$t_{\text{DDRILR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.55	0.65	ns
$t_{\text{DDRILR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.68	0.80	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.27	0.31	ns
$t_{\text{DDRILWCLR}}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.25	0.30	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.41	0.48	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.37	0.43	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Timing Characteristics

Table 2-104 • Combinatorial Cell Propagation Delays
Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-1	Std.	Units
INV	$Y = !A$	t_{PD}	0.49	0.57	ns
AND2	$Y = A \cdot B$	t_{PD}	0.57	0.67	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.57	0.67	ns
OR2	$Y = A + B$	t_{PD}	0.59	0.69	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.59	0.69	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.90	1.05	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.85	1.00	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.06	1.25	ns
MUX2	$Y = A !S + B S$	t_{PD}	0.62	0.72	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.68	0.80	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-105 • Combinatorial Cell Propagation Delays
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-1	Std.	Units
INV	$Y = !A$	t_{PD}	0.48	0.56	ns
AND2	$Y = A \cdot B$	t_{PD}	0.56	0.66	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.56	0.66	ns
OR2	$Y = A + B$	t_{PD}	0.58	0.68	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.58	0.68	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.88	1.03	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.83	0.98	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.04	1.23	ns
MUX2	$Y = A !S + B S$	t_{PD}	0.60	0.71	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.67	0.79	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

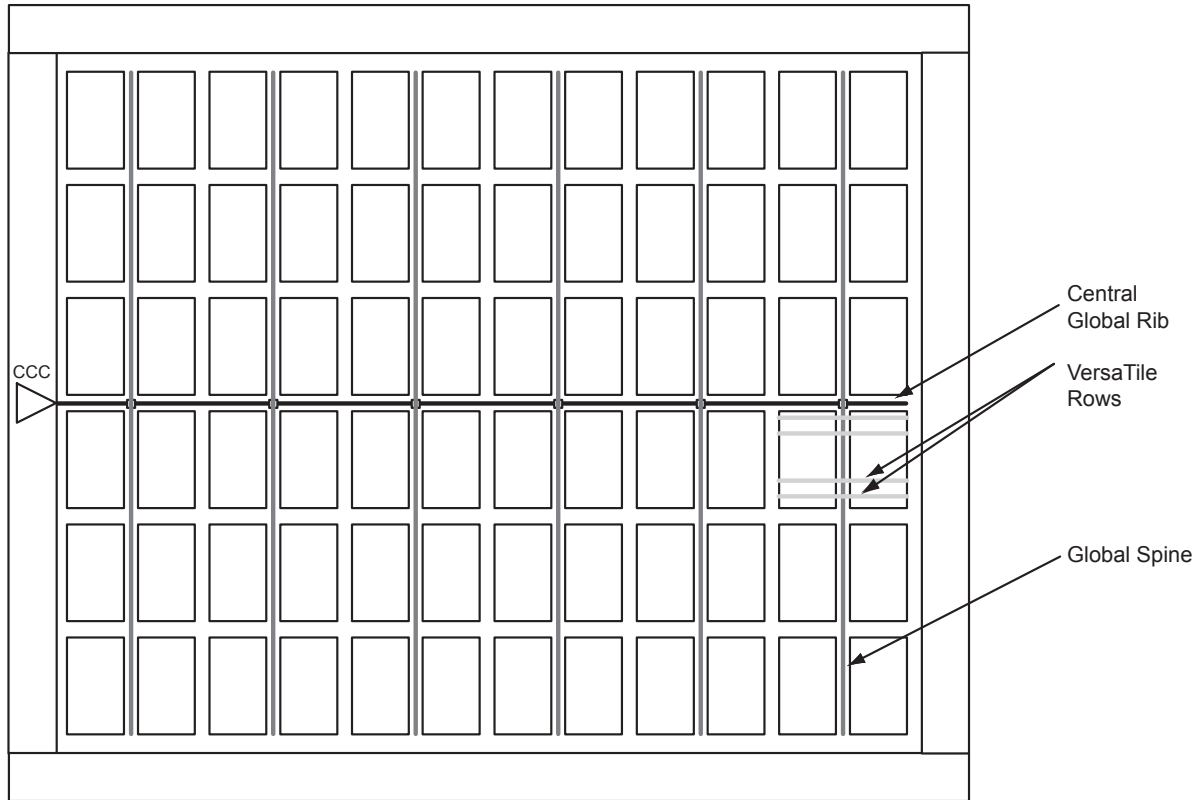


Figure 2-28 • Example of Global Tree Use in an A3P250 Device for Clock Routing

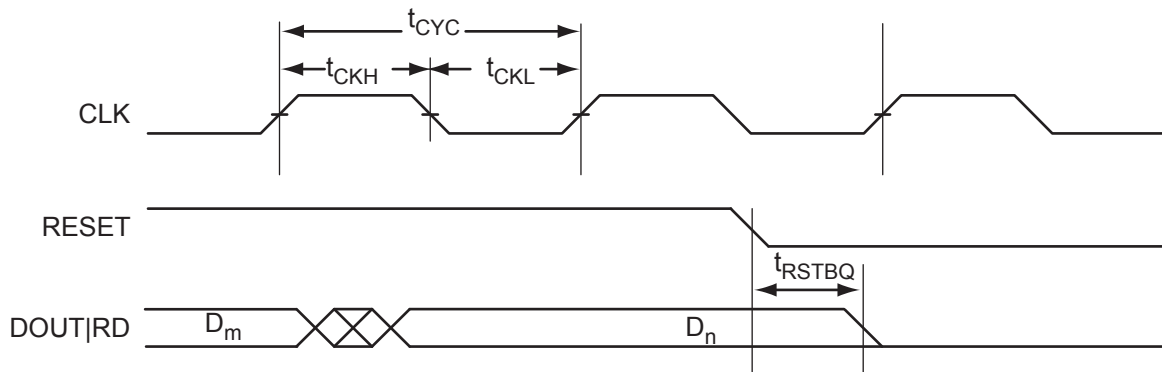


Figure 2-35 • RAM Reset. Applicable to Both RAM4K9 and RAM512x18

Timing Waveforms

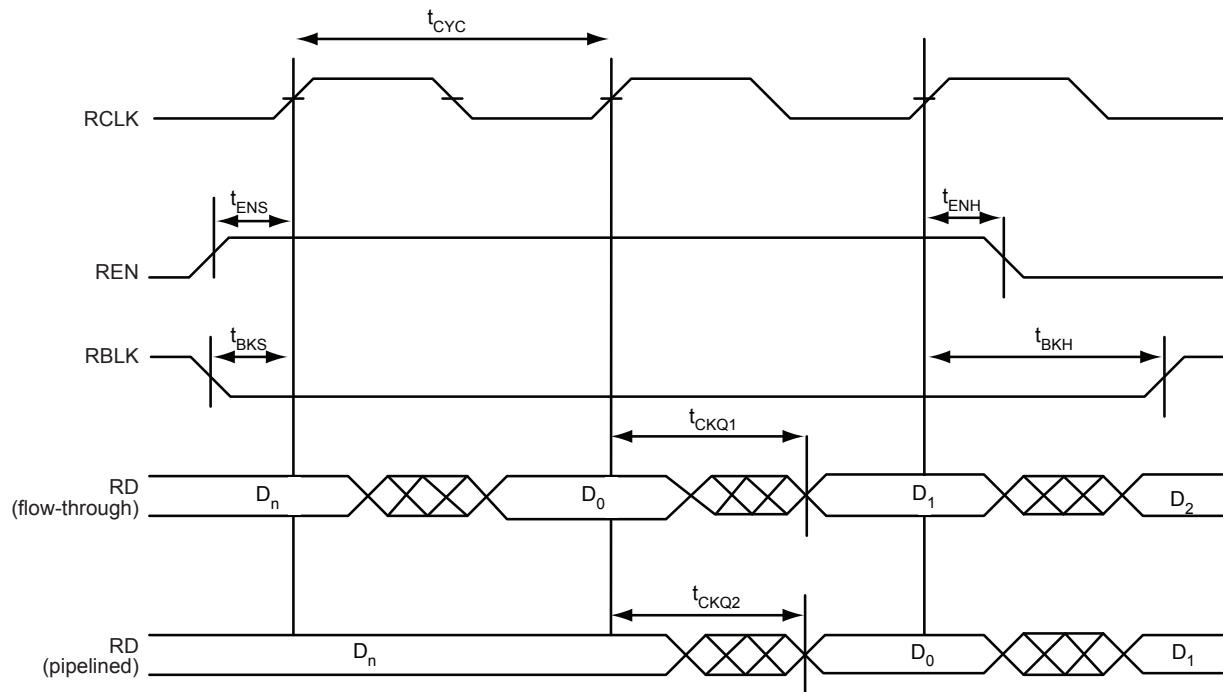


Figure 2-37 • FIFO Read

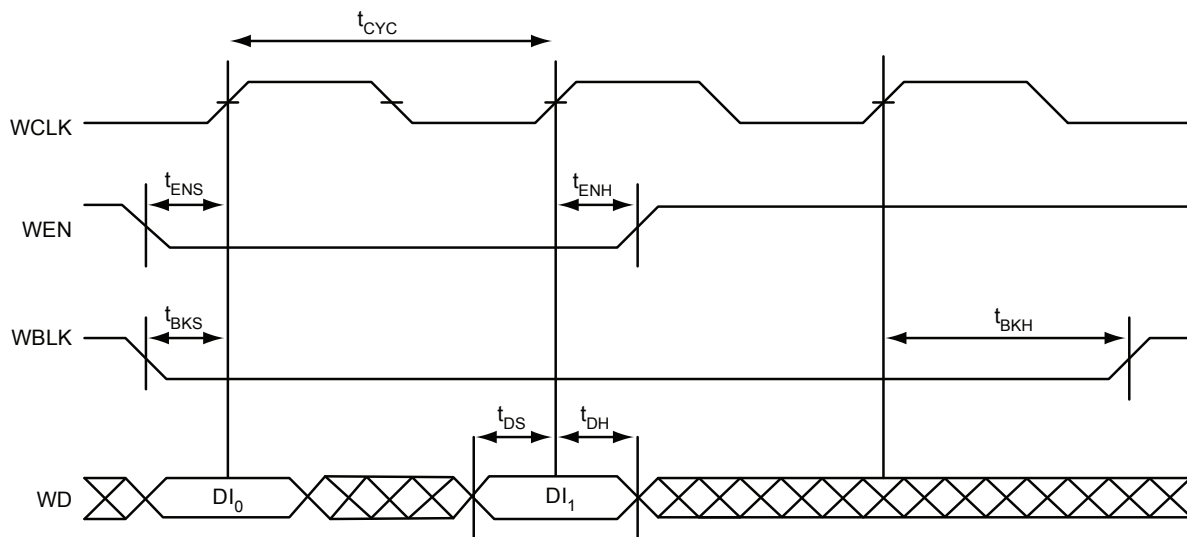
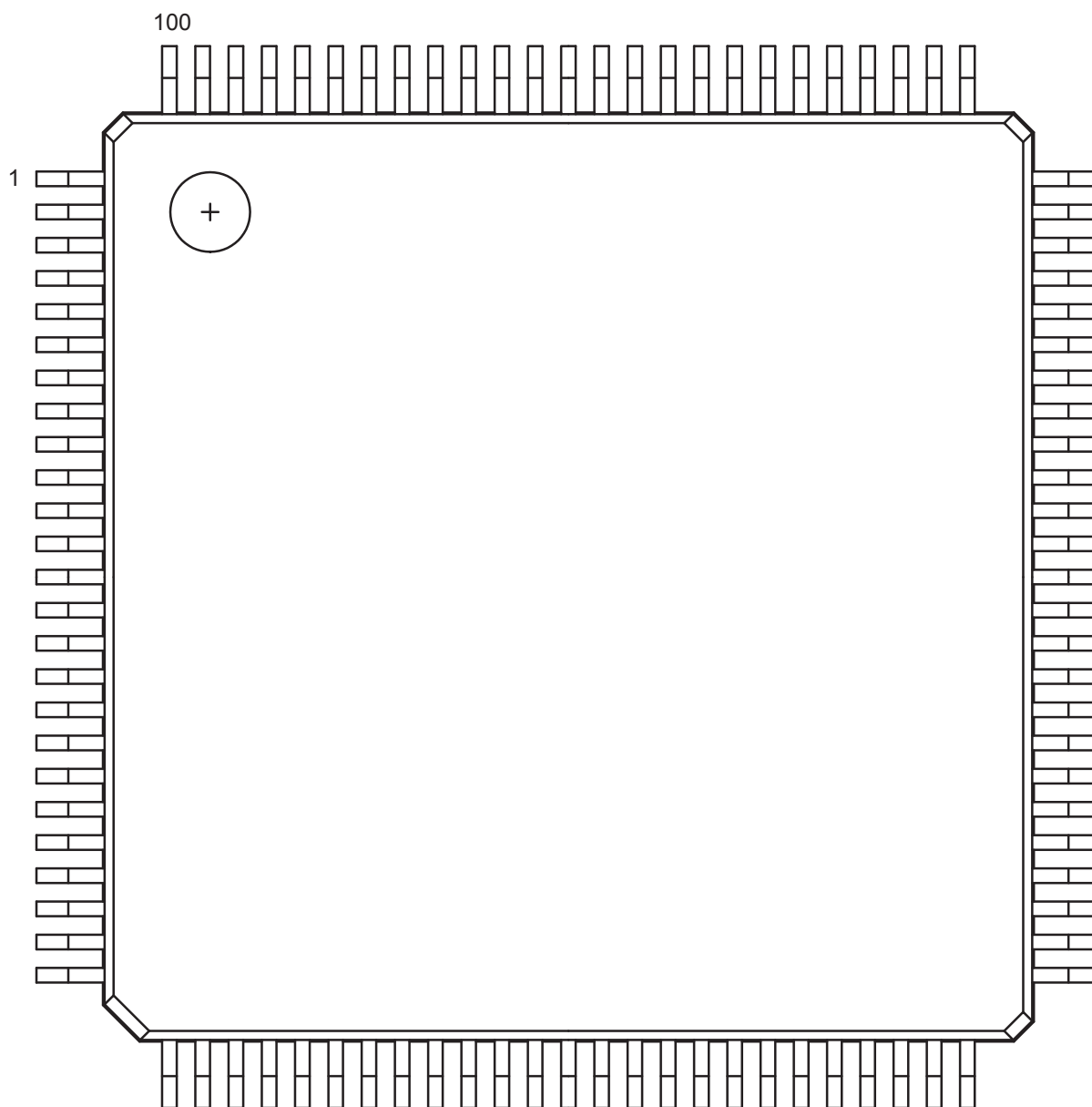


Figure 2-38 • FIFO Write

4 – Package Pin Assignments

VQ100



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

FG144		FG144		FG144	
Pin Number	A3P060 Function	Pin Number	A3P060 Function	Pin Number	A3P060 Function
A1	GNDQ	D1	IO91RSB1	G1	GFA1/IO84RSB1
A2	VMV0	D2	IO92RSB1	G2	GND
A3	GAB0/IO04RSB0	D3	IO93RSB1	G3	VCCPLF
A4	GAB1/IO05RSB0	D4	GAA2/IO51RSB1	G4	GFA0/IO85RSB1
A5	IO08RSB0	D5	GAC0/IO06RSB0	G5	GND
A6	GND	D6	GAC1/IO07RSB0	G6	GND
A7	IO11RSB0	D7	GBC0/IO19RSB0	G7	GND
A8	VCC	D8	GBC1/IO20RSB0	G8	GDC1/IO45RSB0
A9	IO16RSB0	D9	GBB2/IO27RSB0	G9	IO32RSB0
A10	GBA0/IO23RSB0	D10	IO18RSB0	G10	GCC2/IO43RSB0
A11	GBA1/IO24RSB0	D11	IO28RSB0	G11	IO31RSB0
A12	GNDQ	D12	GCB1/IO37RSB0	G12	GCB2/IO42RSB0
B1	GAB2/IO53RSB1	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO88RSB1	H2	GFB2/IO82RSB1
B3	GAA0/IO02RSB0	E3	GFC1/IO89RSB1	H3	GFC2/IO81RSB1
B4	GAA1/IO03RSB0	E4	VCCIB1	H4	GEC1/IO77RSB1
B5	IO00RSB0	E5	IO52RSB1	H5	VCC
B6	IO10RSB0	E6	VCCIB0	H6	IO34RSB0
B7	IO12RSB0	E7	VCCIB0	H7	IO44RSB0
B8	IO14RSB0	E8	GCC1/IO35RSB0	H8	GDB2/IO55RSB1
B9	GBB0/IO21RSB0	E9	VCCIB0	H9	GDC0/IO46RSB0
B10	GBB1/IO22RSB0	E10	VCC	H10	VCCIB0
B11	GND	E11	GCA0/IO40RSB0	H11	IO33RSB0
B12	VMV0	E12	IO30RSB0	H12	VCC
C1	IO95RSB1	F1	GFB0/IO86RSB1	J1	GEB1/IO75RSB1
C2	GFA2/IO83RSB1	F2	VCOMPLF	J2	IO78RSB1
C3	GAC2/IO94RSB1	F3	GFB1/IO87RSB1	J3	VCCIB1
C4	VCC	F4	IO90RSB1	J4	GEC0/IO76RSB1
C5	IO01RSB0	F5	GND	J5	IO79RSB1
C6	IO09RSB0	F6	GND	J6	IO80RSB1
C7	IO13RSB0	F7	GND	J7	VCC
C8	IO15RSB0	F8	GCC0/IO36RSB0	J8	TCK
C9	IO17RSB0	F9	GCB0/IO38RSB0	J9	GDA2/IO54RSB1
C10	GBA2/IO25RSB0	F10	GND	J10	TDO
C11	IO26RSB0	F11	GCA1/IO39RSB0	J11	GDA1/IO49RSB0
C12	GBC2/IO29RSB0	F12	GCA2/IO41RSB0	J12	GDB1/IO47RSB0



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