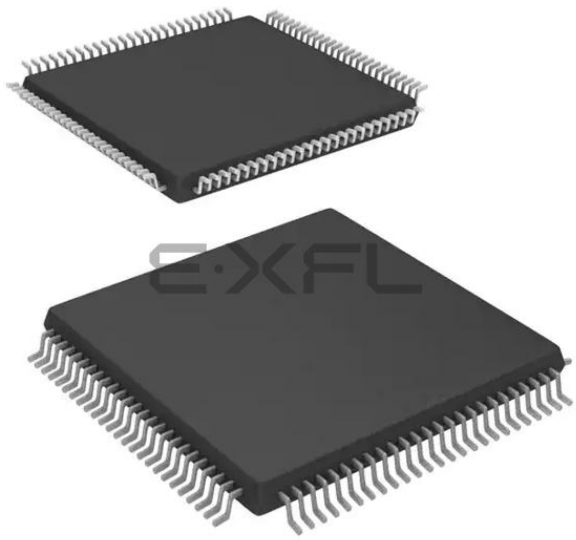


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	71
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p060-vqg100t

I/Os Per Package

ProASIC3 Devices	A3P060	A3P125	A3P250		A3P1000	
	I/O Type					
Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O 2	Differential I/O Pairs	Single-Ended I/O 2	Differential I/O Pairs
VQ100	71	71	68	13	–	–
FG144	96	97	97	24	97	25
FG256	–	–	157	38	177	44
FG484	–	–	–	–	300	74
QNG132	–	84	87	19	–	–

Notes:
1. *When considering migrating your design to a lower- or higher-density device, refer to the* ProASIC3 FPGA Fabric User's Guide *to ensure complying with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of available single-ended I/Os by two.*
3. *FG256 and FG484 are footprint-compatible packages.*

Automotive ProASIC3 Device Status

Automotive ProASIC3 Devices	Status
A3P060	Production
A3P125	Production
A3P250	Production
A3P1000	Production

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Automotive ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

The Microsemi flash-based Automotive ProASIC3 devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based Automotive ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and external clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the Automotive ProASIC3 device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based Automotive ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of Automotive ProASIC3 flash-based FPGAs. Once it is programmed, the flash cell configuration element of Automotive ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Automotive ProASIC3 devices exhibit very low power characteristics, similar to those of an ASIC, making them an ideal choice for power-sensitive applications. Automotive ProASIC3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

Automotive ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The Automotive ProASIC3 family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

User Nonvolatile FlashROM

Automotive ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Unique protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, infotainment systems)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard Automotive ProASIC3 IEEE 1532 JTAG programming interface.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

Automotive ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM

Automotive ProASIC3 devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

PLL and CCC

Automotive ProASIC3 devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the Automotive ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Table 2-3 • **Overshoot and Undershoot Limits (as measured on quiet I/Os)**

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle	Maximum Overshoot/ Undershoot (115°C)	Maximum Overshoot/ Undershoot (135°C)
2.7 V or less	10%	0.81 V	0.72 V
	5%	0.90 V	0.82 V
3 V	10%	0.80 V	0.72 V
	5%	0.90 V	0.81 V
3.3 V	10%	0.79 V	0.69 V
	5%	0.88 V	0.79 V
3.6 V	10%	N/A	N/A
	5%	N/A	N/A

Notes:

1. *The duration is allowed at one out of six clock cycles (estimated SSO density over cycles). If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
2. *This table refers only to overshoot/undershoot limits for simultaneously switching I/Os and does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-2 on page 2-4.

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-2 on page 2-4).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI T**rip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

Power Consumption of Various Internal Resources

Table 2-11 • **Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)			
		A3P1000	A3P250	A3P125	A3P060
PAC1	Clock contribution of a Global Rib	14.50	11.00	11.00	9.30
PAC2	Clock contribution of a Global Spine	2.48	1.58	0.81	0.81
PAC3	Clock contribution of a VersaTile row	0.81			
PAC4	Clock contribution of a VersaTile used as a sequential module	0.12			
PAC5	First contribution of a VersaTile used as a sequential module	0.07			
PAC6	Second contribution of a VersaTile used as a sequential module	0.29			
PAC7	Contribution of a VersaTile used as a combinatorial module	0.29			
PAC8	Average contribution of a routing net	0.70			
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-7 on page 2-6.			
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-7 and Table 2-10 on page 2-8.			
PAC11	Average contribution of a RAM block during a read operation	25.00			
PAC12	Average contribution of a RAM block during a write operation	30.00			
PAC13	Static PLL contribution	2.55 mW			
PAC14	Dynamic contribution for PLL	2.60			

*Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-12 on page 2-11.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-13 on page 2-12.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-13 on page 2-12. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

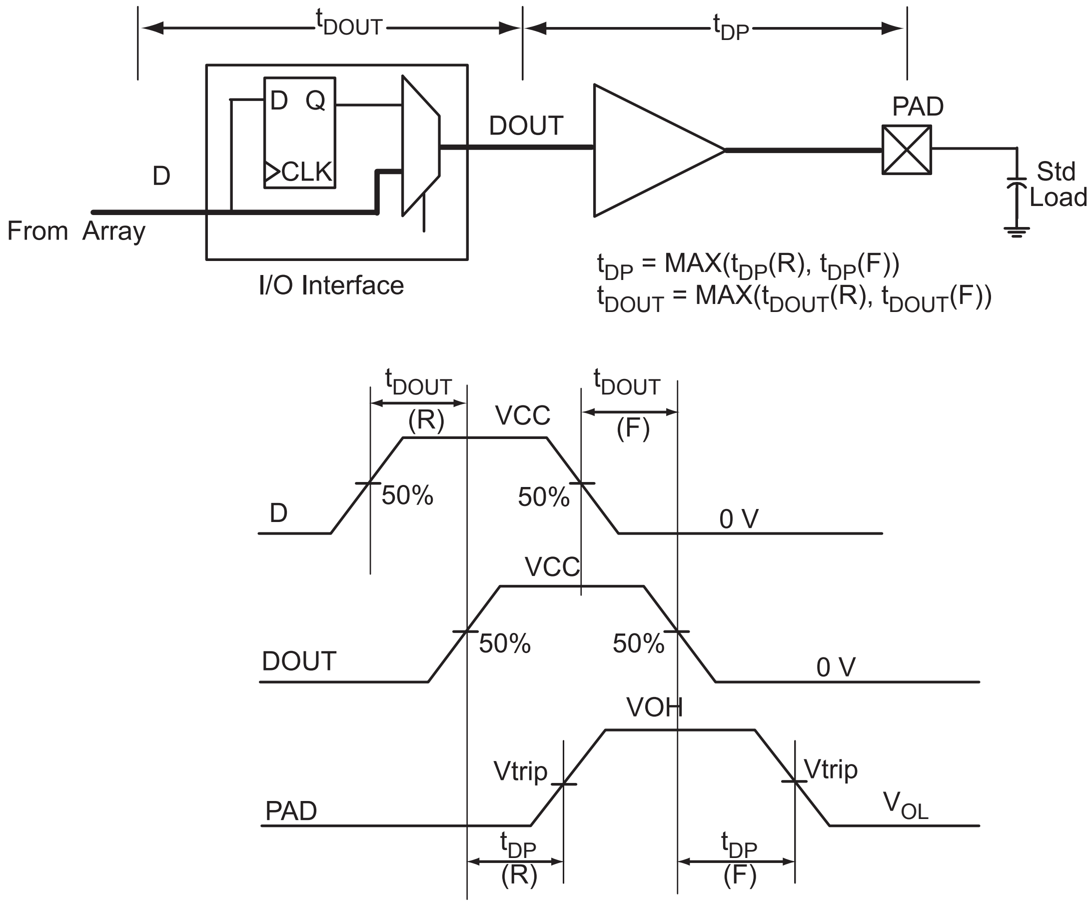


Figure 2-5 • **Output Buffer Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-14 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength	Slew Rate	VIL Min. V	VIL Max. V	VIH Min. V	VIH Max. V	VOL Max. V	VOH Min. V	I_{OL} mA	I_{OH} mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 125°C junction temperature.

Table 2-15 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Standard Plus I/O Banks**

I/O Standard	Drive Strength	Slew Rate	VIL Min. V	VIL Max. V	VIH Min. V	VIH Max. V	VOL Max. V	VOH Min. V	I_{OL} mA	I_{OH} mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	High	–0.3	0.30 * VCCI	0.7 * V_{CCI}	3.6	0.25 * VCCI	0.75 * V_{CCI}	4	4
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 125°C junction temperature.

Table 2-23 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Automotive-Case Conditions: T_J = 115°C, Worst Case VCC = 1.425 V
Worst Case VCCI = 3.0 V
Standard Plus I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.80	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.11	ns
1.8 V LVCMOS	8 mA	High	35 pF	–	0.55	3.73	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.99	ns
1.5 V LVCMOS	4 mA	High	35 pF	–	0.55	4.60	0.04	1.35	0.39	4.61	5.05	2.07	1.85	6.74	7.18	ns
3.3 V PCI	Per PCI spec	High	10 pF	25 [2]	0.55	2.55	0.04	0.82	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25 [2]	0.55	2.55	0.04	0.79	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-48 for connectivity. This resistor is not required during normal operation.*

Table 2-73 • 1.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.83	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.76	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.83	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	9.21	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns
6 mA	STD	0.63	10.10	0.05	1.40	0.45	10.28	9.62	2.05	1.80	12.70	12.04	ns
	-1	0.53	8.59	0.04	1.19	0.38	8.75	8.18	2.05	1.80	10.81	10.24	ns
8 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns
12 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-74 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	8.47	0.05	1.54	0.45	7.38	9.05	1.81	1.45	9.80	11.47	ns
	-1	0.53	7.21	0.04	1.31	0.38	6.28	7.70	1.81	1.45	8.34	9.75	ns
4 mA	STD	0.63	5.24	0.05	1.54	0.45	5.25	5.75	2.00	1.78	7.67	8.17	ns
	-1	0.53	4.45	0.04	1.31	0.38	4.46	4.89	2.00	1.78	6.52	6.95	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-75 • 1.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.07	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.12	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.04	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	8.54	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-80 • 3.3 V PCI/PCI-X
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.628	2.50	0.05	0.92	0.45	1.23	0.91	3.02	3.48	2.40	2.11	ns
–1	0.53	2.12	0.04	0.78	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-81 • 3.3 V PCI/PCI-X
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.628	2.90	0.05	0.90	0.45	1.23	0.91	3.02	3.48	2.40	2.11	ns
–1	0.53	2.47	0.04	0.77	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12 on page 2-50. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

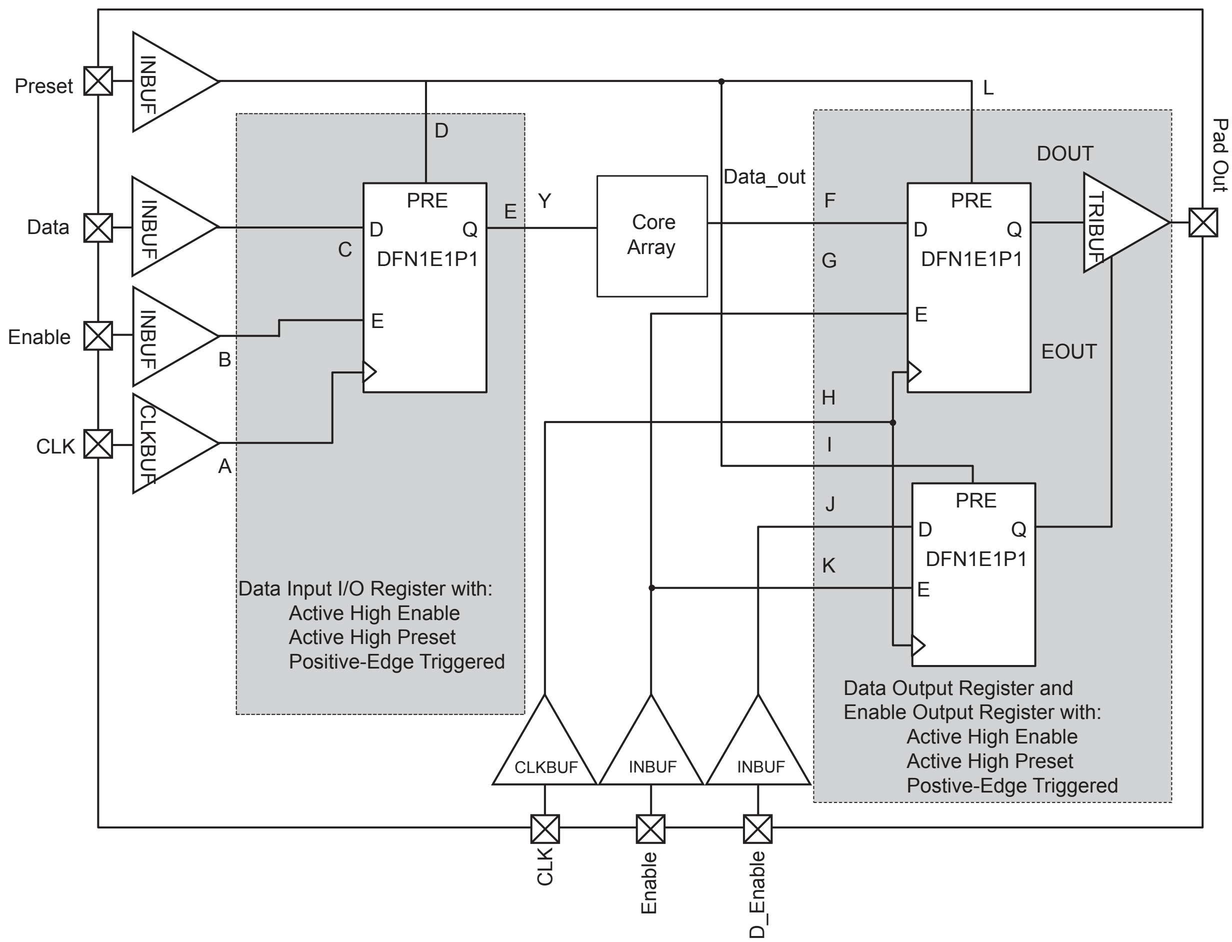


Figure 2-15 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

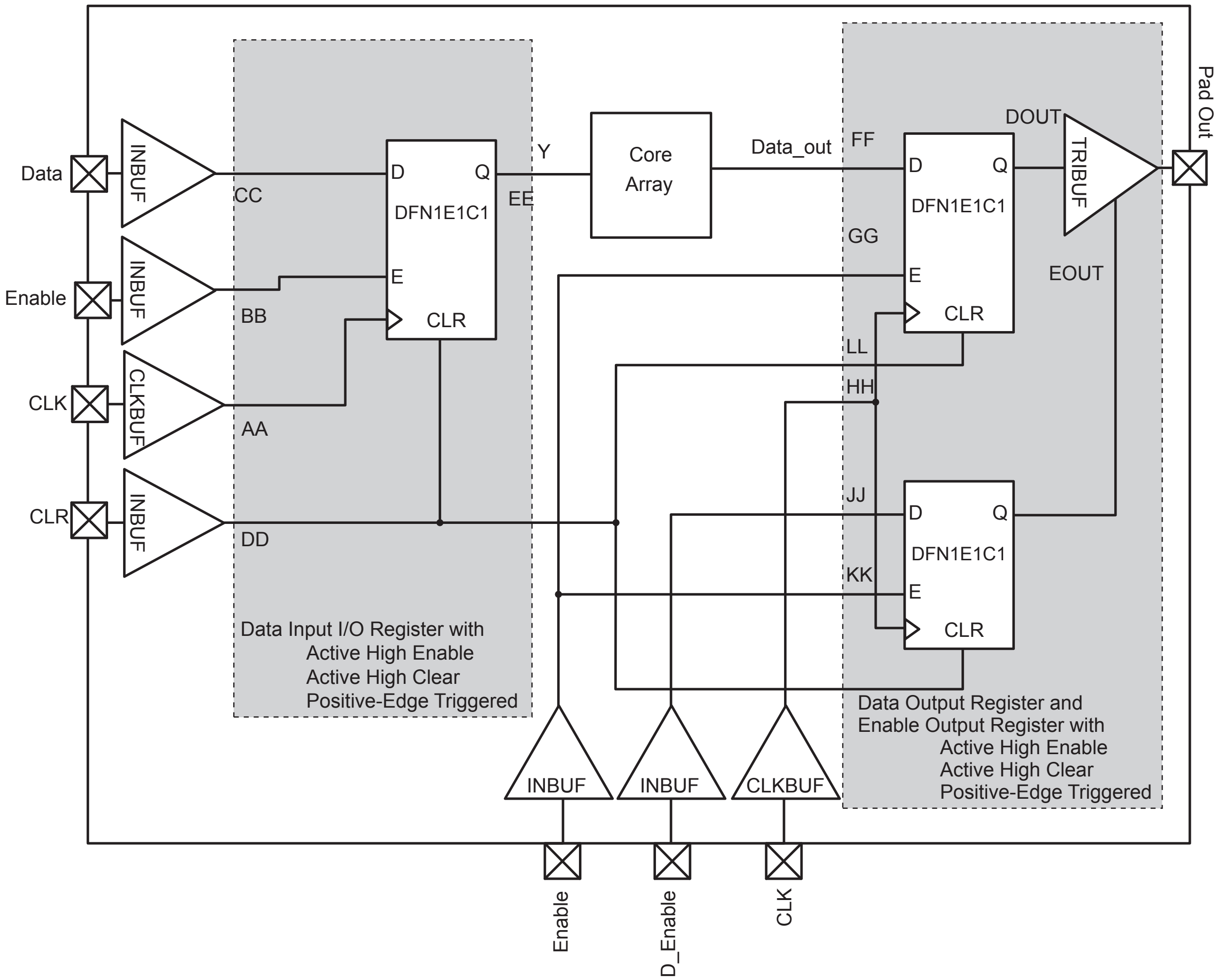


Figure 2-16 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Output DDR Module

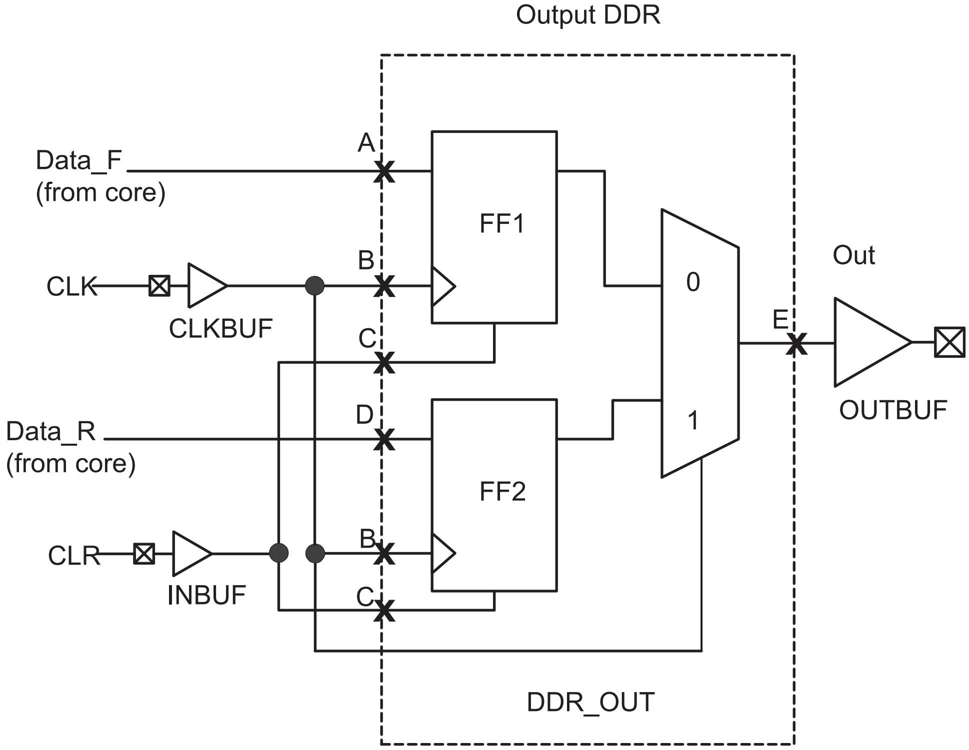


Figure 2-22 **• Output DDR Timing Model**

Table 2-101 **• Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

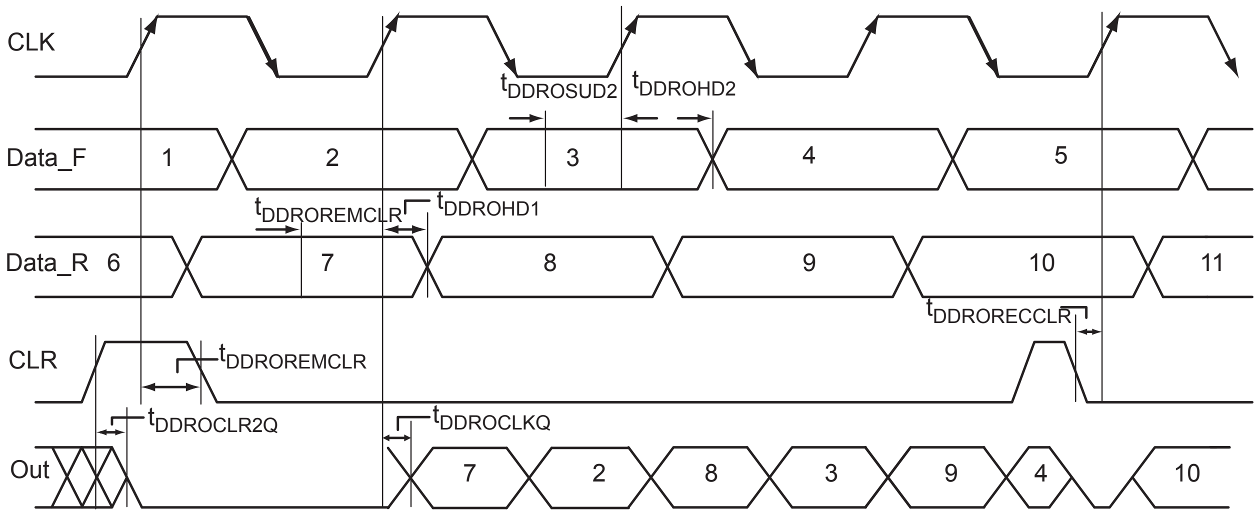


Figure 2-23 • **Output DDR Timing Diagram**

Timing Characteristics

Table 2-102 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.85	1.00	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.46	0.54	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.46	0.54	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.97	1.15	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.27	0.32	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.37	0.43	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Timing Characteristics

***Table 2-104* • Combinatorial Cell Propagation Delays**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.49	0.57	ns
AND2	Y = A · B	t_{PD}	0.57	0.67	ns
NAND2	Y = !(A · B)	t_{PD}	0.57	0.67	ns
OR2	Y = A + B	t_{PD}	0.59	0.69	ns
NOR2	Y = !(A + B)	t_{PD}	0.59	0.69	ns
XOR2	Y = A ⊕ B	t_{PD}	0.90	1.05	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.85	1.00	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.06	1.25	ns
MUX2	Y = A !S + B S	t_{PD}	0.62	0.72	ns
AND3	Y = A · B · C	t_{PD}	0.68	0.80	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

***Table 2-105* • Combinatorial Cell Propagation Delays**
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.48	0.56	ns
AND2	Y = A · B	t_{PD}	0.56	0.66	ns
NAND2	Y = !(A · B)	t_{PD}	0.56	0.66	ns
OR2	Y = A + B	t_{PD}	0.58	0.68	ns
NOR2	Y = !(A + B)	t_{PD}	0.58	0.68	ns
XOR2	Y = A ⊕ B	t_{PD}	0.88	1.03	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.83	0.98	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.04	1.23	ns
MUX2	Y = A !S + B S	t_{PD}	0.60	0.71	ns
AND3	Y = A · B · C	t_{PD}	0.67	0.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

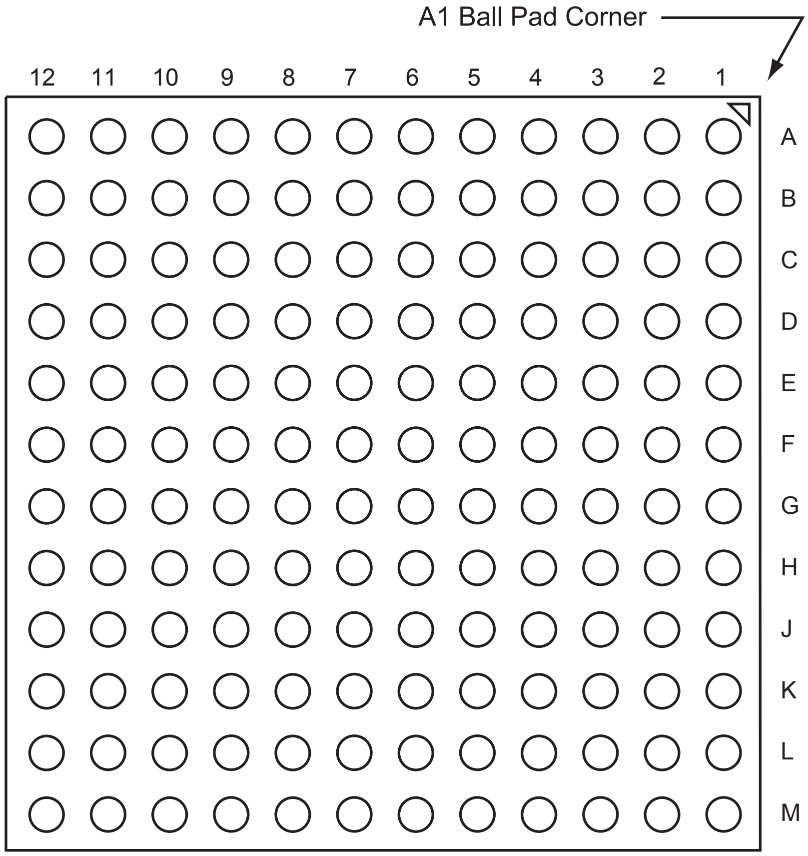
***Table 2-118* • RAM512X18**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.35	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN, WEN Setup Time	0.11	0.13	ns
t_{ENH}	REN, WEN Hold Time	0.07	0.08	ns
t_{DS}	Input data (WD) Setup Time	0.22	0.26	ns
t_{DH}	Input data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (output retained)	2.58	3.03	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.07	1.26	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.43	0.50	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.50	0.59	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.10	1.29	ns
	RESET Low to Data Out Low on RD (pipelined)	1.10	1.29	ns
$t_{REMRSTB}$	RESET Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET Recovery	1.79	2.10	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.25	0.30	ns
t_{CYC}	Clock Cycle Time	3.85	4.53	ns
F_{MAX}	Maximum Frequency	255	217	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to* *Table 2-5 on page 2-5* *for derating values.*

FG144



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

FG256	
Pin Number	A3P250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117UDB3
B2	GAA2/IO118UDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117VDB3
C2	IO118VDB3
C3	NC
C4	NC

FG256	
Pin Number	A3P250 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114VDB3
D2	IO114UDB3
D3	GAC2/IO116UDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116VDB3
E4	IO115UDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO19RSB0

FG256	
Pin Number	A3P250 Function
E9	IO24RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115VDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

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