Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fg256t

Automotive ProASIC3 Ordering Information

A3P1000 – 1 FG G 144 Y T

- **Part Number**
  - **Automotive ProASIC3 Devices**
    - A3P060 = 60,000 System Gates
    - A3P125 = 125,000 System Gates
    - A3P250 = 250,000 System Gates
    - A3P1000 = 1,000,000 System Gates
- **Speed Grade**
  - Blank = Standard
  - 1 = 15% Faster than Standard
- **Package Type**
  - VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
  - FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
  - QN = Quad Flat Pack (0.5 mm pitch)
- **Lead-Free Packaging**
  - Blank = Standard Packaging
  - G = RoHS-Compliant (Green) Packaging
- **Package Lead Count**
- **Security Feature**
  - Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
  - Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

LICENSED DPA COUNTERMEASURES

- **Application (Temperature Range)**
  - T = Grade 2 and Grade 1 AEC-Q100
    Grade 2 = 105°C T_A and 115°C T_J[1]
    Grade 1 = 125°C T_A and 135°C T_J[1]

Notes:

1. *T_A = Ambient temperature and T_J = Junction temperature.*
2. *Minimum order quantities apply. Contact your local Microsemi SoC Products Group sales office for details.*

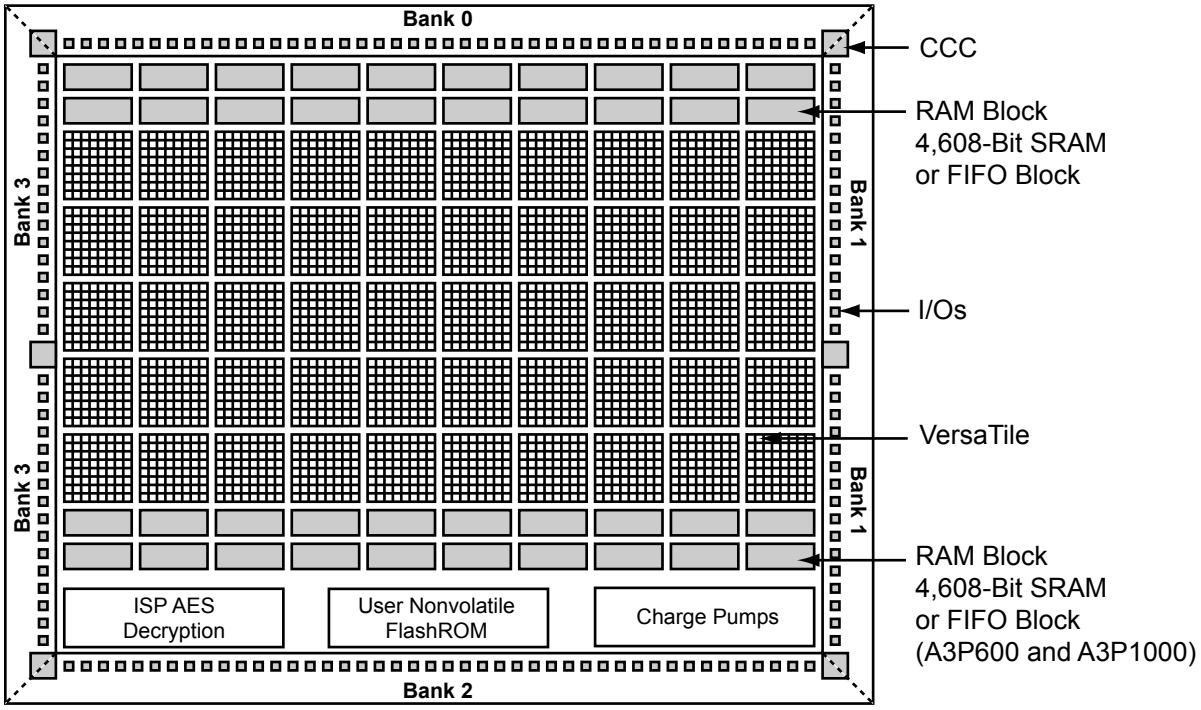


Figure 1-2 • **Automotive ProASIC3 Device Architecture Overview with Four I/O Banks (A3P600 and A3P1000)**

VersaTiles

The Automotive ProASIC3 core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The Automotive ProASIC3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-3 for VersaTile configurations.

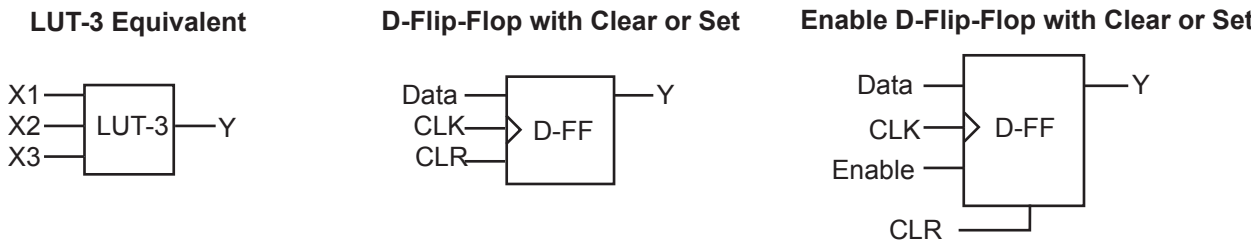


Figure 1-3 • **VersaTile Configurations**

User Nonvolatile FlashROM

Automotive ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Unique protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, infotainment systems)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard Automotive ProASIC3 IEEE 1532 JTAG programming interface.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

Automotive ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM

Automotive ProASIC3 devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

PLL and CCC

Automotive ProASIC3 devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the Automotive ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-13 on page 2-12.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-13 on page 2-12.

PLL Contribution—P_{PLL}

$$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-12 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Detailed I/O DC Characteristics

Table 2-24 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-25 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to Advanced I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	6 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / I_{OLspec}*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / I_{OHspec}*

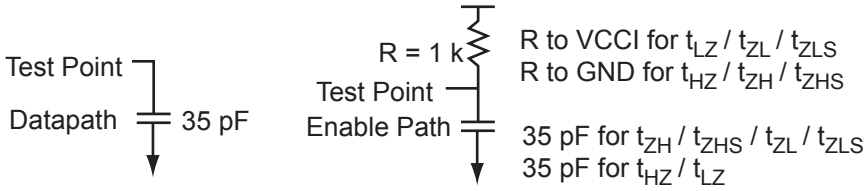


Figure 2-7 • **AC Loading**

Table 2-34 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	35

*Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.*

Table 2-62 • 1.8 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	16.80	0.05	1.40	0.45	15.27	16.80	1.48	0.84	17.69	19.22	ns
	-1	0.53	14.29	0.04	1.19	0.38	12.99	14.29	1.49	0.84	15.05	16.35	ns
4 mA	STD	0.63	11.33	0.05	1.40	0.45	11.26	11.33	1.73	1.43	13.68	13.75	ns
	-1	0.53	9.64	0.04	1.19	0.38	9.58	9.64	1.73	1.43	11.64	11.70	ns
6 mA	STD	0.63	8.71	0.05	1.40	0.45	8.87	8.48	1.89	1.72	11.29	10.90	ns
	-1	0.53	7.41	0.04	1.19	0.38	7.54	7.22	1.89	1.72	9.60	9.27	ns
8 mA	STD	0.63	8.12	0.05	1.40	0.45	8.27	7.89	1.93	1.79	10.69	10.31	ns
	-1	0.53	6.90	0.04	1.19	0.38	7.03	6.72	1.93	1.79	9.09	8.77	ns
12 mA	STD	0.63	7.89	0.05	1.40	0.45	7.83	7.89	1.98	2.07	10.25	10.31	ns
	-1	0.53	6.71	0.04	1.19	0.38	6.66	6.71	1.98	2.07	8.72	8.77	ns
16 mA	STD	0.63	7.89	0.05	1.40	0.45	7.83	7.89	1.98	2.07	10.25	10.31	ns
	-1	0.53	6.71	0.04	1.19	0.38	6.66	6.71	1.98	2.07	8.72	8.77	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-63 • 1.8 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	12.83	0.05	1.32	0.45	9.44	12.26	1.20	0.80	11.86	14.68	ns
	-1	0.53	10.92	0.04	1.12	0.38	8.03	10.43	1.20	0.80	10.09	12.49	ns
4 mA	STD	0.63	7.48	0.05	1.32	0.45	5.93	7.01	1.41	1.36	8.35	9.43	ns
	-1	0.53	6.36	0.04	1.12	0.38	5.04	5.97	1.42	1.37	7.10	8.02	ns
6 mA	STD	0.63	4.81	0.05	1.32	0.45	4.15	4.39	1.57	1.63	6.57	6.81	ns
	-1	0.53	4.09	0.04	1.12	0.38	3.53	3.74	1.57	1.63	5.59	5.79	ns
8 mA	STD	0.63	4.25	0.05	1.32	0.45	4.15	4.39	1.57	1.63	6.57	6.81	ns
	-1	0.53	3.61	0.04	1.12	0.38	3.53	3.74	1.57	1.63	5.59	5.79	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-64 • 1.8 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	16.80	0.05	1.40	0.45	14.60	16.01	1.20	0.77	17.02	18.43	ns
	-1	0.53	14.29	0.04	1.19	0.38	12.42	13.62	1.20	0.77	14.48	15.68	ns
4 mA	STD	0.63	11.33	0.05	1.40	0.45	10.53	10.71	1.42	1.31	12.95	13.13	ns
	-1	0.53	9.64	0.04	1.19	0.38	8.96	9.11	1.42	1.31	11.01	11.17	ns
6 mA	STD	0.63	8.71	0.05	1.40	0.45	8.19	7.92	1.57	1.57	10.61	10.34	ns
	-1	0.53	7.41	0.04	1.19	0.38	6.97	6.74	1.57	1.57	9.03	8.79	ns
8 mA	STD	0.63	8.12	0.05	1.40	0.45	8.19	7.92	1.57	1.57	10.61	10.34	ns
	-1	0.53	6.90	0.04	1.19	0.38	6.97	6.74	1.57	1.57	9.03	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-65 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	–0.3	0.30 * VCCI	0.7 * V_{CCI}	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * V_{CCI}	12	12	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Timing Characteristics

Table 2-68 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.35	0.05	1.61	0.46	7.63	9.35	1.87	1.50	10.13	11.851	ns
	-1	0.55	7.95	0.04	1.37	0.39	6.49	7.95	1.87	1.50	8.62	10.081	ns
4 mA	STD	0.64	5.94	0.05	1.61	0.46	5.42	5.94	2.07	1.84	7.92	8.442	ns
	-1	0.55	5.05	0.04	1.37	0.39	4.61	5.05	2.07	1.85	6.74	7.181	ns
6 mA	STD	0.64	5.22	0.05	1.61	0.46	5.09	5.22	2.11	1.93	7.59	7.718	ns
	-1	0.55	4.44	0.04	1.37	0.39	4.33	4.44	2.11	1.93	6.45	6.566	ns
8 mA	STD	0.64	4.56	0.05	1.61	0.46	2.25	1.98	4.41	4.70	3.46	3.211	ns
	-1	0.55	3.88	0.04	1.37	0.39	2.25	1.98	3.75	4.00	3.46	3.213	ns
12 mA	STD	0.64	4.56	0.05	1.61	0.46	2.25	1.98	4.41	4.70	3.46	3.211	ns
	-1	0.55	3.88	0.04	1.37	0.39	2.25	1.98	3.75	4.00	3.46	3.213	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-69 • 1.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	14.29	0.05	1.45	0.46	14.32	14.29	1.88	1.43	16.82	16.794	ns
	-1	0.55	12.16	0.04	1.23	0.39	12.18	12.16	1.88	1.43	14.31	14.286	ns
4 mA	STD	0.64	11.19	0.05	1.45	0.46	11.40	10.67	2.07	1.77	13.90	13.175	ns
	-1	0.55	9.52	0.04	1.23	0.39	9.70	9.08	2.07	1.77	11.82	11.207	ns
6 mA	STD	0.64	10.44	0.05	1.45	0.46	10.63	9.94	2.12	1.86	13.13	12.442	ns
	-1	0.55	8.88	0.04	1.23	0.39	9.04	8.46	2.12	1.86	11.17	10.584	ns
8 mA	STD	0.64	9.96	0.05	1.45	0.46	10.15	9.94	2.18	2.19	12.65	12.445	ns
	-1	0.55	8.47	0.04	1.23	0.39	8.63	8.46	2.19	2.20	10.76	10.586	ns
12 mA	STD	0.64	9.96	0.05	1.45	0.46	10.15	9.94	2.18	2.19	12.65	12.445	ns
	-1	0.55	8.47	0.04	1.23	0.39	8.63	8.46	2.19	2.20	10.76	10.586	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-70 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	8.76	0.05	1.59	0.46	7.63	9.35	1.87	1.50	10.13	11.851	ns
	-1	0.55	7.45	0.04	1.35	0.39	6.49	7.95	1.87	1.50	8.62	10.081	ns
4 mA	STD	0.64	5.41	0.05	1.59	0.46	5.42	5.94	2.07	1.84	7.92	8.442	ns
	-1	0.55	4.60	0.04	1.35	0.39	4.61	5.05	2.07	1.85	6.74	7.181	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-71 • 1.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.51	0.05	1.45	0.46	14.32	14.29	1.88	1.43	16.82	16.794	ns
	-1	0.55	11.49	0.04	1.23	0.39	12.18	12.16	1.88	1.43	14.31	14.286	ns
4 mA	STD	0.64	10.38	0.05	1.45	0.46	11.40	10.67	2.07	1.77	13.90	13.175	ns
	-1	0.55	8.83	0.04	1.23	0.39	9.70	9.08	2.07	1.77	11.82	11.207	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-72 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	9.05	0.05	1.56	0.45	7.38	9.05	1.81	1.45	9.80	11.47	ns
	-1	0.53	7.70	0.04	1.32	0.38	6.28	7.70	1.81	1.45	8.34	9.75	ns
4 mA	STD	0.63	5.75	0.05	1.56	0.45	5.25	5.75	2.00	1.78	7.67	8.17	ns
	-1	0.53	4.89	0.04	1.32	0.38	4.46	4.89	2.00	1.78	6.52	6.95	ns
6 mA	STD	0.63	5.05	0.05	1.56	0.45	4.92	5.05	2.04	1.87	7.34	7.47	ns
	-1	0.53	4.29	0.04	1.32	0.38	4.19	4.29	2.04	1.87	6.24	6.35	ns
8 mA	STD	0.63	4.41	0.05	1.56	0.45	2.18	1.91	4.27	4.55	3.35	3.11	ns
	-1	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns
12 mA	STD	0.63	4.41	0.05	1.56	0.45	2.18	1.91	4.27	4.55	3.35	3.11	ns
	-1	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

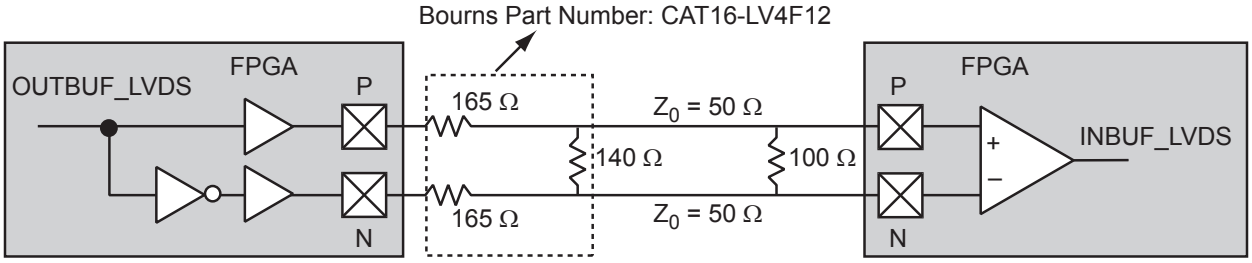


Figure 2-12 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 2-82 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
VI	Input Voltage	0	–	2.925	V
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common-Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common-Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350	–	mV

Table 2-83 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

*Note: *Measuring point = Vtrip. See Table 2-18 on page 2-17 for a complete table of trip points.*

Timing Characteristics

Table 2-84 • **LVDS**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.64	2.05	0.05	1.79	ns
–1	0.55	1.74	0.04	1.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-85 • **LVDS**
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.63	1.98	0.05	1.73	ns
–1	0.53	1.68	0.04	1.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-95 • Output Data Register Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.70	0.82	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.37	0.44	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.52	0.61	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.96	1.12	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.96	1.12	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Output DDR Module

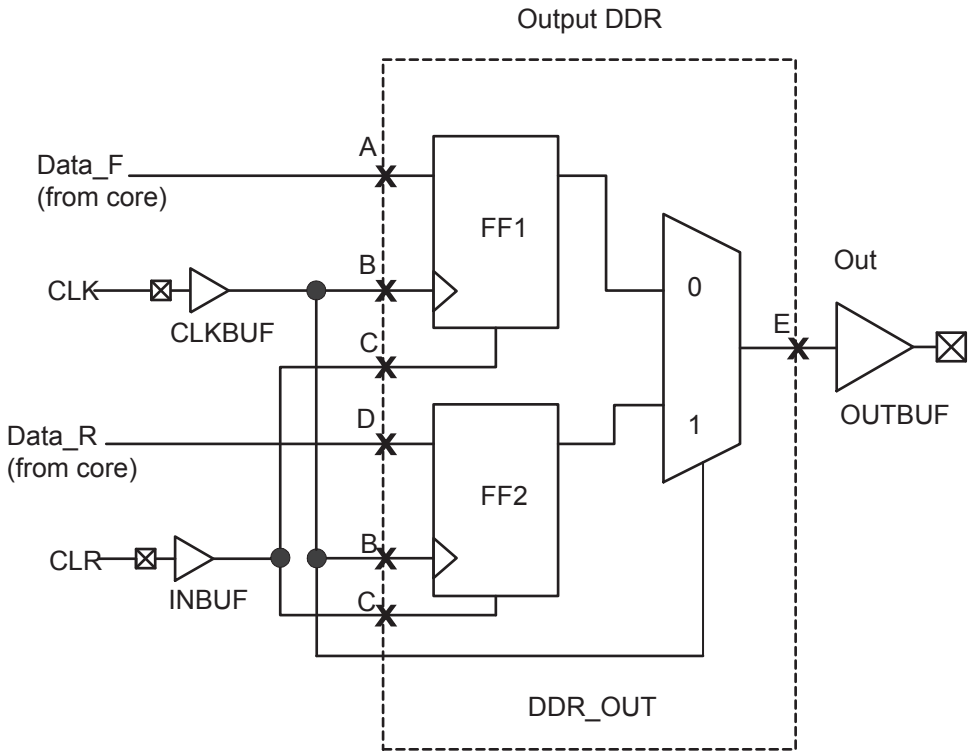


Figure 2-22 • **Output DDR Timing Model**

Table 2-101 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

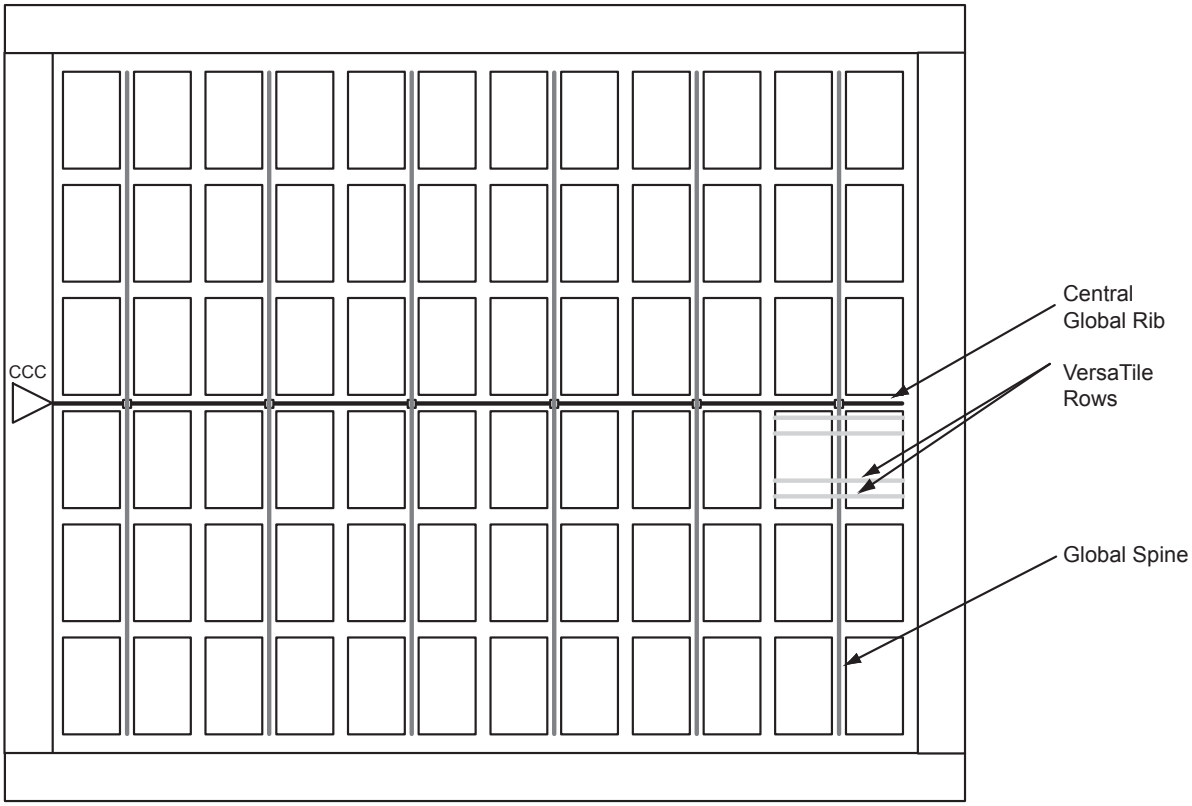


Figure 2-28 • **Example of Global Tree Use in an A3P250 Device for Clock Routing**

FIFO

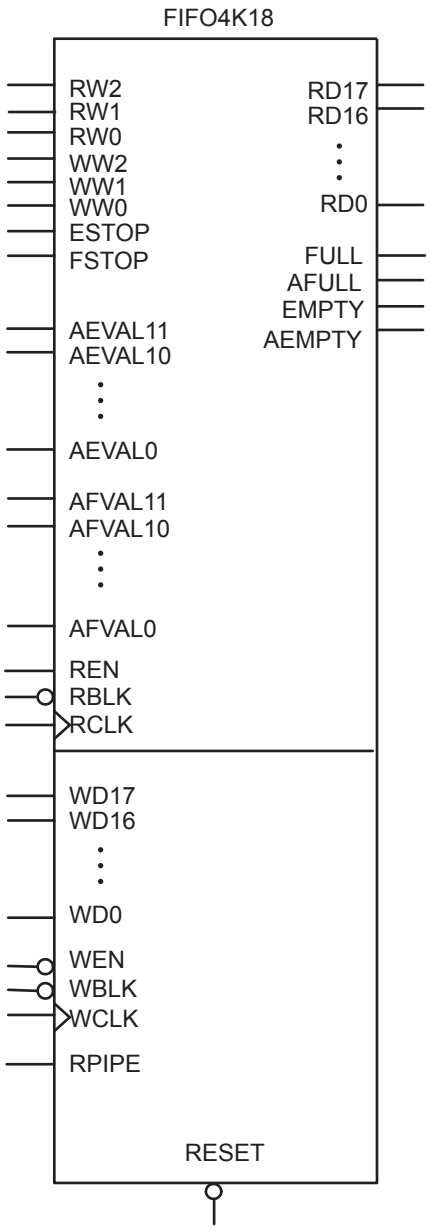


Figure 2-36 • **FIFO Model**

Timing Waveforms

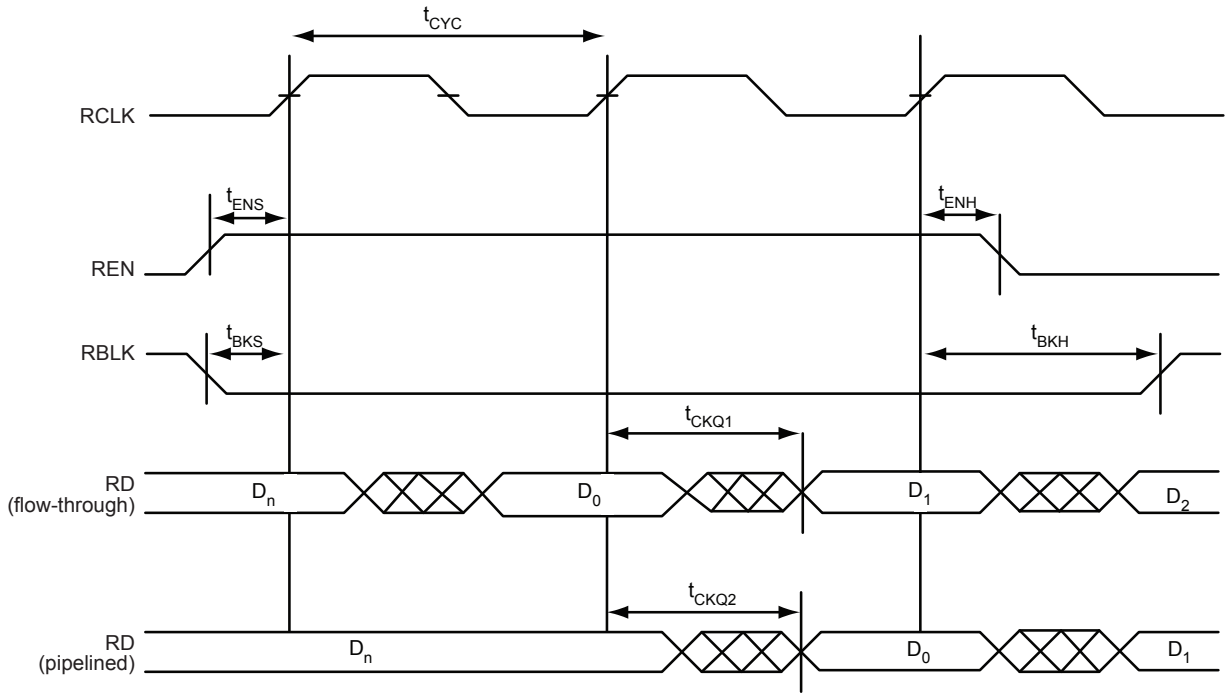


Figure 2-37 • FIFO Read

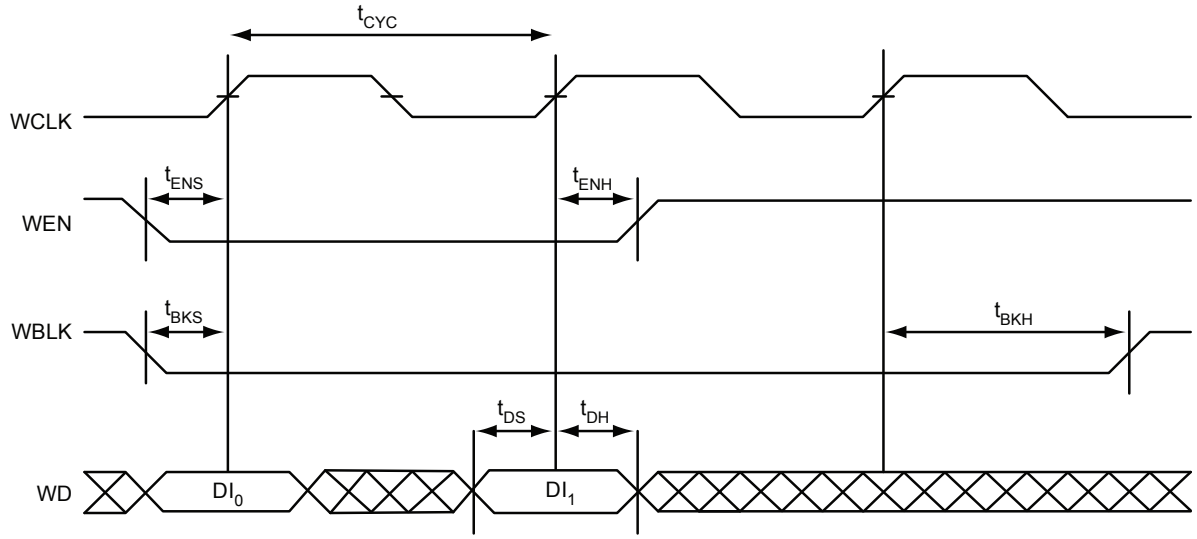
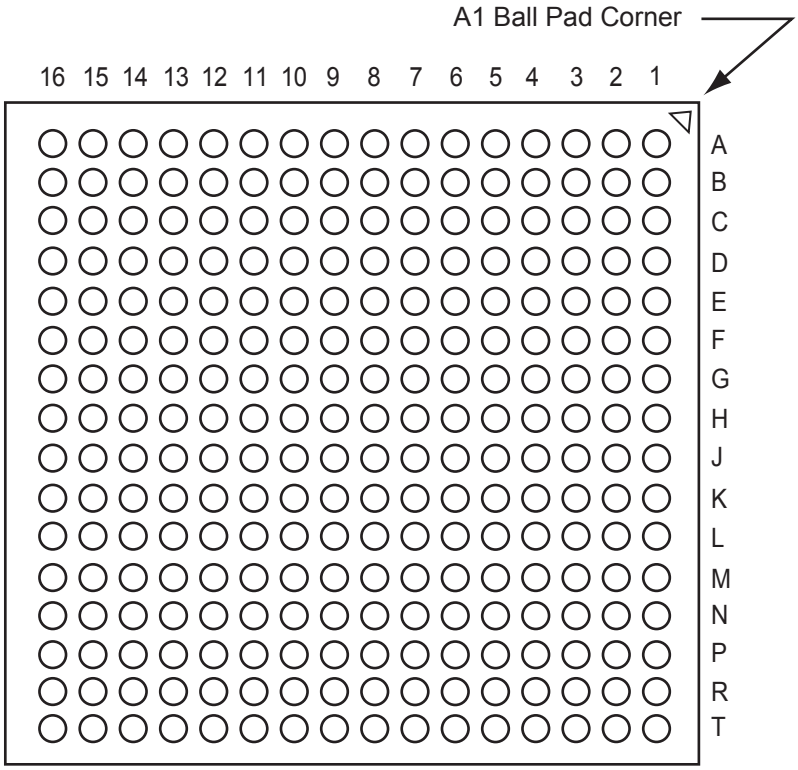


Figure 2-38 • FIFO Write

FG144	
Pin Number	A3P250 Function
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	GEB2/IO96RSB2
L4	IO91RSB2
L5	VCCIB2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG256



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

FG256	
Pin Number	A3P250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117UDB3
B2	GAA2/IO118UDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117VDB3
C2	IO118VDB3
C3	NC
C4	NC

FG256	
Pin Number	A3P250 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114VDB3
D2	IO114UDB3
D3	GAC2/IO116UDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116VDB3
E4	IO115UDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO19RSB0

FG256	
Pin Number	A3P250 Function
E9	IO24RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115VDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

Revision	Changes	Page
Revision 2 (continued)	The "Pin Descriptions and Packaging" chapter has been added (SAR 34767),	3-1
	The "VQ100" pin table for A3P125 has been added (SAR 37944).	4-3
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34767).	4-1
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Automotive ProASIC3 Device Status" table on page II indicates the status for each device in the device family.	N/A

Revision	Changes	Page
Revision 1 (Dec 2009) Product Brief v1.1	The QNG132 package was added to the "Automotive ProASIC3 Product Family" table, "I/Os Per Package" table, "Automotive ProASIC3 Ordering Information", and "Temperature Grade Offerings".	I – IV
Packaging v1.1	Pin tables for A3P125 and A3P250 were added for the "QN132" package.	4-6