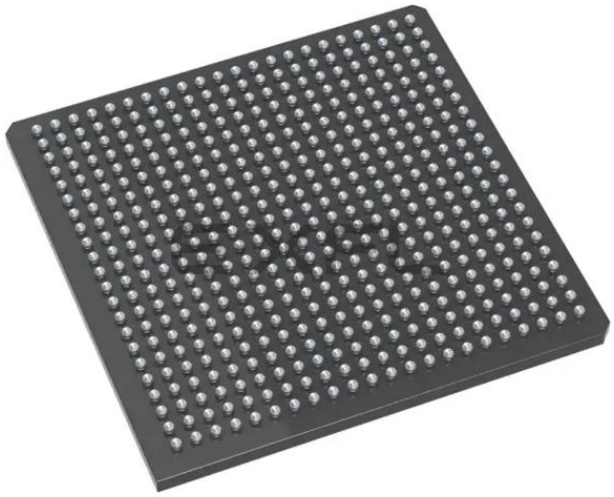

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	300
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fg484t

I/Os Per Package

ProASIC3 Devices	A3P060	A3P125	A3P250		A3P1000	
	I/O Type					
Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O [2]	Differential I/O Pairs	Single-Ended I/O [2]	Differential I/O Pairs
VQ100	71	71	68	13	–	–
FG144	96	97	97	24	97	25
FG256	–	–	157	38	177	44
FG484	–	–	–	–	300	74
QNG132	–	84	87	19	–	–

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the ProASIC3 FPGA Fabric User's Guide to ensure complying with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of available single-ended I/Os by two.*
3. *FG256 and FG484 are footprint-compatible packages.*

Automotive ProASIC3 Device Status

Automotive ProASIC3 Devices	Status
A3P060	Production
A3P125	Production
A3P250	Production
A3P1000	Production

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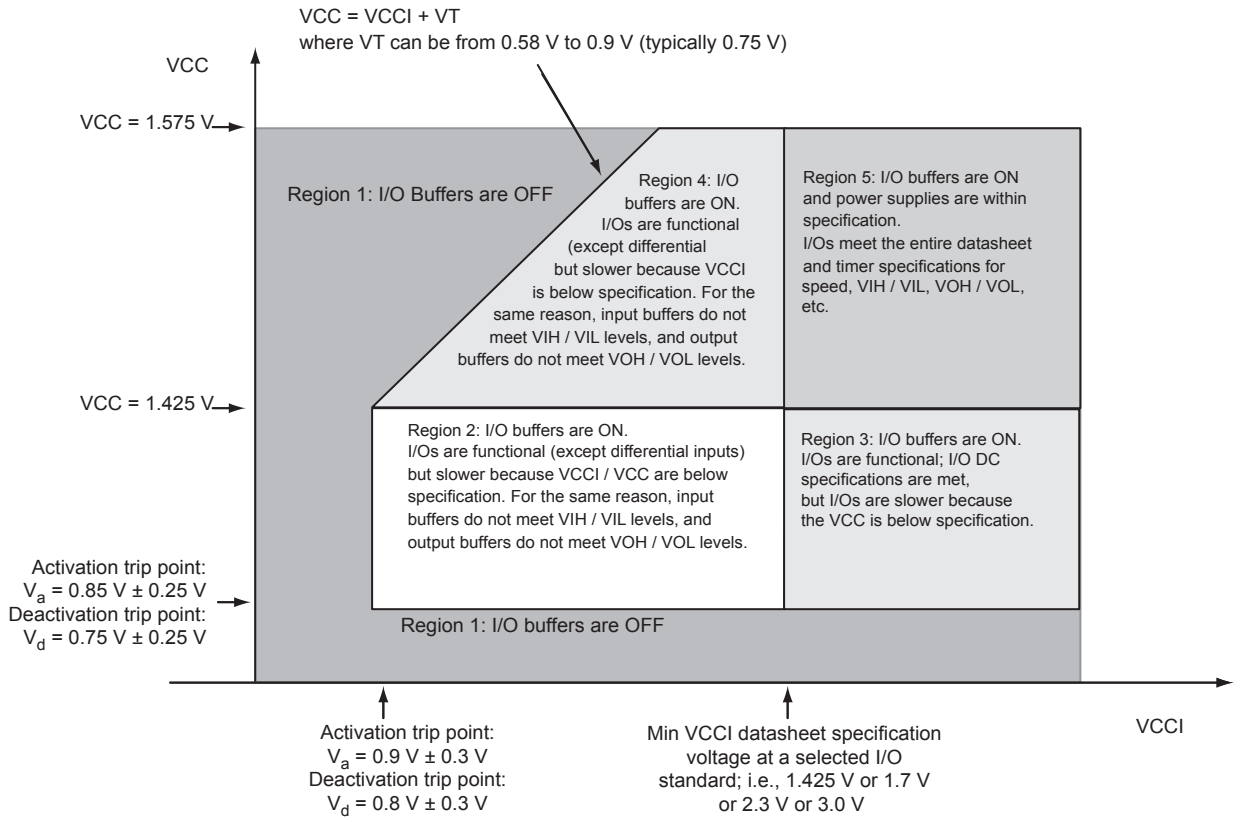

Figure 2-2 • **I/O State as a Function of VCCI and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \textit{EQ 1}$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-4 on page 2-5.

P = Power dissipation

Calculating Power Dissipation

Quiescent Supply Current

Table 2-6 • Quiescent Supply Current Characteristics

	A3P060	A3P125	A3P250	A3P1000
Typical (25°C)	2 mA	2 mA	3 mA	8 mA
Maximum (Automotive Grade 1) – 135°C	53 mA	53 mA	106 mA	265 mA
Maximum (Automotive Grade 2) – 115°C	26 mA	26 mA	53 mA	131 mA

Note: IDD Includes VCC, VPUMP, VCCI, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-7 and Table 2-10 on page 2-8.

Power per I/O Pin

Table 2-7 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Advanced I/O Banks

	VMV (V)	Static Power PDC2 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.69
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 2-10 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Standard Plus I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VMV.*
3. *PAC10 is the total dynamic power measured on VCCI and VMV.*

Power Consumption of Various Internal Resources

Table 2-11 • **Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)			
		A3P1000	A3P250	A3P125	A3P060
PAC1	Clock contribution of a Global Rib	14.50	11.00	11.00	9.30
PAC2	Clock contribution of a Global Spine	2.48	1.58	0.81	0.81
PAC3	Clock contribution of a VersaTile row	0.81			
PAC4	Clock contribution of a VersaTile used as a sequential module	0.12			
PAC5	First contribution of a VersaTile used as a sequential module	0.07			
PAC6	Second contribution of a VersaTile used as a sequential module	0.29			
PAC7	Contribution of a VersaTile used as a combinatorial module	0.29			
PAC8	Average contribution of a routing net	0.70			
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-7 on page 2-6.			
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-7 and Table 2-10 on page 2-8.			
PAC11	Average contribution of a RAM block during a read operation	25.00			
PAC12	Average contribution of a RAM block during a write operation	30.00			
PAC13	Static PLL contribution	2.55 mW			
PAC14	Dynamic contribution for PLL	2.60			

*Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-12 on page 2-11.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-13 on page 2-12.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-13 on page 2-12. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Table 2-22 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Automotive-Case Conditions: T_J = 135°C, Worst Case VCC = 1.425 V
Worst Case VCCI = 3.0 V
Advanced I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.80	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.39	0.04	1.23	0.39	3.45	3.27	1.83	1.86	5.58	5.39	ns
1.8 V LVCMOS	12 mA	High	35 pF	–	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.92	ns
1.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.88	0.04	1.37	0.39	2.25	1.98	3.75	4.00	3.46	3.21	ns
3.3 V PCI	Per PCI spec	High	10 pF	25 [2]	0.55	2.19	0.04	0.81	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25 [2]	0.55	2.55	0.04	0.79	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns
LVDS	24 mA	High	–	–	0.55	1.74	0.04	1.52	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.55	1.71	0.04	1.34	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-48 for connectivity. This resistor is not required during normal operation.*

Table 2-29 • I/O Short Currents IOSH/IOSL Applicable to Standard Plus I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
2.5 V LVCMOS	2 mA	18	16
	6 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

*Note: *T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-30 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months
125°C	25 days
135°	12 days

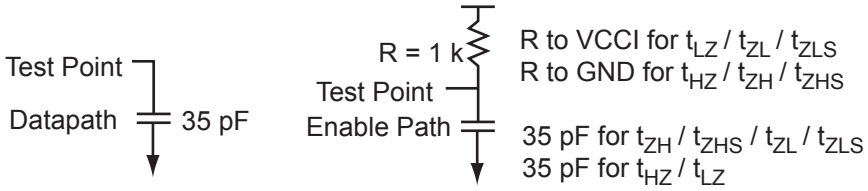

Figure 2-7 • **AC Loading**

Table 2-34 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	35

*Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.*

Timing Characteristics

Table 2-35 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	8.56	0.05	1.14	0.46	8.72	7.37	1.46	1.42	11.22	9.866	ns
	-1	0.55	7.28	0.04	0.97	0.39	7.42	6.27	1.46	1.42	9.54	8.393	ns
6 mA	STD	0.64	5.49	0.05	1.14	0.46	5.59	4.55	1.65	1.74	8.09	7.05	ns
	-1	0.55	4.67	0.04	0.97	0.39	4.75	3.87	1.65	1.74	6.88	5.997	ns
8 mA	STD	0.64	5.49	0.05	1.14	0.46	5.59	4.55	1.65	1.74	8.09	7.05	ns
	-1	0.55	4.67	0.04	0.97	0.39	4.75	3.87	1.65	1.74	6.88	5.997	ns
12 mA	STD	0.64	3.95	0.05	1.14	0.46	4.02	1.56	3.59	1.94	6.52	2.795	ns
	-1	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.797	ns
16 mA	STD	0.64	3.73	0.05	1.14	0.46	1.84	1.42	3.65	4.11	3.05	2.651	ns
	-1	0.55	3.17	0.04	0.97	0.39	1.84	1.42	3.10	3.50	3.05	2.653	ns
24 mA	STD	0.64	3.44	0.05	1.14	0.46	1.70	1.17	3.72	4.54	2.91	2.405	ns
	-1	0.55	2.92	0.04	0.97	0.39	1.70	1.17	3.16	3.86	2.91	2.407	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	11.47	0.05	1.14	0.46	11.68	9.95	1.46	1.33	14.18	12.449	ns
	-1	0.55	9.75	0.04	0.97	0.39	9.94	8.46	1.46	1.33	12.06	10.59	ns
6 mA	STD	0.64	8.13	0.05	1.14	0.46	8.28	7.03	1.65	1.65	10.79	9.526	ns
	-1	0.55	6.92	0.04	0.97	0.39	7.05	5.98	1.65	1.65	9.17	8.103	ns
8 mA	STD	0.64	8.13	0.05	1.14	0.46	8.28	7.03	1.65	1.65	10.79	9.526	ns
	-1	0.55	6.92	0.04	0.97	0.39	7.05	5.98	1.65	1.65	9.17	8.103	ns
12 mA	STD	0.64	6.24	0.05	1.14	0.46	6.36	5.45	1.77	1.85	8.86	7.946	ns
	-1	0.55	5.31	0.04	0.97	0.39	5.41	4.63	1.77	1.85	7.53	6.76	ns
16 mA	STD	0.64	5.82	0.05	1.14	0.46	5.93	5.10	1.80	1.90	8.43	7.604	ns
	-1	0.55	4.95	0.04	0.97	0.39	5.04	4.34	1.80	1.90	7.17	6.468	ns
24 mA	STD	0.64	5.42	0.05	1.14	0.46	5.52	5.08	1.83	2.10	8.02	7.581	ns
	-1	0.55	4.61	0.04	0.97	0.39	4.70	4.32	1.83	2.11	6.82	6.449	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-43 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		V_{OL}	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-44 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	VIL		VIH		V_{OL}	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

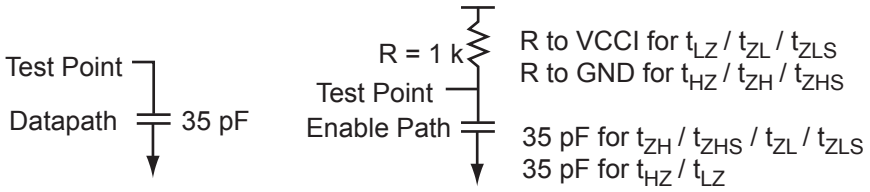

Figure 2-8 • AC Loading

Table 2-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	35

*Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.*

Timing Characteristics

Table 2-46 • 2.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.69	0.05	1.45	0.46	8.76	9.69	1.48	1.25	11.26	12.187	ns
	-1	0.55	8.24	0.04	1.23	0.39	7.45	8.24	1.48	1.25	9.58	10.367	ns
6 mA	STD	0.64	5.78	0.05	1.45	0.46	5.63	5.78	1.68	1.62	8.13	8.277	ns
	-1	0.55	4.91	0.04	1.23	0.39	4.79	4.91	1.69	1.63	6.92	7.04	ns
12 mA	STD	0.64	3.98	0.05	1.45	0.46	4.05	3.84	1.82	1.86	6.55	6.338	ns
	-1	0.55	3.39	0.04	1.23	0.39	3.45	3.27	1.83	1.86	5.58	5.392	ns
16 mA	STD	0.64	3.75	0.05	1.45	0.46	1.85	1.69	3.76	3.97	3.06	2.926	ns
	-1	0.55	3.19	0.04	1.23	0.39	1.85	1.69	3.20	3.38	3.06	2.929	ns
24 mA	STD	0.64	3.45	0.05	1.45	0.46	1.70	1.35	3.84	4.47	2.92	2.585	ns
	-1	0.55	2.94	0.04	1.23	0.39	1.71	1.35	3.27	3.80	2.92	2.586	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-47 • 2.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	12.12	0.05	1.45	0.46	12.54	12.74	1.48	1.19	15.04	15.243	ns
	-1	0.55	10.31	0.04	1.23	0.39	10.67	10.84	1.48	1.20	12.80	12.966	ns
6 mA	STD	0.64	8.24	0.05	1.45	0.46	9.07	8.74	1.68	1.57	11.57	11.237	ns
	-1	0.55	7.01	0.04	1.23	0.39	7.71	7.43	1.69	1.57	9.84	9.559	ns
12 mA	STD	0.64	6.91	0.05	1.45	0.46	7.04	6.62	1.82	1.80	9.54	9.117	ns
	-1	0.55	5.88	0.04	1.23	0.39	5.99	5.63	1.83	1.80	8.11	7.756	ns
16 mA	STD	0.64	6.44	0.05	1.45	0.46	6.56	6.18	1.86	1.86	9.06	8.678	ns
	-1	0.55	5.48	0.04	1.23	0.39	5.58	5.26	1.86	1.86	7.71	7.382	ns
24 mA	STD	0.64	6.16	0.05	1.45	0.46	6.15	6.16	1.90	2.10	8.65	8.657	ns
	-1	0.55	5.24	0.04	1.23	0.39	5.23	5.24	1.90	2.10	7.36	7.364	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-54 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * V_{CCI}	3.6	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	16	16	74	91	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-55 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	44	35	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

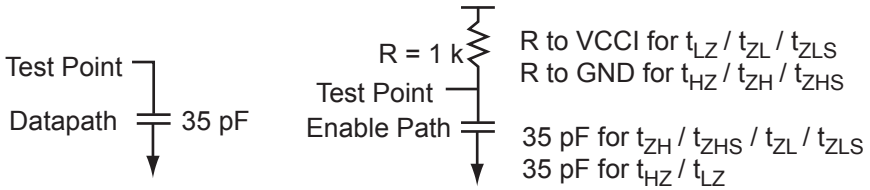

Figure 2-9 • AC Loading

Table 2-56 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	35

*Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

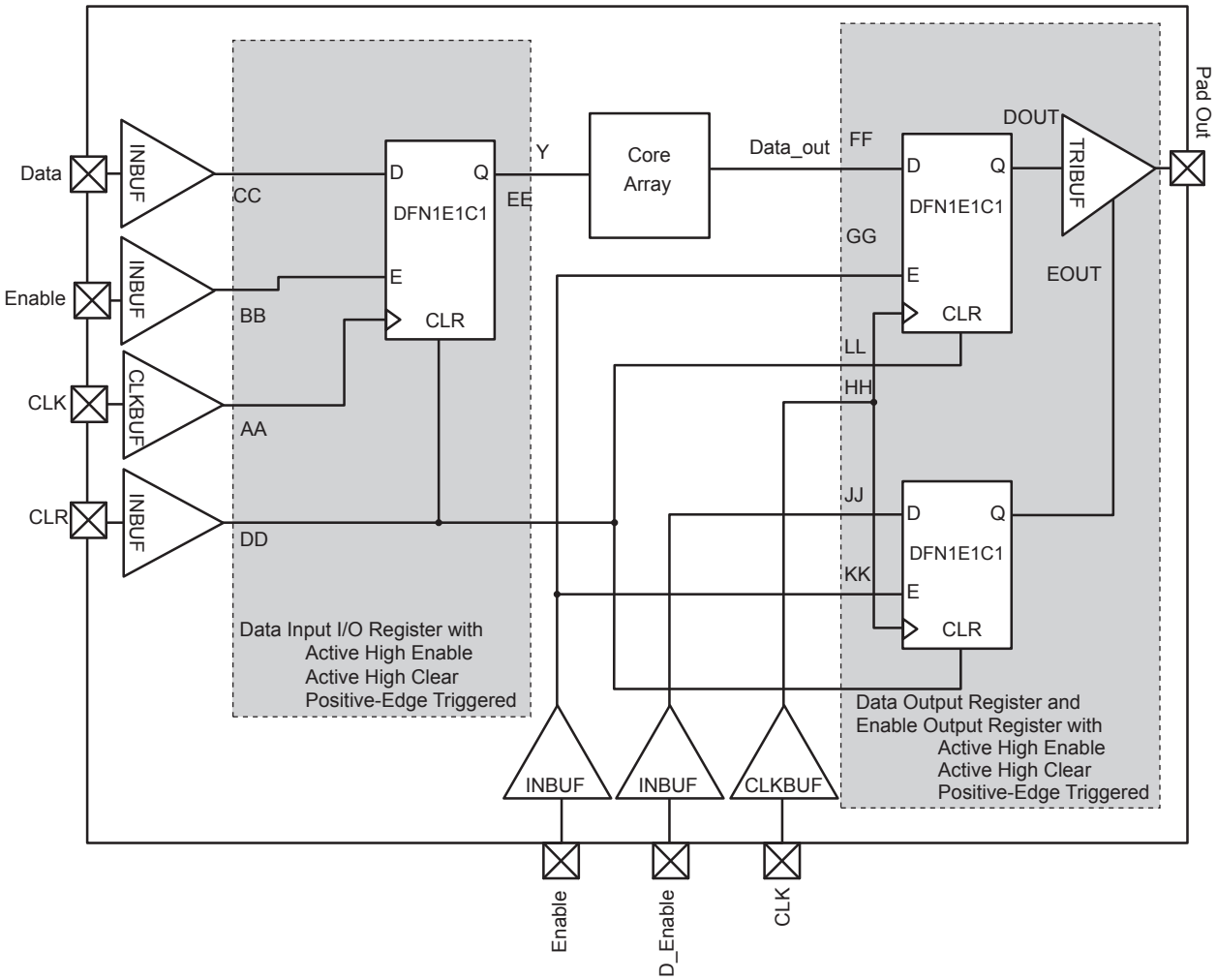

Figure 2-16 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-95 • Output Data Register Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.70	0.82	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.37	0.44	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.52	0.61	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.96	1.12	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.96	1.12	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Output Enable Register

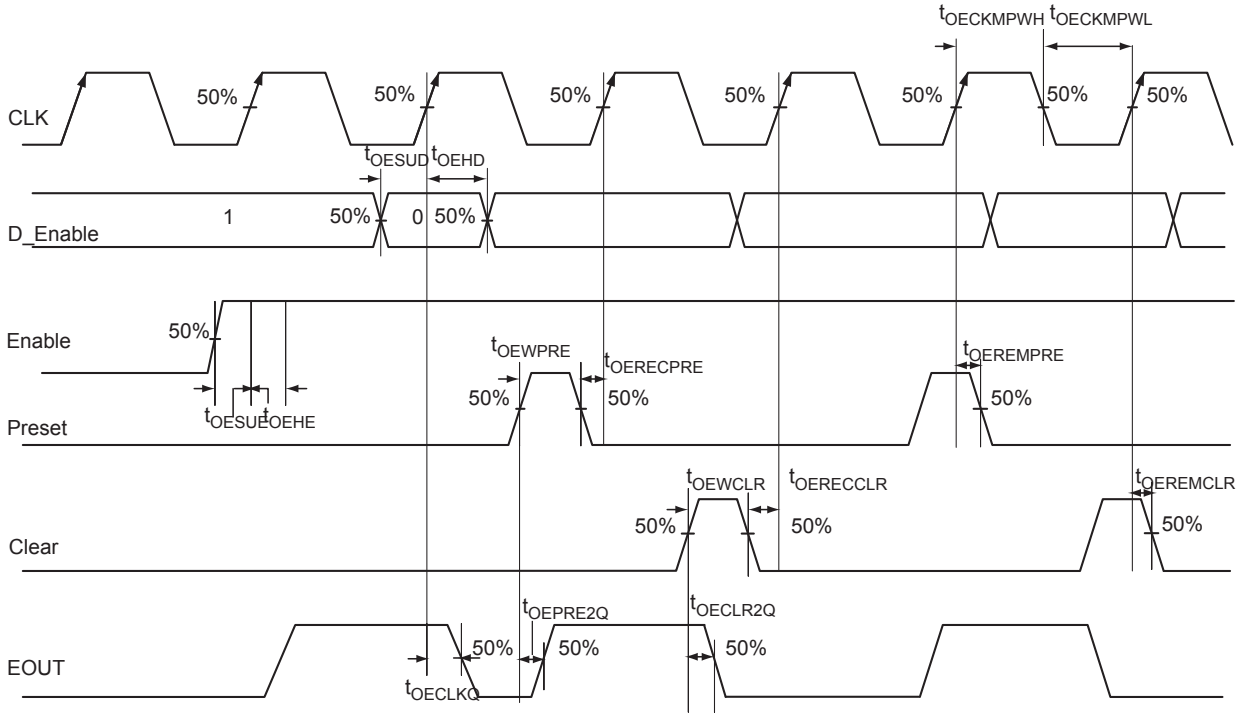

Figure 2-19 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-96 • **Output Enable Register Propagation Delays**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.54	0.64	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.38	0.45	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.53	0.62	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.32	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.32	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Timing Waveforms

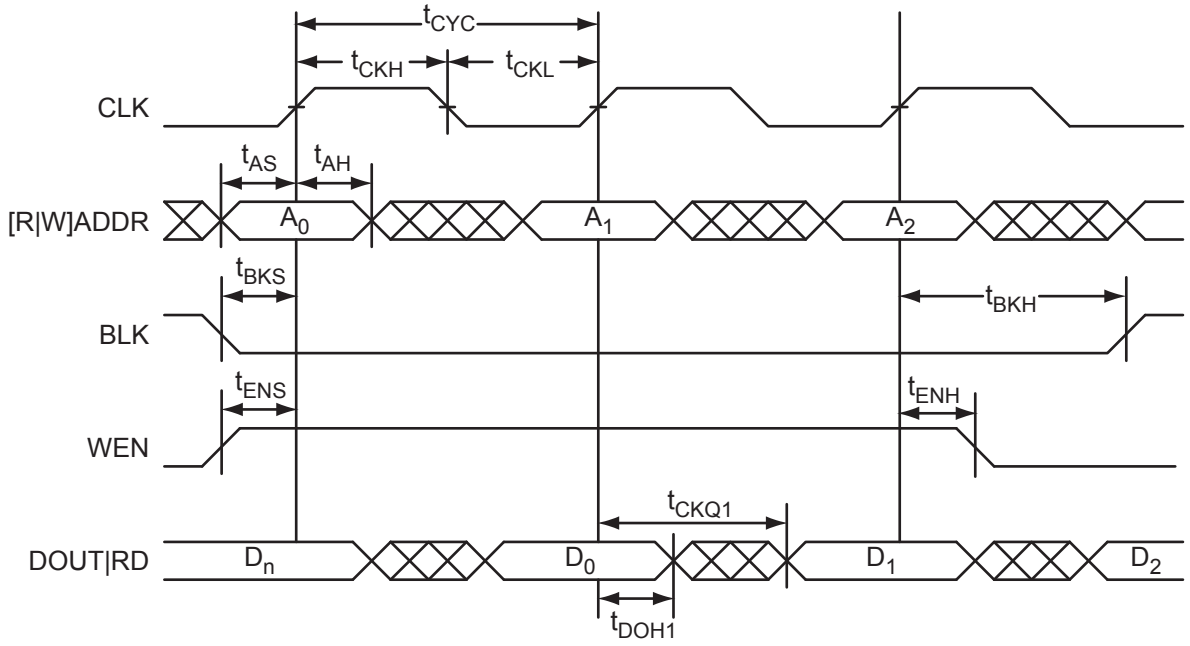

Figure 2-31 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

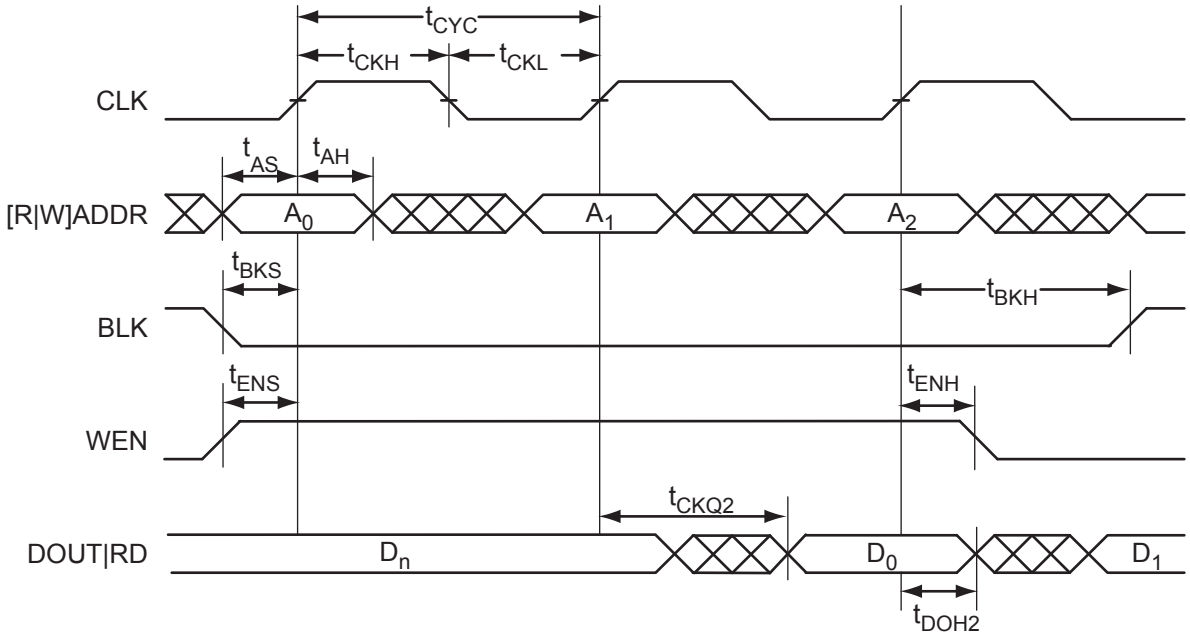

Figure 2-32 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

QN132	
Pin Number	A3P250 Function
A1	GAB2/IO117UPB3
A2	IO117VPB3
A3	VCCIB3
A4	GFC1/IO110PDB3
A5	GFB0/IO109NPB3
A6	VCCPLF
A7	GFA1/IO108PPB3
A8	GFC2/IO105PPB3
A9	IO103NDB3
A10	VCC
A11	GEA1/IO98PPB3
A12	GEA0/IO98NPB3
A13	GEC2/IO95RSB2
A14	IO91RSB2
A15	VCC
A16	IO90RSB2
A17	IO87RSB2
A18	IO85RSB2
A19	IO82RSB2
A20	IO76RSB2
A21	IO70RSB2
A22	VCC
A23	GDB2/IO62RSB2
A24	TDI
A25	TRST
A26	GDC1/IO58UDB1
A27	VCC
A28	IO54NDB1
A29	IO52NDB1
A30	GCA2/IO51PPB1
A31	GCA0/IO50NPB1
A32	GCB1/IO49PDB1
A33	IO47NSB1
A34	VCC
A35	IO41NPB1
A36	GBA2/IO41PPB1

QN132	
Pin Number	A3P250 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO118VDB3
B2	GAC2/IO116UDB3
B3	GND
B4	GFC0/IO110NDB3
B5	VCOMPLF
B6	GND
B7	GFB2/IO106PSB3
B8	IO103PDB3
B9	GND
B10	GEB0/IO99NDB3
B11	VMV3
B12	GEB2/IO96RSB2
B13	IO92RSB2
B14	GND
B15	IO89RSB2
B16	IO86RSB2
B17	GND
B18	IO78RSB2
B19	IO72RSB2
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO58VDB1

QN132	
Pin Number	A3P250 Function
B25	GND
B26	IO54PDB1
B27	GCB2/IO52PDB1
B28	GND
B29	GCB0/IO49NDB1
B30	GCC1/IO48PDB1
B31	GND
B32	GBB2/IO42PDB1
B33	VMV1
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO118UDB3
C2	IO116VDB3
C3	VCC
C4	GFB1/IO109PPB3
C5	GFA0/IO108NPB3
C6	GFA2/IO107PSB3
C7	IO105NPB3
C8	VCCIB3
C9	GEB1/IO99PDB3
C10	GNDQ
C11	GEA2/IO97RSB2
C12	IO94RSB2
C13	VCCIB2
C14	IO88RSB2
C15	IO84RSB2
C16	IO80RSB2

FG256	
Pin Number	**A3P250 Function**
P9	IO76RSB2
P10	IO71RSB2
P11	IO66RSB2
P12	NC
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO60VDB1
R1	GEA1/IO98PDB3
R2	GEA0/IO98NDB3
R3	NC
R4	GEC2/IO95RSB2
R5	IO91RSB2
R6	IO88RSB2
R7	IO84RSB2
R8	IO80RSB2
R9	IO77RSB2
R10	IO72RSB2
R11	IO68RSB2
R12	IO65RSB2
R13	GDB2/IO62RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO94RSB2
T3	GEB2/IO96RSB2
T4	IO93RSB2
T5	IO90RSB2
T6	IO87RSB2
T7	IO83RSB2
T8	IO79RSB2
T9	IO78RSB2
T10	IO73RSB2
T11	IO70RSB2
T12	GDC2/IO63RSB2

FG256	
Pin Number	**A3P250 Function**
T13	IO67RSB2
T14	GDA2/IO61RSB2
T15	TMS
T16	GND

FG484	
Pin Number	**A3P1000 Function**
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2

FG484	
Pin Number	**A3P1000 Function**
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1

FG484	
Pin Number	**A3P1000 Function**
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC