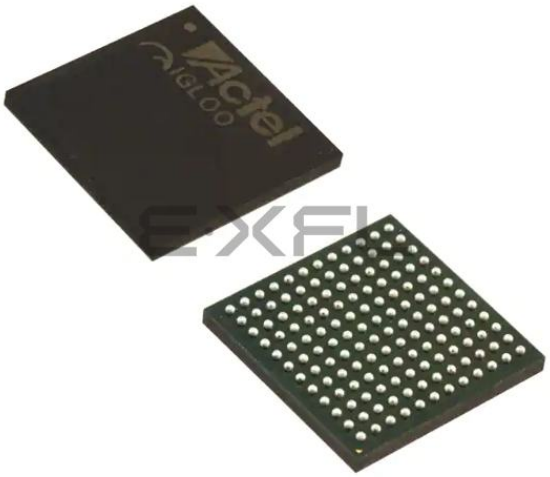


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fgg144t

I/Os Per Package

ProASIC3 Devices	A3P060	A3P125	A3P250		A3P1000	
	I/O Type					
Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O [2]	Differential I/O Pairs	Single-Ended I/O [2]	Differential I/O Pairs
VQ100	71	71	68	13	–	–
FG144	96	97	97	24	97	25
FG256	–	–	157	38	177	44
FG484	–	–	–	–	300	74
QNG132	–	84	87	19	–	–

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the ProASIC3 FPGA Fabric User's Guide to ensure complying with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of available single-ended I/Os by two.*
3. *FG256 and FG484 are footprint-compatible packages.*

Automotive ProASIC3 Device Status

Automotive ProASIC3 Devices	Status
A3P060	Production
A3P125	Production
A3P250	Production
A3P1000	Production

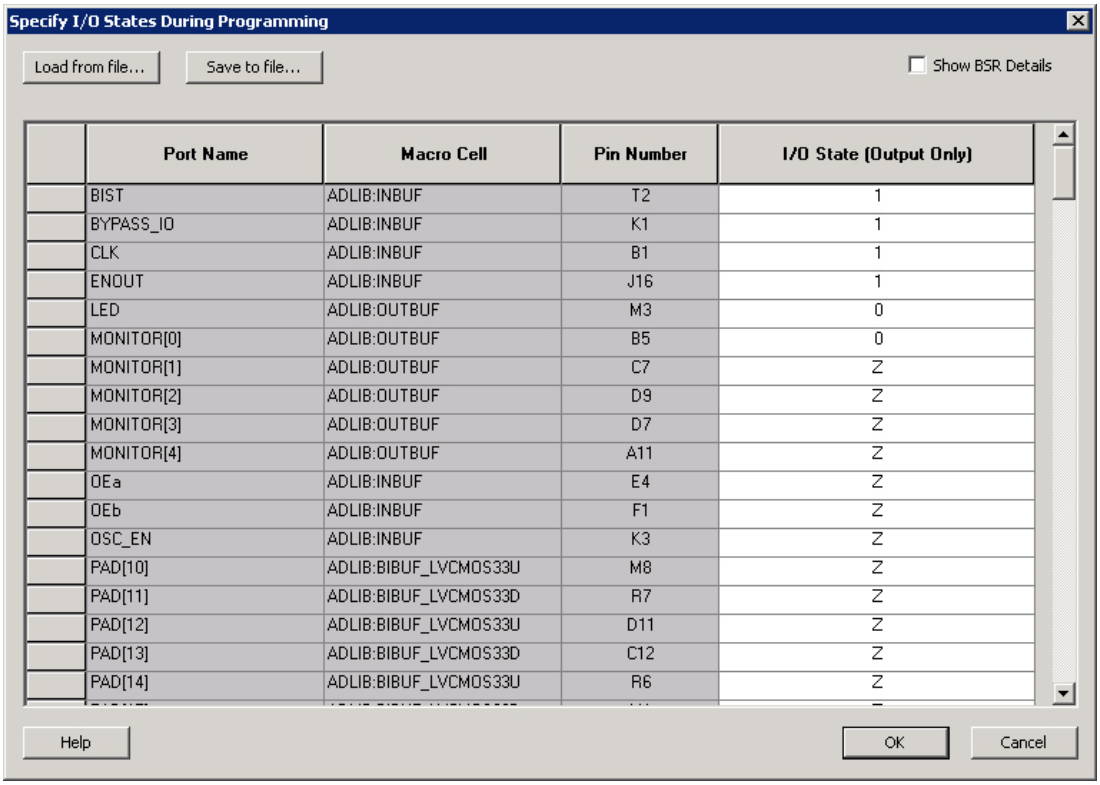
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tristate: I/O is tristated



	Port Name	Macro Cell	Pin Number	I/O State (Output Only)
	BIST	ADLIB:INBUF	T2	1
	BYPASS_IO	ADLIB:INBUF	K1	1
	CLK	ADLIB:INBUF	B1	1
	ENOUT	ADLIB:INBUF	J16	1
	LED	ADLIB:OUTBUF	M3	0
	MONITOR[0]	ADLIB:OUTBUF	B5	0
	MONITOR[1]	ADLIB:OUTBUF	C7	Z
	MONITOR[2]	ADLIB:OUTBUF	D9	Z
	MONITOR[3]	ADLIB:OUTBUF	D7	Z
	MONITOR[4]	ADLIB:OUTBUF	A11	Z
	OEa	ADLIB:INBUF	E4	Z
	OEb	ADLIB:INBUF	F1	Z
	OSC_EN	ADLIB:INBUF	K3	Z
	PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
	PAD[11]	ADLIB:BIBUF_LVCMOS33D	R7	Z
	PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
	PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
	PAD[14]	ADLIB:BIBUF_LVCMOS33U	R6	Z

Figure 1-4 • **I/O States During Programming Window**

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

Table 2-10 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Standard Plus I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VMV.*
3. *PAC10 is the total dynamic power measured on VCCI and VMV.*

Detailed I/O DC Characteristics

Table 2-24 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-25 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to Advanced I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	6 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / I_{OLspec}*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / I_{OHspec}*

**Table 2-28 • I/O Short Currents IOSH/IOSL
Applicable to Advanced I/O Banks**

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	6 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

*Note: *T_J = 100°C*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-32 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-33 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	109	103	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-41 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	7.79	0.05	1.08	0.45	7.94	6.80	1.22	1.23	7.94	6.80	ns
	-1	0.55	6.85	0.04	0.95	0.39	6.98	5.98	1.26	1.27	6.98	5.98	ns
6 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
8 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
12 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns
16 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-42 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	10.47	0.05	1.08	0.45	10.66	9.11	1.22	1.16	10.66	9.11	ns
	-1	0.55	9.21	0.04	0.95	0.39	9.38	8.01	1.26	1.20	9.38	8.01	ns
6 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
8 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
12 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns
16 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Timing Characteristics

Table 2-57 • 1.8 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.26	0.05	1.36	0.46	10.22	13.26	1.53	0.90	12.72	15.764	ns
	-1	0.55	11.28	0.04	1.16	0.39	8.69	11.28	1.53	0.90	10.82	13.41	ns
4 mA	STD	0.64	7.73	0.05	1.36	0.46	6.55	7.73	1.78	1.54	9.05	10.232	ns
	-1	0.55	6.58	0.04	1.16	0.39	5.58	6.58	1.78	1.54	7.70	8.704	ns
6 mA	STD	0.64	4.97	0.05	1.36	0.46	4.67	4.97	1.95	1.83	7.17	7.472	ns
	-1	0.55	4.23	0.04	1.16	0.39	3.98	4.23	1.95	1.83	6.10	6.356	ns
8 mA	STD	0.64	4.39	0.05	1.36	0.46	4.39	4.39	1.99	1.91	6.89	6.888	ns
	-1	0.55	3.73	0.04	1.16	0.39	3.74	3.73	1.99	1.91	5.86	5.859	ns
12 mA	STD	0.64	3.95	0.05	1.36	0.46	1.95	1.68	4.14	4.56	3.16	2.915	ns
	-1	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.918	ns
16 mA	STD	0.64	3.95	0.05	1.36	0.46	1.95	1.68	4.14	4.56	3.16	2.915	ns
	-1	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.918	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-60 • 1.8 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	17.36	0.05	1.45	0.46	15.09	16.55	1.24	0.79	17.59	19.052	ns
	-1	0.55	14.77	0.04	1.23	0.39	12.84	14.08	1.24	0.79	14.96	16.207	ns
4 mA	STD	0.64	11.71	0.05	1.45	0.46	10.88	11.07	1.47	1.35	13.38	13.567	ns
	-1	0.55	9.96	0.04	1.23	0.39	9.26	9.41	1.47	1.35	11.38	11.541	ns
6 mA	STD	0.64	9.00	0.05	1.45	0.46	8.47	8.18	1.62	1.62	10.97	10.685	ns
	-1	0.55	7.66	0.04	1.23	0.39	7.21	6.96	1.62	1.62	9.33	9.089	ns
8 mA	STD	0.64	8.39	0.05	1.45	0.46	8.47	8.18	1.62	1.62	10.97	10.685	ns
	-1	0.55	7.14	0.04	1.23	0.39	7.21	6.96	1.62	1.62	9.33	9.089	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-61 • 1.8 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	12.83	0.05	1.32	0.45	9.88	12.83	1.48	0.87	12.30	15.25	ns
	-1	0.53	10.92	0.04	1.12	0.38	8.41	10.92	1.48	0.87	10.46	12.97	ns
4 mA	STD	0.63	7.48	0.05	1.32	0.45	6.34	7.48	1.72	1.49	8.76	9.90	ns
	-1	0.53	6.36	0.04	1.12	0.38	5.39	6.36	1.72	1.49	7.45	8.42	ns
6 mA	STD	0.63	4.81	0.05	1.32	0.45	4.52	4.81	1.89	1.77	6.94	7.23	ns
	-1	0.53	4.09	0.04	1.12	0.38	3.85	4.09	1.89	1.77	5.90	6.15	ns
8 mA	STD	0.63	4.25	0.05	1.32	0.45	4.25	4.25	1.92	1.85	6.67	6.66	ns
	-1	0.53	3.61	0.04	1.12	0.38	3.61	3.61	1.93	1.85	5.67	5.67	ns
12 mA	STD	0.63	3.82	0.05	1.32	0.45	1.89	1.63	4.00	4.41	3.06	2.82	ns
	-1	0.53	3.25	0.04	1.12	0.38	1.89	1.63	3.41	3.75	3.06	2.82	ns
16 mA	STD	0.63	3.82	0.05	1.32	0.45	1.89	1.63	4.00	4.41	3.06	2.82	ns
	-1	0.53	3.25	0.04	1.12	0.38	1.89	1.63	3.41	3.75	3.06	2.82	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-64 • 1.8 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	16.80	0.05	1.40	0.45	14.60	16.01	1.20	0.77	17.02	18.43	ns
	-1	0.53	14.29	0.04	1.19	0.38	12.42	13.62	1.20	0.77	14.48	15.68	ns
4 mA	STD	0.63	11.33	0.05	1.40	0.45	10.53	10.71	1.42	1.31	12.95	13.13	ns
	-1	0.53	9.64	0.04	1.19	0.38	8.96	9.11	1.42	1.31	11.01	11.17	ns
6 mA	STD	0.63	8.71	0.05	1.40	0.45	8.19	7.92	1.57	1.57	10.61	10.34	ns
	-1	0.53	7.41	0.04	1.19	0.38	6.97	6.74	1.57	1.57	9.03	8.79	ns
8 mA	STD	0.63	8.12	0.05	1.40	0.45	8.19	7.92	1.57	1.57	10.61	10.34	ns
	-1	0.53	6.90	0.04	1.19	0.38	6.97	6.74	1.57	1.57	9.03	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-65 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	–0.3	0.30 * VCCI	0.7 * V_{CCI}	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * V_{CCI}	12	12	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

3.3 V PCI, 3.3 V PCI-X

The Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-76 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-11.

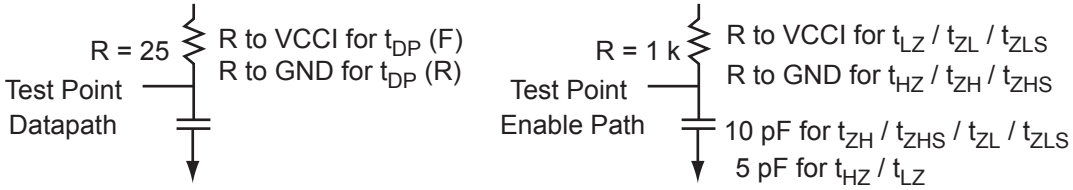


Figure 2-11 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 2-77.

Table 2-77 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for tDP(R) 0.615 * VCCI for tDP(F)	10

*Note: *Measuring point = Vtrip. See Table 2-18 on page 2-17 for a complete table of trip points.*

Timing Characteristics

Table 2-78 • 3.3 V PCI/PCI-X
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.64	2.58	0.05	0.95	0.46	1.27	0.94	3.12	3.60	2.49	2.18	ns
–1	0.55	2.19	0.04	0.81	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-79 • 3.3 V PCI/PCI-X
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.64	3.00	0.05	0.93	0.46	1.27	0.94	3.12	3.60	2.49	2.18	ns
–1	0.55	2.55	0.04	0.79	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-93 • Input Data Register Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.29	0.34	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.31	0.37	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.44	0.52	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.54	0.64	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.54	0.64	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.27	0.31	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.27	0.31	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Output Register

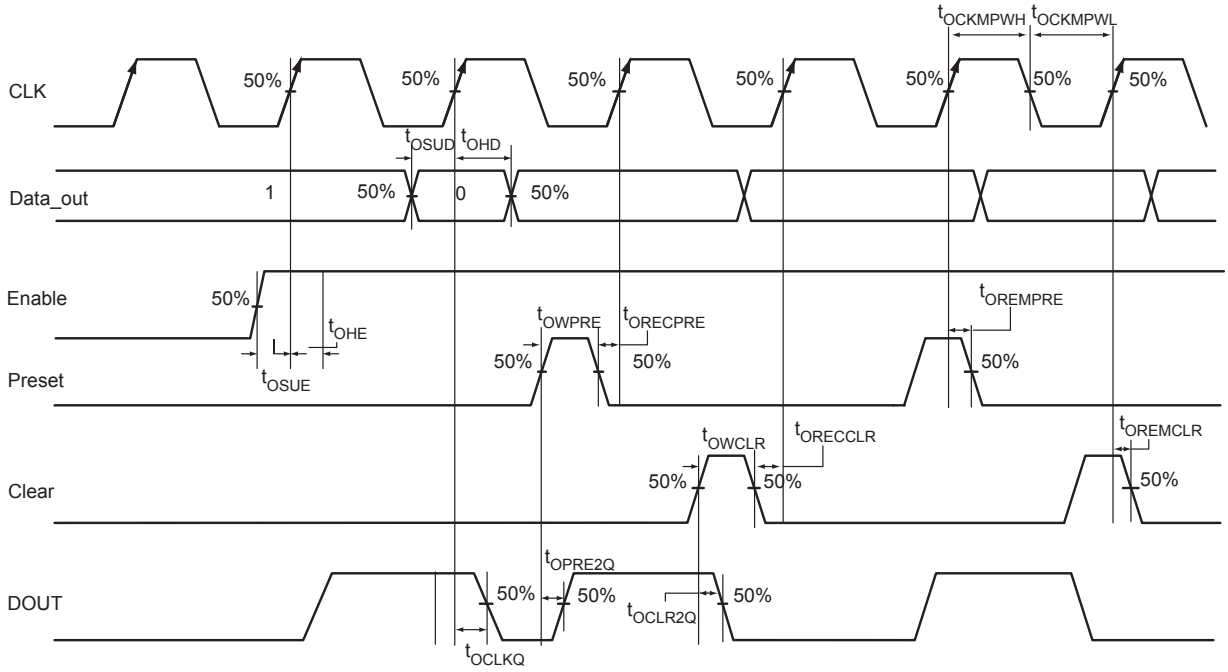


Figure 2-18 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-94 • **Output Data Register Propagation Delays**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.72	0.84	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.38	0.45	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.53	0.63	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.98	1.15	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.98	1.15	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.32	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.32	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Timing Characteristics

Table 2-104 • Combinatorial Cell Propagation Delays
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.49	0.57	ns
AND2	Y = A · B	t_{PD}	0.57	0.67	ns
NAND2	Y = !(A · B)	t_{PD}	0.57	0.67	ns
OR2	Y = A + B	t_{PD}	0.59	0.69	ns
NOR2	Y = !(A + B)	t_{PD}	0.59	0.69	ns
XOR2	Y = A ⊕ B	t_{PD}	0.90	1.05	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.85	1.00	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.06	1.25	ns
MUX2	Y = A !S + B S	t_{PD}	0.62	0.72	ns
AND3	Y = A · B · C	t_{PD}	0.68	0.80	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-105 • Combinatorial Cell Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.48	0.56	ns
AND2	Y = A · B	t_{PD}	0.56	0.66	ns
NAND2	Y = !(A · B)	t_{PD}	0.56	0.66	ns
OR2	Y = A + B	t_{PD}	0.58	0.68	ns
NOR2	Y = !(A + B)	t_{PD}	0.58	0.68	ns
XOR2	Y = A ⊕ B	t_{PD}	0.88	1.03	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.83	0.98	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.04	1.23	ns
MUX2	Y = A !S + B S	t_{PD}	0.60	0.71	ns
AND3	Y = A · B · C	t_{PD}	0.67	0.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Timing Waveforms

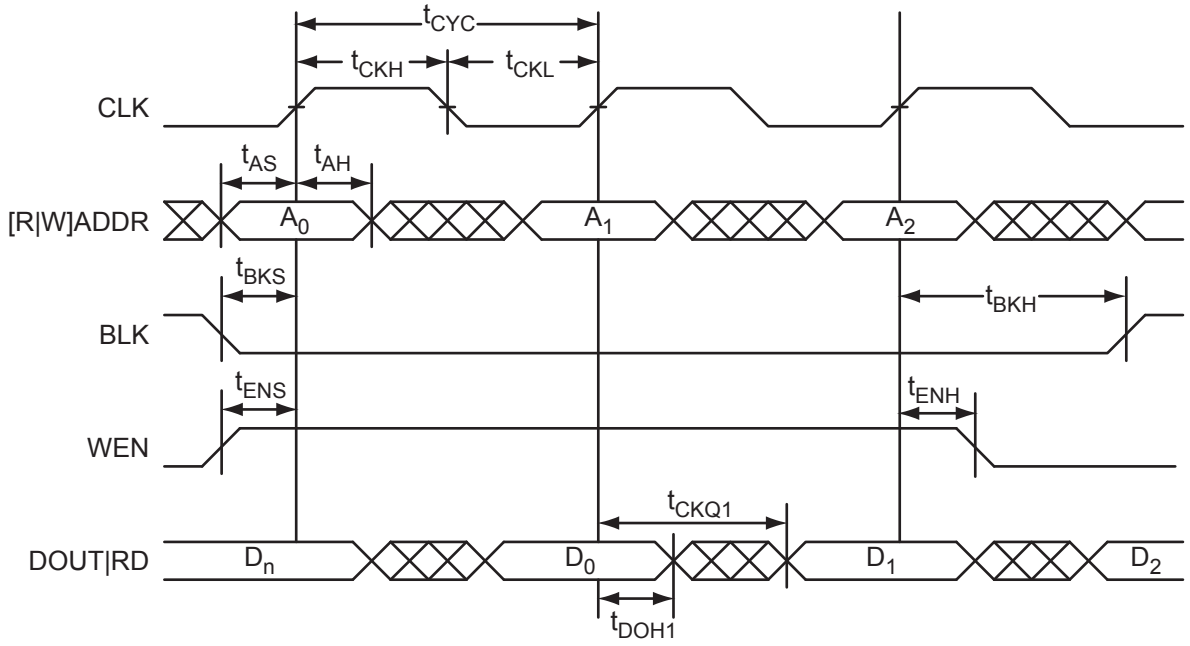


Figure 2-31 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

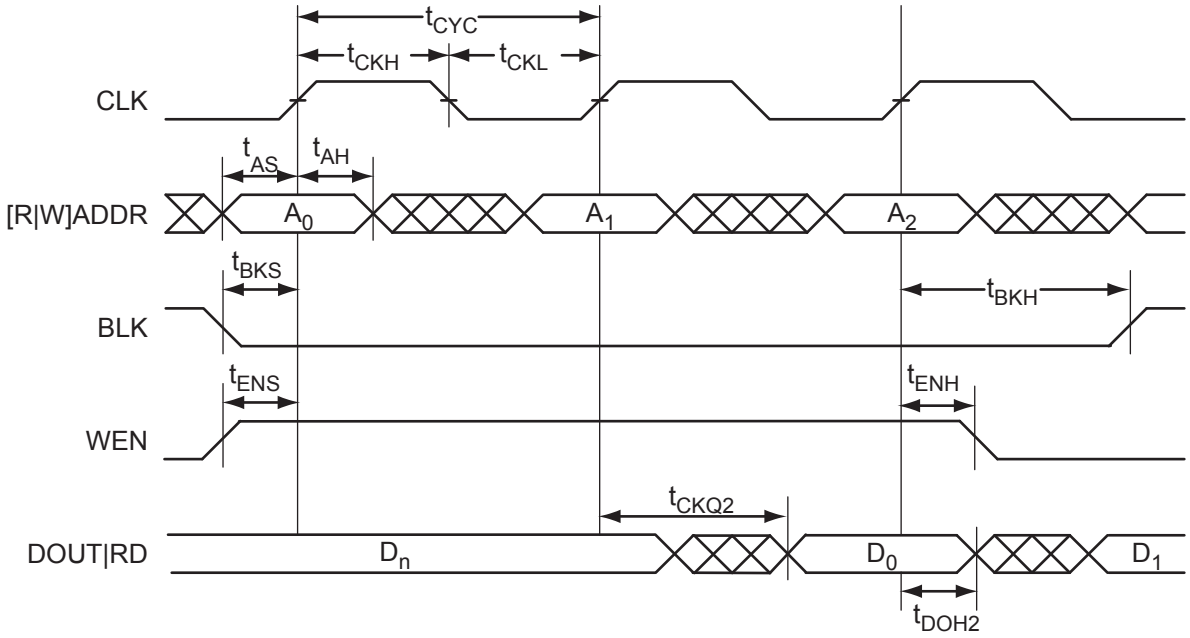


Figure 2-32 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

3 – Pin Descriptions and Packaging

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to four I/O banks on Automotive ProASIC3 devices, plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *Automotive ProASIC3 FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on Automotive ProASIC3 devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on Automotive ProASIC3 devices.

VJTAG **JTAG Supply Voltage**

Automotive ProASIC3 devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is

QN132	
Pin Number	A3P250 Function
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Automotive ProASIC3 Device Status" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group’s products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

51700099-5/01.13