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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-fg144t

Advanced Architecture

The proprietary Automotive ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The Automotive ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM memory
- Extensive CCCs and PLLs
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the Automotive ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

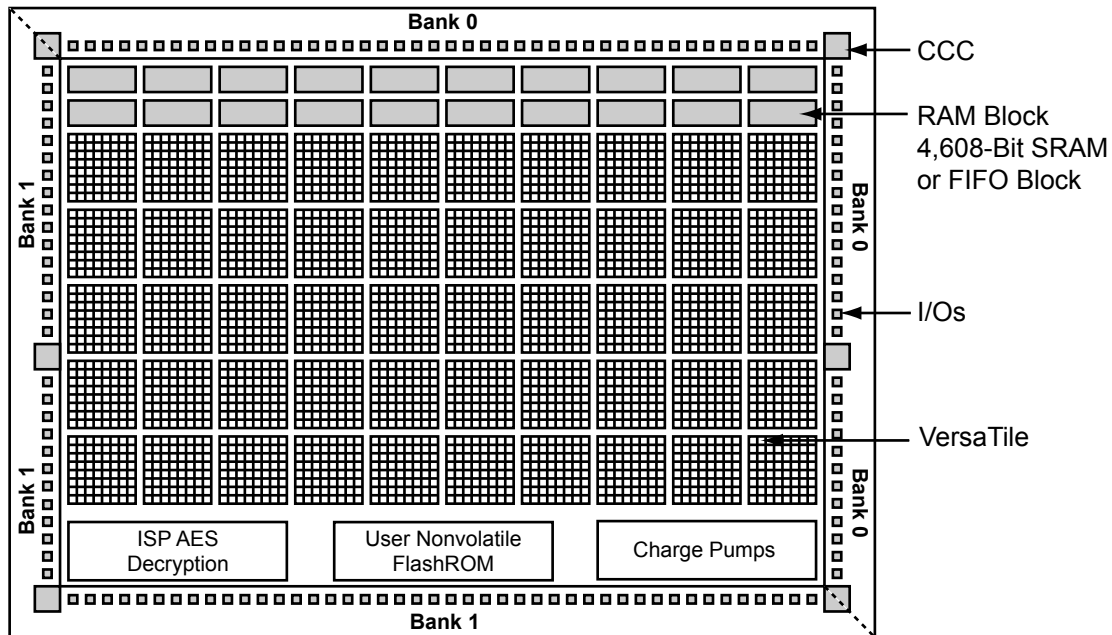


Figure 1-1 • Automotive ProASIC3 Device Architecture Overview with Two I/O Banks (A3P060 and A3P125)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 350 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

Automotive ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The Automotive ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Automotive ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

Automotive ProASIC3 banks for the A3P250 and A3P1000 devices support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the [FlashPro User's Guide](#) for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify ([Figure 1-4 on page 1-7](#)).

Table 2-10 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹
Applicable to Standard Plus I/O Banks

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. PDC3 is the static power (where applicable) measured on VMV.
3. PAC10 is the total dynamic power measured on VCCI and VMV.

Power Consumption of Various Internal Resources

Table 2-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices

Parameter	Definition	Device Specific Dynamic Power (μW/MHz)			
		A3P1000	A3P250	A3P125	A3P060
PAC1	Clock contribution of a Global Rib	14.50	11.00	11.00	9.30
PAC2	Clock contribution of a Global Spine	2.48	1.58	0.81	0.81
PAC3	Clock contribution of a VersaTile row	0.81			
PAC4	Clock contribution of a VersaTile used as a sequential module	0.12			
PAC5	First contribution of a VersaTile used as a sequential module	0.07			
PAC6	Second contribution of a VersaTile used as a sequential module	0.29			
PAC7	Contribution of a VersaTile used as a combinatorial module	0.29			
PAC8	Average contribution of a routing net	0.70			
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-7 on page 2-6 .			
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-7 and Table 2-10 on page 2-8 .			
PAC11	Average contribution of a RAM block during a read operation	25.00			
PAC12	Average contribution of a RAM block during a write operation	30.00			
PAC13	Static PLL contribution	2.55 mW			
PAC14	Dynamic contribution for PLL	2.60			

Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-12 on page 2-11](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-13 on page 2-12](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-13 on page 2-12](#). The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Table 2-39 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	8.28	0.05	1.10	0.45	8.44	7.13	1.42	1.37	10.85	9.55	ns
	-1	0.53	7.05	0.04	0.94	0.38	7.18	6.06	1.42	1.37	9.23	8.12	ns
6 mA	STD	0.63	5.31	0.05	1.10	0.45	5.41	4.40	1.60	1.68	7.83	6.82	ns
	-1	0.53	4.52	0.04	0.94	0.38	4.60	3.74	1.60	1.68	6.66	5.80	ns
8 mA	STD	0.63	5.31	0.05	1.10	0.45	5.41	4.40	1.60	1.68	7.83	6.82	ns
	-1	0.53	4.52	0.04	0.94	0.38	4.60	3.74	1.60	1.68	6.66	5.80	ns
12 mA	STD	0.63	3.82	0.05	1.10	0.45	3.89	1.51	3.47	1.88	6.31	2.70	ns
	-1	0.53	3.25	0.04	0.94	0.38	3.31	1.51	2.96	1.88	5.37	2.71	ns
16 mA	STD	0.63	3.60	0.05	1.10	0.45	1.78	1.37	3.53	3.98	2.95	2.57	ns
	-1	0.53	3.07	0.04	0.94	0.38	1.78	1.37	3.00	3.38	2.95	2.57	ns
24 mA	STD	0.63	3.33	0.05	1.10	0.45	1.64	1.13	3.60	4.39	2.81	2.33	ns
	-1	0.53	2.83	0.04	0.94	0.38	1.64	1.13	3.06	3.74	2.82	2.33	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-40 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	11.09	0.05	1.10	0.45	11.30	9.63	1.41	1.29	13.72	12.04	ns
	-1	0.53	9.44	0.04	0.94	0.38	9.61	8.19	1.41	1.29	11.67	10.25	ns
6 mA	STD	0.63	7.87	0.05	1.10	0.45	8.02	6.80	1.59	1.59	10.43	9.22	ns
	-1	0.53	6.69	0.04	0.94	0.38	6.82	5.78	1.59	1.60	8.88	7.84	ns
8 mA	STD	0.63	7.87	0.05	1.10	0.45	8.02	6.80	1.59	1.59	10.43	9.22	ns
	-1	0.53	6.69	0.04	0.94	0.38	6.82	5.78	1.59	1.60	8.88	7.84	ns
12 mA	STD	0.63	6.04	0.05	1.10	0.45	6.15	5.27	1.71	1.79	8.57	7.69	ns
	-1	0.53	5.14	0.04	0.94	0.38	5.23	4.48	1.71	1.79	7.29	6.54	ns
16 mA	STD	0.63	5.63	0.05	1.10	0.45	5.74	4.94	1.74	1.84	8.16	7.36	ns
	-1	0.53	4.79	0.04	0.94	0.38	4.88	4.20	1.74	1.84	6.94	6.26	ns
24 mA	STD	0.63	5.25	0.05	1.10	0.45	5.34	4.92	1.77	2.04	7.76	7.34	ns
	-1	0.53	4.46	0.04	0.94	0.38	4.55	4.18	1.77	2.04	6.60	6.24	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-73 • 1.5 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.83	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.76	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.83	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	9.21	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns
6 mA	STD	0.63	10.10	0.05	1.40	0.45	10.28	9.62	2.05	1.80	12.70	12.04	ns
	-1	0.53	8.59	0.04	1.19	0.38	8.75	8.18	2.05	1.80	10.81	10.24	ns
8 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns
12 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-74 • 1.5 V LVCMOS High Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	8.47	0.05	1.54	0.45	7.38	9.05	1.81	1.45	9.80	11.47	ns
	-1	0.53	7.21	0.04	1.31	0.38	6.28	7.70	1.81	1.45	8.34	9.75	ns
4 mA	STD	0.63	5.24	0.05	1.54	0.45	5.25	5.75	2.00	1.78	7.67	8.17	ns
	-1	0.53	4.45	0.04	1.31	0.38	4.46	4.89	2.00	1.78	6.52	6.95	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-75 • 1.5 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.07	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.12	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.04	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	8.54	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in [Figure 2-13](#). The input and output buffer delays are available in the LVDS section in [Table 2-84](#) on page 2-50.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

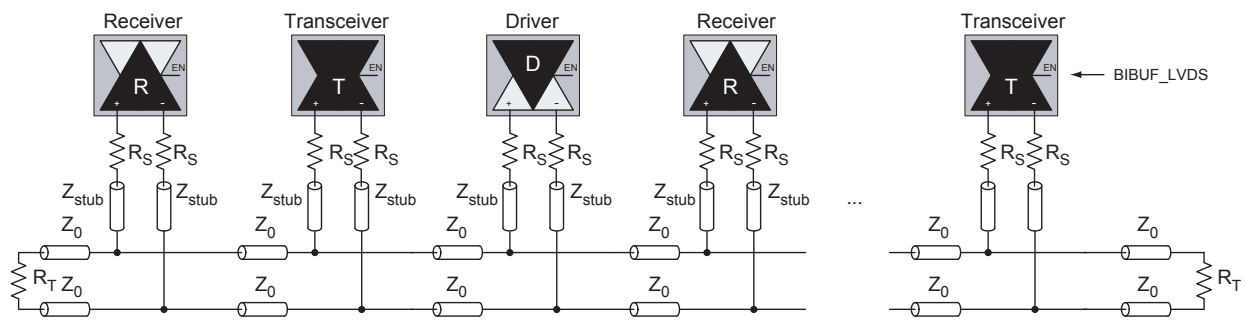


Figure 2-13 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-14](#) on page 2-52. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

Table 2-91 • Parameter Definitions and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-16 on page 2-55 for more information.

Output Register

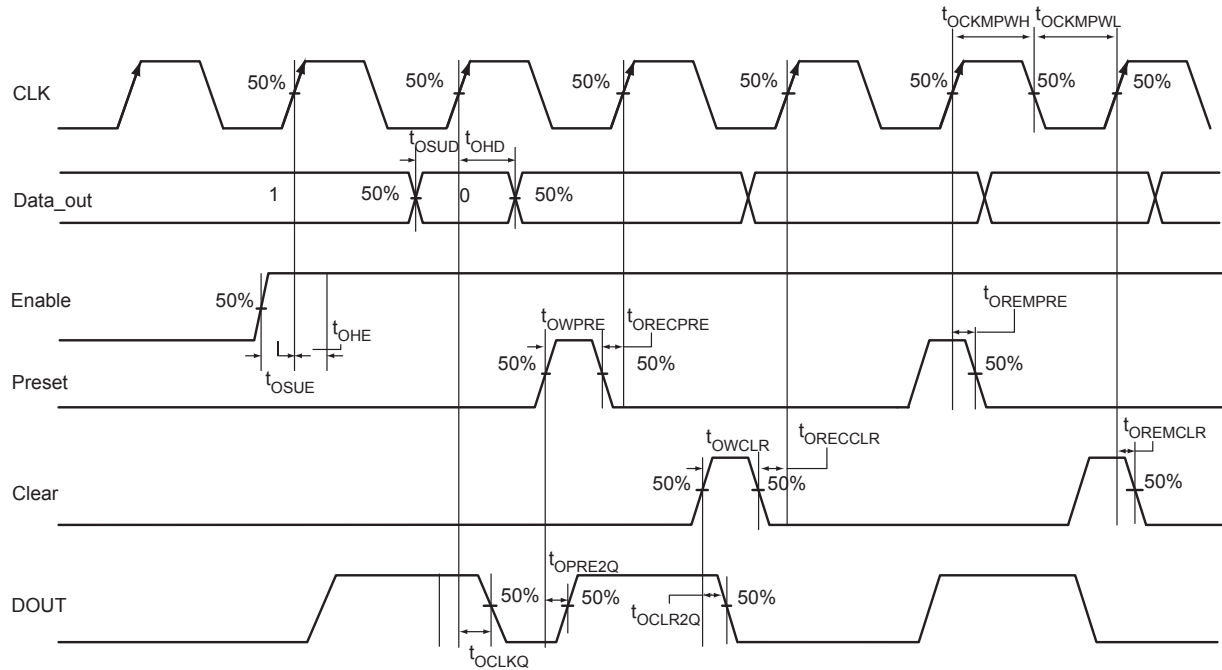


Figure 2-18 • Output Register Timing Diagram

Timing Characteristics

Table 2-94 • Output Data Register Propagation Delays
Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.72	0.84	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.38	0.45	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.53	0.63	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.98	1.15	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.98	1.15	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.32	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.32	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-95 • Output Data Register Propagation Delays
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.70	0.82	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.37	0.44	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.52	0.61	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.96	1.12	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.96	1.12	ns
t_{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.41	0.48	ns
t_{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-120 • RAM512X18
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.35	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN, WEN Setup Time	0.11	0.13	ns
t_{ENH}	REN, WEN Hold Time	0.07	0.08	ns
t_{DS}	Input data (WD) Setup Time	0.22	0.26	ns
t_{DH}	Input data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (output retained, WMODE = 0)	2.58	3.03	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.07	1.26	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.43	0.50	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.50	0.59	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.10	1.29	ns
	RESET Low to Data Out Low on RD (pipelined)	1.10	1.29	ns
$t_{REMRSTB}$	RESET Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET Recovery	1.79	2.10	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.25	0.30	ns
t_{CYC}	Clock Cycle Time	3.85	4.53	ns
F_{MAX}	Maximum Frequency	260	221	MHz

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Timing Waveforms

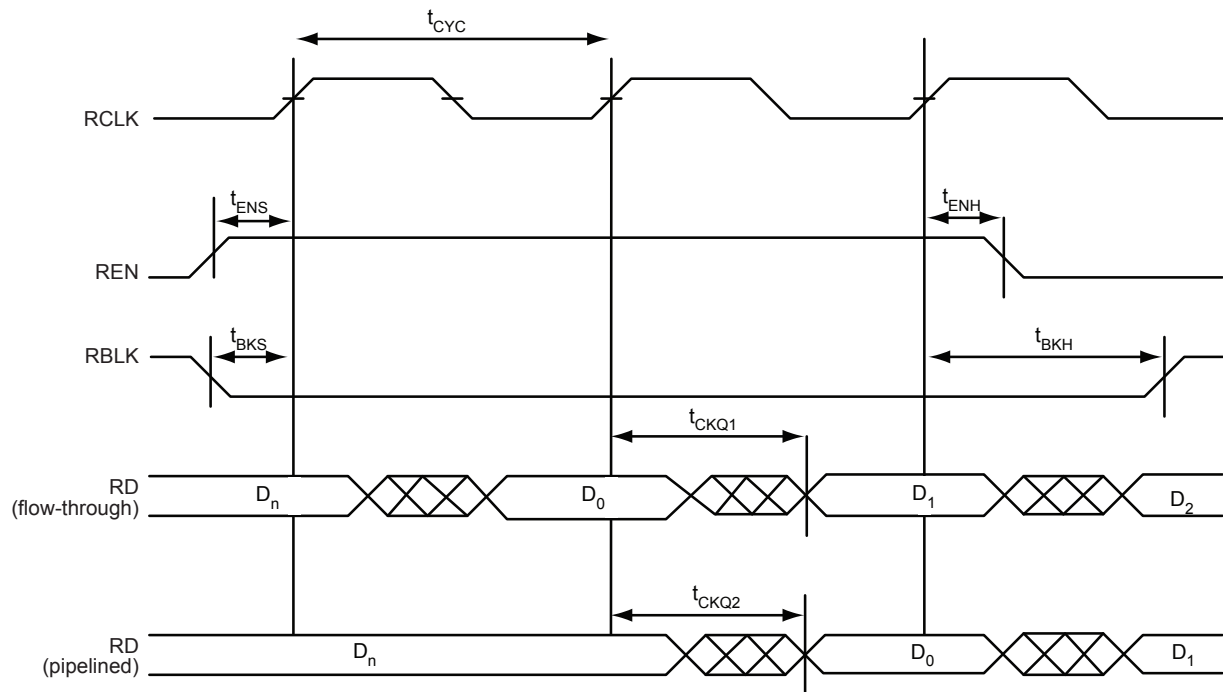


Figure 2-37 • FIFO Read

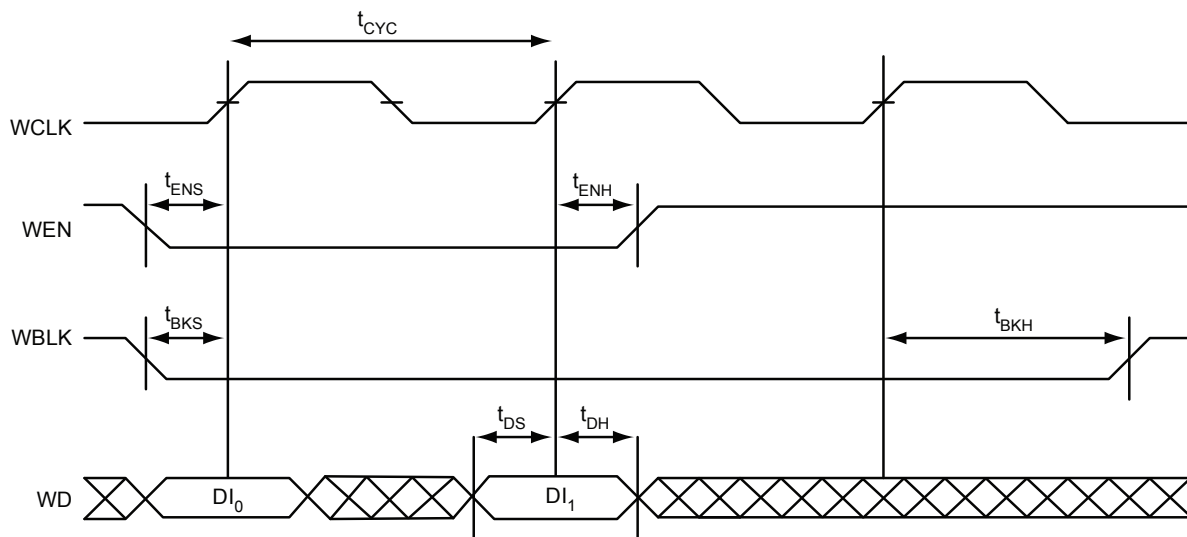


Figure 2-38 • FIFO Write

FG144	
Pin Number	A3P060 Function
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO57RSB1
K9	GDC2/IO56RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	VCCIB1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG144		FG144		FG144	
Pin Number	A3P250 Function	Pin Number	A3P250 Function	Pin Number	A3P250 Function
A1	GNDQ	D1	IO112NDB3	G1	GFA1/IO108PPB3
A2	VMV0	D2	IO112PDB3	G2	GND
A3	GAB0/IO02RSB0	D3	IO116VDB3	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO118UPB3	G4	GFA0/IO108NPB3
A5	IO16RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO29RSB0	D7	GBC0/IO35RSB0	G7	GND
A8	VCC	D8	GBC1/IO36RSB0	G8	GDC1/IO58UPB1
A9	IO33RSB0	D9	GBB2/IO42PDB1	G9	IO53NDB1
A10	GBA0/IO39RSB0	D10	IO42NDB1	G10	GCC2/IO53PDB1
A11	GBA1/IO40RSB0	D11	IO43NPB1	G11	IO52NDB1
A12	GNDQ	D12	GCB1/IO49PPB1	G12	GCB2/IO52PDB1
B1	GAB2/IO117UDB3	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO110NDB3	H2	GFB2/IO106PDB3
B3	GAA0/IO00RSB0	E3	GFC1/IO110PDB3	H3	GFC2/IO105PSB3
B4	GAA1/IO01RSB0	E4	VCCIB3	H4	GEC1/IO100PDB3
B5	IO14RSB0	E5	IO118VPB3	H5	VCC
B6	IO19RSB0	E6	VCCIB0	H6	IO79RSB2
B7	IO22RSB0	E7	VCCIB0	H7	IO65RSB2
B8	IO30RSB0	E8	GCC1/IO48PDB1	H8	GDB2/IO62RSB2
B9	GBB0/IO37RSB0	E9	VCCIB1	H9	GDC0/IO58VPB1
B10	GBB1/IO38RSB0	E10	VCC	H10	VCCIB1
B11	GND	E11	GCA0/IO50NDB1	H11	IO54PSB1
B12	VMV1	E12	IO51NDB1	H12	VCC
C1	IO117VDB3	F1	GFB0/IO109NPB3	J1	GEB1/IO99PDB3
C2	GFA2/IO107PPB3	F2	VCOMPLF	J2	IO106NDB3
C3	GAC2/IO116UDB3	F3	GFB1/IO109PPB3	J3	VCCIB3
C4	VCC	F4	IO107NPB3	J4	GEC0/IO100NDB3
C5	IO12RSB0	F5	GND	J5	IO88RSB2
C6	IO17RSB0	F6	GND	J6	IO81RSB2
C7	IO24RSB0	F7	GND	J7	VCC
C8	IO31RSB0	F8	GCC0/IO48NDB1	J8	TCK
C9	IO34RSB0	F9	GCB0/IO49NPB1	J9	GDA2/IO61RSB2
C10	GBA2/IO41PDB1	F10	GND	J10	TDO
C11	IO41NDB1	F11	GCA1/IO50PDB1	J11	GDA1/IO60UDB1
C12	GBC2/IO43PPB1	F12	GCA2/IO51PDB1	J12	GDB1/IO59UDB1

FG256	
Pin Number	A3P250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117UDB3
B2	GAA2/IO118UDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117VDB3
C2	IO118VDB3
C3	NC
C4	NC

FG256	
Pin Number	A3P250 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114VDB3
D2	IO114UDB3
D3	GAC2/IO116UDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116VDB3
E4	IO115UDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO19RSB0

FG256	
Pin Number	A3P250 Function
E9	IO24RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115VDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

FG256		FG256		FG256	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
A1	GND	C5	GAC0/IO04RSB0	E9	IO47RSB0
A2	GAA0/IO00RSB0	C6	GAC1/IO05RSB0	E10	VCCIB0
A3	GAA1/IO01RSB0	C7	IO25RSB0	E11	VCCIB0
A4	GAB0/IO02RSB0	C8	IO36RSB0	E12	VMV1
A5	IO16RSB0	C9	IO42RSB0	E13	GBC2/IO80PDB1
A6	IO22RSB0	C10	IO49RSB0	E14	IO83PPB1
A7	IO28RSB0	C11	IO56RSB0	E15	IO86PPB1
A8	IO35RSB0	C12	GBC0/IO72RSB0	E16	IO87PDB1
A9	IO45RSB0	C13	IO62RSB0	F1	IO217NDB3
A10	IO50RSB0	C14	VMV0	F2	IO218NDB3
A11	IO55RSB0	C15	IO78NDB1	F3	IO216PDB3
A12	IO61RSB0	C16	IO81NDB1	F4	IO216NDB3
A13	GBB1/IO75RSB0	D1	IO222NDB3	F5	VCCIB3
A14	GBA0/IO76RSB0	D2	IO222PDB3	F6	GND
A15	GBA1/IO77RSB0	D3	GAC2/IO223PDB3	F7	VCC
A16	GND	D4	IO223NDB3	F8	VCC
B1	GAB2/IO224PDB3	D5	GNDQ	F9	VCC
B2	GAA2/IO225PDB3	D6	IO23RSB0	F10	VCC
B3	GNDQ	D7	IO29RSB0	F11	GND
B4	GAB1/IO03RSB0	D8	IO33RSB0	F12	VCCIB1
B5	IO17RSB0	D9	IO46RSB0	F13	IO83NPB1
B6	IO21RSB0	D10	IO52RSB0	F14	IO86NPB1
B7	IO27RSB0	D11	IO60RSB0	F15	IO90PPB1
B8	IO34RSB0	D12	GNDQ	F16	IO87NDB1
B9	IO44RSB0	D13	IO80NDB1	G1	IO210PSB3
B10	IO51RSB0	D14	GBB2/IO79PDB1	G2	IO213NDB3
B11	IO57RSB0	D15	IO79NDB1	G3	IO213PDB3
B12	GBC1/IO73RSB0	D16	IO82NSB1	G4	GFC1/IO209PPB3
B13	GBB0/IO74RSB0	E1	IO217PDB3	G5	VCCIB3
B14	IO71RSB0	E2	IO218PDB3	G6	VCC
B15	GBA2/IO78PDB1	E3	IO221NDB3	G7	GND
B16	IO81PDB1	E4	IO221PDB3	G8	GND
C1	IO224NDB3	E5	VMV0	G9	GND
C2	IO225NDB3	E6	VCCIB0	G10	GND
C3	VMV3	E7	VCCIB0	G11	VCC
C4	IO11RSB0	E8	IO38RSB0	G12	VCCIB1

FG256	
Pin Number	A3P1000 Function
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1

FG256	
Pin Number	A3P1000 Function
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3

FG256	
Pin Number	A3P1000 Function
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2

FG484		FG484		FG484	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
K19	IO88NDB1	M11	GND	P3	IO199NDB3
K20	IO94NPB1	M12	GND	P4	IO202NDB3
K21	IO98NDB1	M13	GND	P5	IO202PDB3
K22	IO98PDB1	M14	VCC	P6	IO196PPB3
L1	NC	M15	GCB2/IO95PPB1	P7	IO193PPB3
L2	IO200PDB3	M16	GCA1/IO93PPB1	P8	VCCIB3
L3	IO210NPB3	M17	GCC2/IO96PPB1	P9	GND
L4	GFB0/IO208NPB3	M18	IO100PPB1	P10	VCC
L5	GFA0/IO207NDB3	M19	GCA2/IO94PPB1	P11	VCC
L6	GFB1/IO208PPB3	M20	IO101PPB1	P12	VCC
L7	VCOMPLF	M21	IO99PPB1	P13	VCC
L8	GFC0/IO209NPB3	M22	NC	P14	GND
L9	VCC	N1	IO201NDB3	P15	VCCIB1
L10	GND	N2	IO201PDB3	P16	GDB0/IO112NPB1
L11	GND	N3	NC	P17	IO106NDB1
L12	GND	N4	GFC2/IO204PDB3	P18	IO106PDB1
L13	GND	N5	IO204NDB3	P19	IO107PDB1
L14	VCC	N6	IO203NDB3	P20	NC
L15	GCC0/IO91NPB1	N7	IO203PDB3	P21	IO104PDB1
L16	GCB1/IO92PPB1	N8	VCCIB3	P22	IO103NDB1
L17	GCA0/IO93NPB1	N9	VCC	R1	NC
L18	IO96NPB1	N10	GND	R2	IO197PPB3
L19	GCB0/IO92NPB1	N11	GND	R3	VCC
L20	IO97PDB1	N12	GND	R4	IO197NPB3
L21	IO97NDB1	N13	GND	R5	IO196NPB3
L22	IO99NPB1	N14	VCC	R6	IO193NPB3
M1	NC	N15	VCCIB1	R7	GEC0/IO190NPB3
M2	IO200NDB3	N16	IO95NPB1	R8	VMV3
M3	IO206NDB3	N17	IO100NPB1	R9	VCCIB2
M4	GFA2/IO206PDB3	N18	IO102NDB1	R10	VCCIB2
M5	GFA1/IO207PDB3	N19	IO102PDB1	R11	IO147RSB2
M6	VCCPLF	N20	NC	R12	IO136RSB2
M7	IO205NDB3	N21	IO101NPB1	R13	VCCIB2
M8	GFB2/IO205PDB3	N22	IO103PDB1	R14	VCCIB2
M9	VCC	P1	NC	R15	VMV2
M10	GND	P2	IO199PDB3	R16	IO110NDB1



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