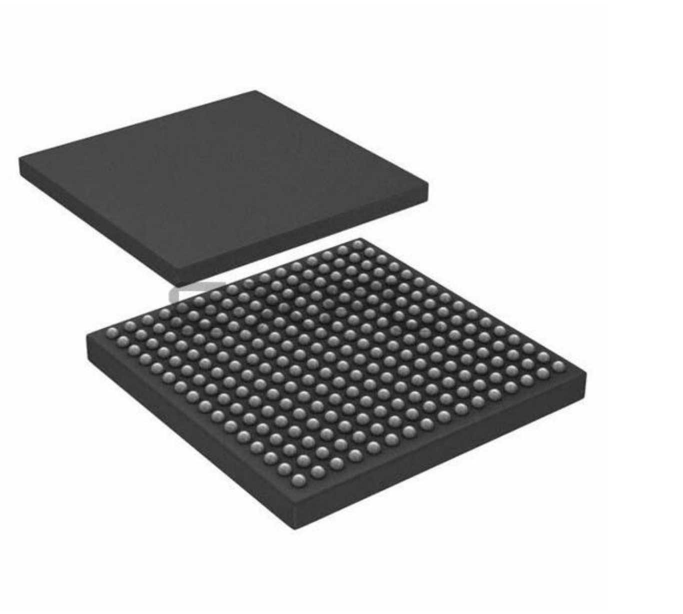


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-fg256t

Temperature Grade Offerings

Package	A3P060	A3P125	A3P250	A3P1000
VQ100	C, I, T	C, I, T	C, I, T	–
FG144	C, I, T	C, I, T	C, I, T	C, I, T
FG256	–	–	C, I, T	C, I, T
FG484	–	–	–	C, I, T
QNG132	–	C, I, T	C, I, T	–

Notes:
1. *C = Commercial temperature range: 0°C to 70°C*
2. *I = Industrial temperature range: –40°C to 85°C*
3. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
4. *Specifications for Commercial and Industrial grade devices can be found in the* ProASIC3 Flash Family FPGAs *datasheet.*

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
T (Grade 1 and Grade 2), Commercial, Industrial	3	3

Notes:
1. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
2. *Specifications for Commercial and Industrial grade devices can be found in the* ProASIC3 Flash Family FPGAs *datasheet.*

Contact your local Microsemi SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

Table of Contents

Automotive ProASIC3 Device Family Overview

General Description . . . 1-1

Automotive ProASIC3 DC and Switching Characteristics

General Specifications . . . 2-1
Calculating Power Dissipation . . . 2-6
User I/O Characteristics . . . 2-12
VersaTile Characteristics . . . 2-69
Global Resource Characteristics . . . 2-75
Clock Conditioning Circuits . . . 2-80
Embedded SRAM and FIFO Characteristics . . . 2-82
Embedded FlashROM Characteristics . . . 2-96
JTAG 1532 Characteristics . . . 2-97

Pin Descriptions and Packaging

Supply Pins . . . 3-1
User Pins . . . 3-2
JTAG Pins . . . 3-3
Special Function Pins . . . 3-4
Packaging . . . 3-4
Related Documents . . . 3-4

Package Pin Assignments

VQ100 . . . 4-1
QN132 . . . 4-5
FG144 . . . 4-10
FG256 . . . 4-19
FG484 . . . 4-26

Datasheet Information

List of Changes . . . 5-1
Datasheet Categories . . . 5-4
Safety Critical, Life Support, and High-Reliability Applications Policy . . . 5-4

Total Static Power Consumption—P_{STAT}

$$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution—P_{CLOCK}

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Automotive ProASIC3 FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the *Automotive ProASIC3 FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-13 on page 2-12.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-13 on page 2-12.

PLL Contribution—P_{PLL}

$$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-12 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

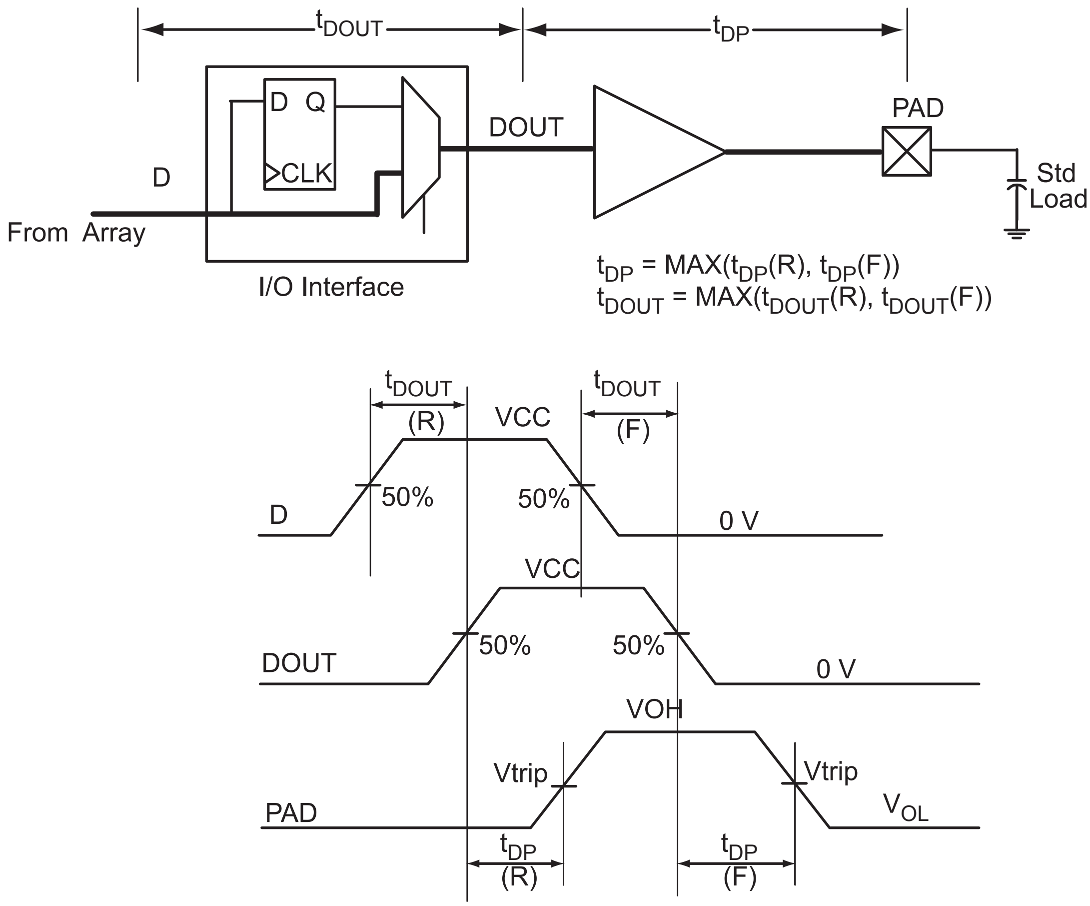


Figure 2-5 • **Output Buffer Model and Delays (example)**

Table 2-60 • **1.8 V LVCMOS Low Slew**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	17.36	0.05	1.45	0.46	15.09	16.55	1.24	0.79	17.59	19.052	ns
	-1	0.55	14.77	0.04	1.23	0.39	12.84	14.08	1.24	0.79	14.96	16.207	ns
4 mA	STD	0.64	11.71	0.05	1.45	0.46	10.88	11.07	1.47	1.35	13.38	13.567	ns
	-1	0.55	9.96	0.04	1.23	0.39	9.26	9.41	1.47	1.35	11.38	11.541	ns
6 mA	STD	0.64	9.00	0.05	1.45	0.46	8.47	8.18	1.62	1.62	10.97	10.685	ns
	-1	0.55	7.66	0.04	1.23	0.39	7.21	6.96	1.62	1.62	9.33	9.089	ns
8 mA	STD	0.64	8.39	0.05	1.45	0.46	8.47	8.18	1.62	1.62	10.97	10.685	ns
	-1	0.55	7.14	0.04	1.23	0.39	7.21	6.96	1.62	1.62	9.33	9.089	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-61 • **1.8 V LVCMOS High Slew**
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	12.83	0.05	1.32	0.45	9.88	12.83	1.48	0.87	12.30	15.25	ns
	-1	0.53	10.92	0.04	1.12	0.38	8.41	10.92	1.48	0.87	10.46	12.97	ns
4 mA	STD	0.63	7.48	0.05	1.32	0.45	6.34	7.48	1.72	1.49	8.76	9.90	ns
	-1	0.53	6.36	0.04	1.12	0.38	5.39	6.36	1.72	1.49	7.45	8.42	ns
6 mA	STD	0.63	4.81	0.05	1.32	0.45	4.52	4.81	1.89	1.77	6.94	7.23	ns
	-1	0.53	4.09	0.04	1.12	0.38	3.85	4.09	1.89	1.77	5.90	6.15	ns
8 mA	STD	0.63	4.25	0.05	1.32	0.45	4.25	4.25	1.92	1.85	6.67	6.66	ns
	-1	0.53	3.61	0.04	1.12	0.38	3.61	3.61	1.93	1.85	5.67	5.67	ns
12 mA	STD	0.63	3.82	0.05	1.32	0.45	1.89	1.63	4.00	4.41	3.06	2.82	ns
	-1	0.53	3.25	0.04	1.12	0.38	1.89	1.63	3.41	3.75	3.06	2.82	ns
16 mA	STD	0.63	3.82	0.05	1.32	0.45	1.89	1.63	4.00	4.41	3.06	2.82	ns
	-1	0.53	3.25	0.04	1.12	0.38	1.89	1.63	3.41	3.75	3.06	2.82	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

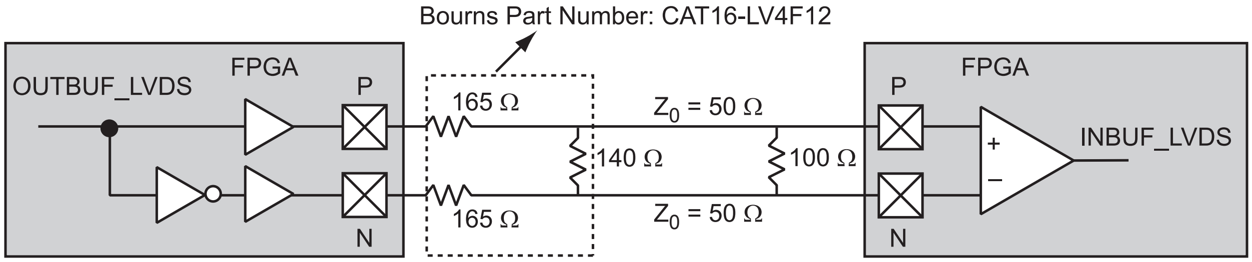


Figure 2-12 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 2-82 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
VI	Input Voltage	0	–	2.925	V
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common-Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common-Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350	–	mV

Table 2-83 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

*Note: *Measuring point = Vtrip. See Table 2-18 on page 2-17 for a complete table of trip points.*

Timing Characteristics

Table 2-84 • **LVDS**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.64	2.05	0.05	1.79	ns
–1	0.55	1.74	0.04	1.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-85 • **LVDS**
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.63	1.98	0.05	1.73	ns
–1	0.53	1.68	0.04	1.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-93 • Input Data Register Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.29	0.34	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.31	0.37	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.44	0.52	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.54	0.64	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.54	0.64	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.27	0.31	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.27	0.31	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Output Enable Register

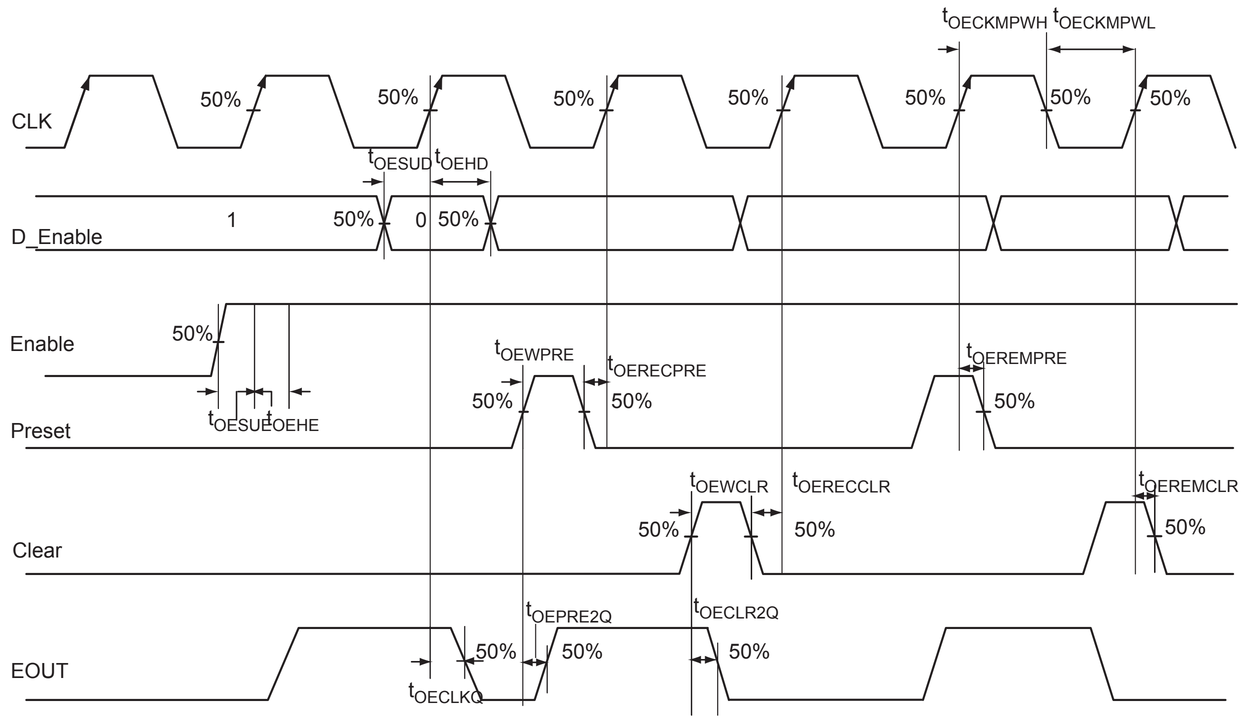


Figure 2-19 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-96 • Output Enable Register Propagation Delays
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.54	0.64	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.38	0.45	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.53	0.62	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.32	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.32	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-97 • Output Enable Register Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.53	0.62	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.37	0.44	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.52	0.61	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.79	0.93	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.79	0.93	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.31	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.31	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e and ProASIC3/E Macro Library Guide*.

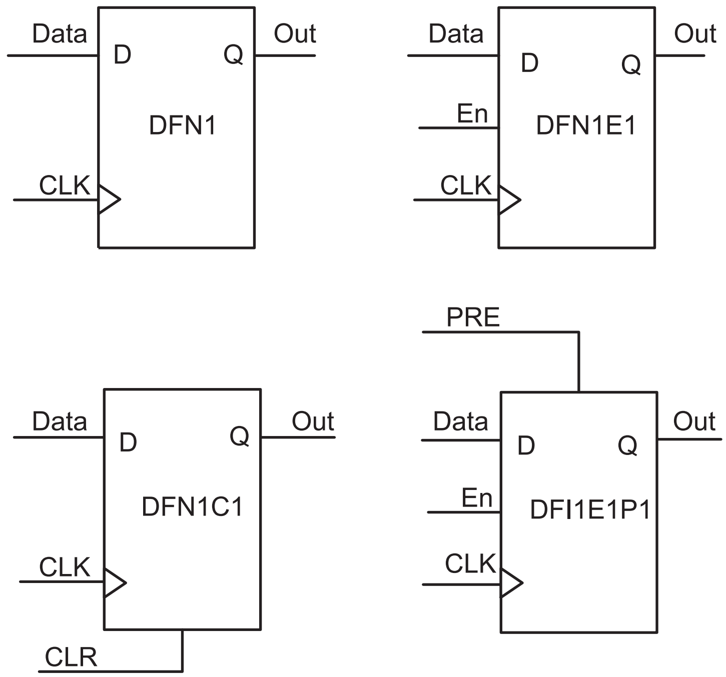
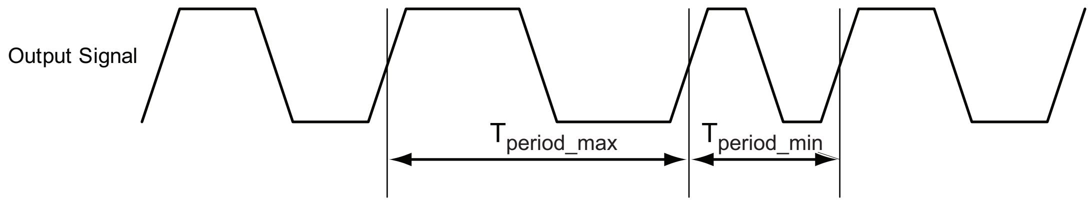


Figure 2-26 • **Sample of Sequential Cells**



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-29 • **Peak-to-Peak Jitter Definition**

Timing Characteristics

Table 2-117 • RAM4K9
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.36	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN, WEN Setup Time	0.17	0.20	ns
t_{ENH}	REN, WEN Hold Time	0.12	0.14	ns
t_{BKS}	BLK Setup Time	0.28	0.33	ns
t_{BKH}	BLK Hold Time	0.02	0.03	ns
t_{DS}	Input Data (DIN) Setup Time	0.22	0.26	ns
t_{DH}	Input Data (DIN) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DOUT (output retained, WMODE = 0)	2.17	2.55	ns
	Clock High to New Data Valid on DOUT (flow-through, WMODE = 1)	2.86	3.37	ns
t_{CKQ2}	Clock High to New Data Valid on DOUT (pipelined)	1.09	1.28	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.28	0.33	ns
t_{C2CWWH}[1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.26	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.38	0.45	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.42	0.49	ns
t_{RSTBQ}	RESET Low to Data Out Low on DO (flow-through)	1.12	1.32	ns
	RESET Low to Data Out Low on DO (pipelined)	1.12	1.32	ns
$t_{REMRSTB}$	RESET Removal	0.35	0.41	ns
$t_{RECRSTB}$	RESET Recovery	1.82	2.14	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.26	0.30	ns
t_{CYC}	Clock Cycle Time	3.93	4.62	ns
F_{MAX}	Maximum Frequency	255	217	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to* *Table 2-5 on page 2-5* *for derating values.*

insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

Automotive ProASIC3 devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *Automotive ProASIC3 FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter of the *Automotive ProASIC3 FPGA Fabric User's Guide* for an explanation of the naming of global pins.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Actel offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

User's Guides

Automotive ProASIC FPGA Fabric User's Guide

http://www.microsemi.com/soc/documents/PA3_Auto_UG.pdf

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsmei.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/soc/documents/PckgMechDrwngs.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Actel. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials: http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

VQ100	
Pin Number	A3P250 Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2

VQ100	
Pin Number	A3P250 Function
35	IO85RSB2
36	IO84RSB2
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC

VQ100	
Pin Number	A3P250 Function
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

QN132	
Pin Number	A3P250 Function
A1	GAB2/IO117UPB3
A2	IO117VPB3
A3	VCCIB3
A4	GFC1/IO110PDB3
A5	GFB0/IO109NPB3
A6	VCCPLF
A7	GFA1/IO108PPB3
A8	GFC2/IO105PPB3
A9	IO103NDB3
A10	VCC
A11	GEA1/IO98PPB3
A12	GEA0/IO98NPB3
A13	GEC2/IO95RSB2
A14	IO91RSB2
A15	VCC
A16	IO90RSB2
A17	IO87RSB2
A18	IO85RSB2
A19	IO82RSB2
A20	IO76RSB2
A21	IO70RSB2
A22	VCC
A23	GDB2/IO62RSB2
A24	TDI
A25	TRST
A26	GDC1/IO58UDB1
A27	VCC
A28	IO54NDB1
A29	IO52NDB1
A30	GCA2/IO51PPB1
A31	GCA0/IO50NPB1
A32	GCB1/IO49PDB1
A33	IO47NSB1
A34	VCC
A35	IO41NPB1
A36	GBA2/IO41PPB1

QN132	
Pin Number	A3P250 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO118VDB3
B2	GAC2/IO116UDB3
B3	GND
B4	GFC0/IO110NDB3
B5	VCOMPLF
B6	GND
B7	GFB2/IO106PSB3
B8	IO103PDB3
B9	GND
B10	GEB0/IO99NDB3
B11	VMV3
B12	GEB2/IO96RSB2
B13	IO92RSB2
B14	GND
B15	IO89RSB2
B16	IO86RSB2
B17	GND
B18	IO78RSB2
B19	IO72RSB2
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO58VDB1

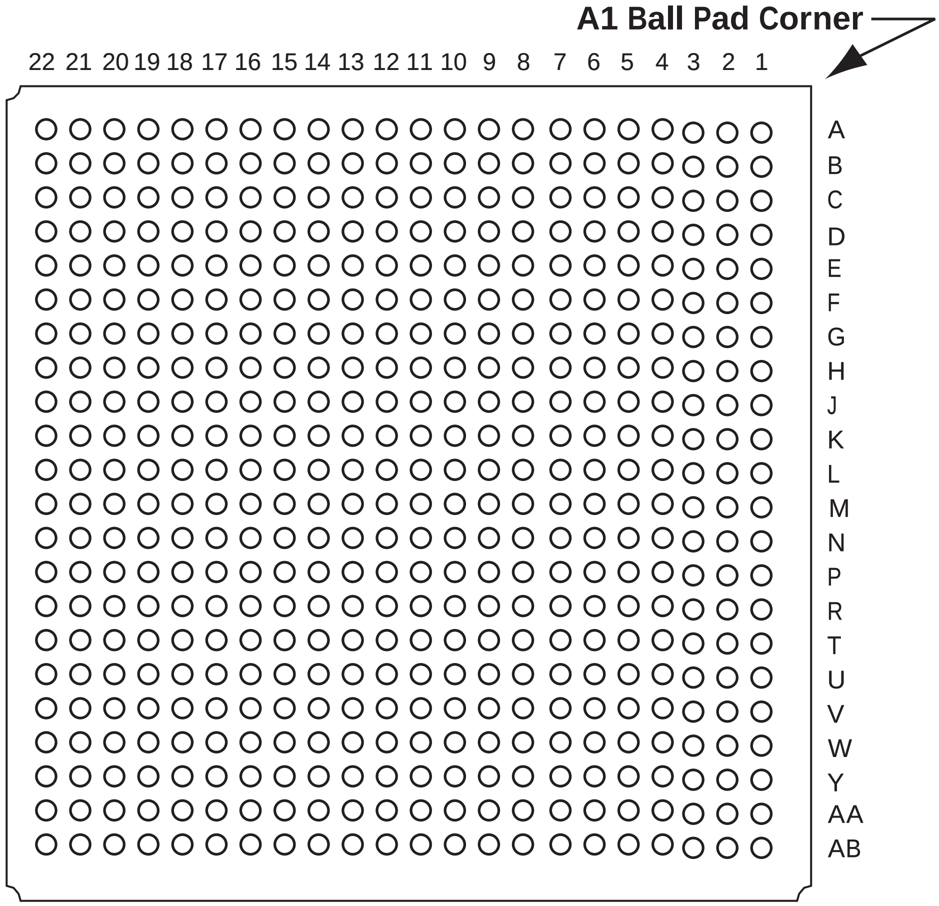
QN132	
Pin Number	A3P250 Function
B25	GND
B26	IO54PDB1
B27	GCB2/IO52PDB1
B28	GND
B29	GCB0/IO49NDB1
B30	GCC1/IO48PDB1
B31	GND
B32	GBB2/IO42PDB1
B33	VMV1
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO118UDB3
C2	IO116VDB3
C3	VCC
C4	GFB1/IO109PPB3
C5	GFA0/IO108NPB3
C6	GFA2/IO107PSB3
C7	IO105NPB3
C8	VCCIB3
C9	GEB1/IO99PDB3
C10	GNDQ
C11	GEA2/IO97RSB2
C12	IO94RSB2
C13	VCCIB2
C14	IO88RSB2
C15	IO84RSB2
C16	IO80RSB2

FG144	
Pin Number	A3P125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	A3P125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	A3P125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.