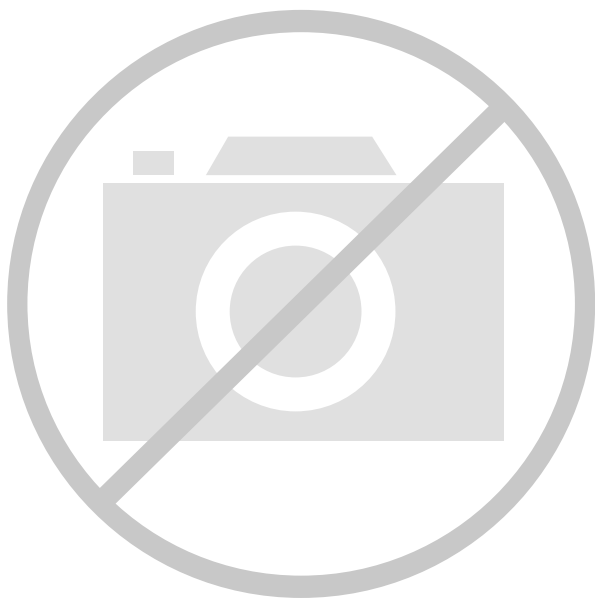




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	300
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-fgg484t

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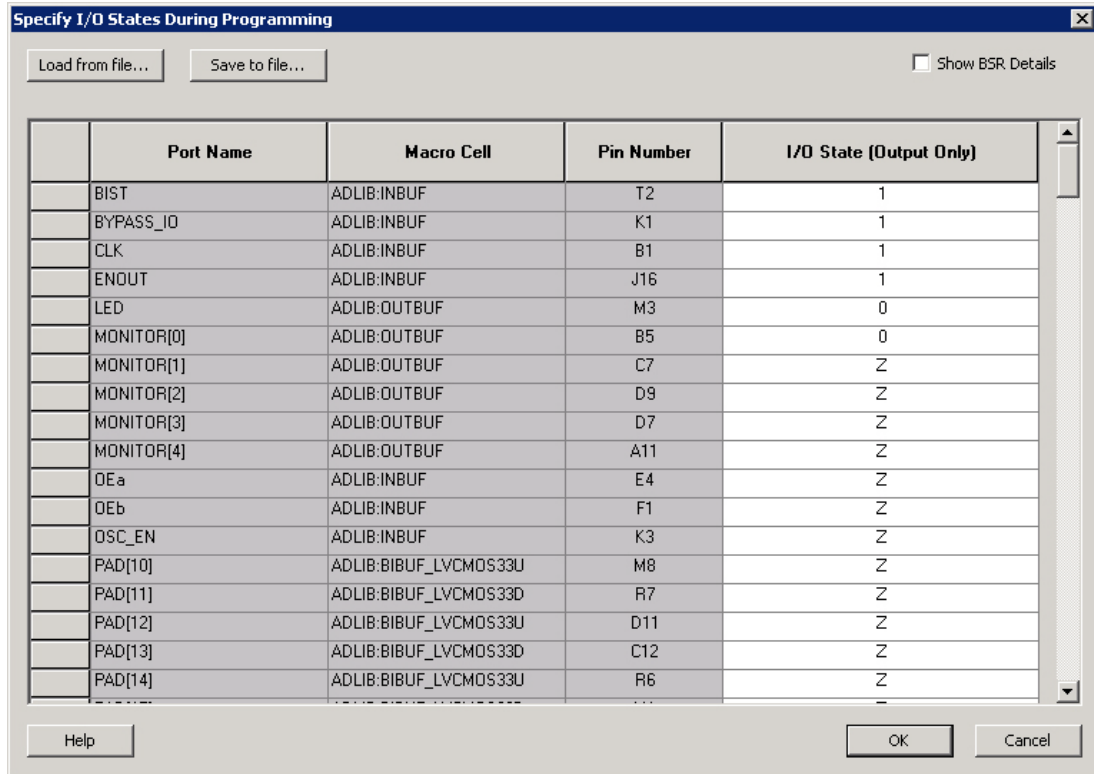
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5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 – I/O is set to drive out logic High
 - 0 – I/O is set to drive out logic Low
 - Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming
 - Z -Tristate: I/O is tristated



The window titled "Specify I/O States During Programming" contains a table with the following data:

	Port Name	Macro Cell	Pin Number	I/O State (Output Only)
	BIST	ADLIB:INBUF	T2	1
	BYPASS_I0	ADLIB:INBUF	K1	1
	CLK	ADLIB:INBUF	B1	1
	ENOUT	ADLIB:INBUF	J16	1
	LED	ADLIB:OUTBUF	M3	0
	MONITOR[0]	ADLIB:OUTBUF	B5	0
	MONITOR[1]	ADLIB:OUTBUF	C7	Z
	MONITOR[2]	ADLIB:OUTBUF	D9	Z
	MONITOR[3]	ADLIB:OUTBUF	D7	Z
	MONITOR[4]	ADLIB:OUTBUF	A11	Z
	OEa	ADLIB:INBUF	E4	Z
	OEb	ADLIB:INBUF	F1	Z
	OSC_EN	ADLIB:INBUF	K3	Z
	PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
	PAD[11]	ADLIB:BIBUF_LVCMOS33D	R7	Z
	PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
	PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
	PAD[14]	ADLIB:BIBUF_LVCMOS33U	R6	Z

The window also includes buttons for "Load from file...", "Save to file...", "Show BSR Details" (checkbox), "Help", "OK", and "Cancel".

Figure 1-4 • I/O States During Programming Window

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the [Automotive ProASIC3 FPGA Fabric User's Guide](#).

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the [Automotive ProASIC3 FPGA Fabric User's Guide](#).

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

N_{S-CELL} is the number VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

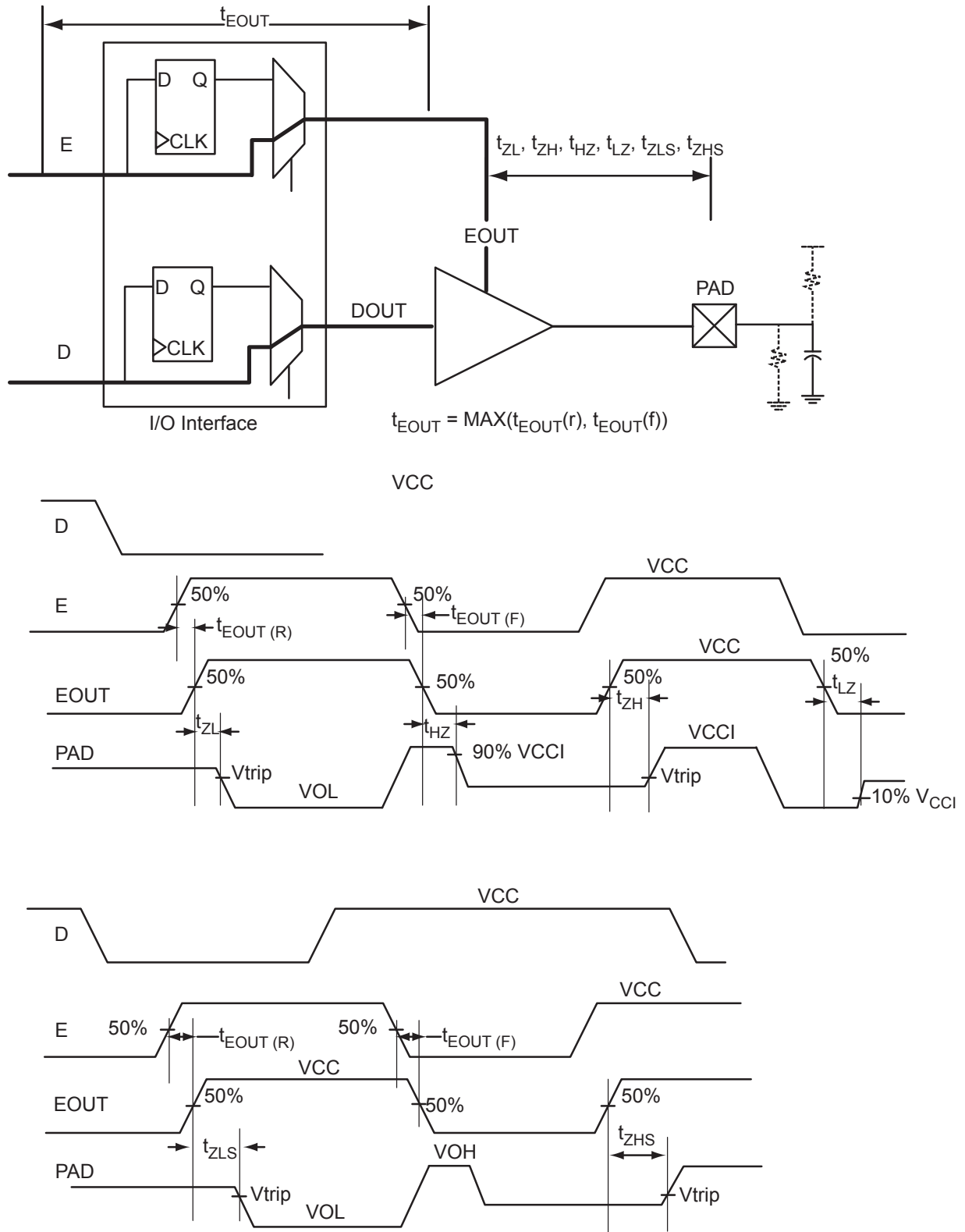


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (example)

Detailed I/O DC Characteristics

Table 2-24 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF

Table 2-25 • I/O Output Buffer Maximum Resistances¹
Applicable to Advanced I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	6 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / I_{OH_{spec}}$

Table 2-28 • I/O Short Currents IOSH/IOSL
Applicable to Advanced I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	6 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: * $T_J = 100^{\circ}\text{C}$

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-54 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	2	2	11	9	10	10
4 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	4	4	22	17	10	10
6 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	6	6	44	35	10	10
8 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	8	8	51	45	10	10
12 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	12	12	74	91	10	10
16 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	16	16	74	91	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-55 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	2	2	11	9	10	10
4 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	4	4	22	17	10	10
6 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	6	6	44	35	10	10
8 mA	−0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} − 0.45	8	8	44	35	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

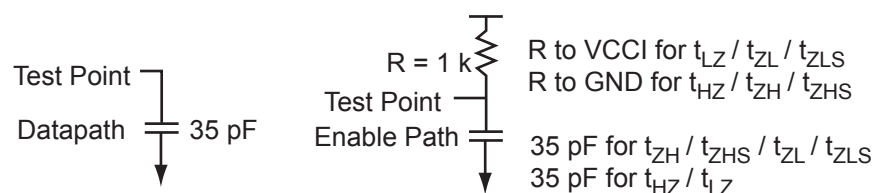


Figure 2-9 • AC Loading

Table 2-56 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.8	0.9	35

Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.

Table 2-66 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
2 mA	−0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	2	2	0	0	10	10
4 mA	−0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	4	4	0	0	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

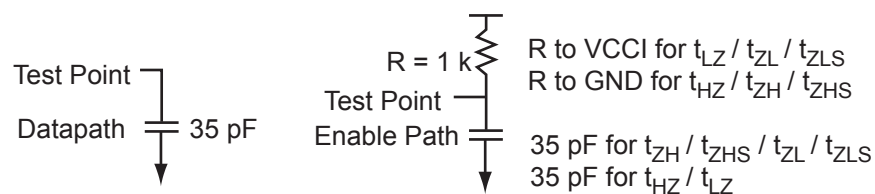


Figure 2-10 • AC Loading

Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	35

Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.

Timing Characteristics

Table 2-68 • 1.5 V LVCMOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.35	0.05	1.61	0.46	7.63	9.35	1.87	1.50	10.13	11.851	ns
	-1	0.55	7.95	0.04	1.37	0.39	6.49	7.95	1.87	1.50	8.62	10.081	ns
4 mA	STD	0.64	5.94	0.05	1.61	0.46	5.42	5.94	2.07	1.84	7.92	8.442	ns
	-1	0.55	5.05	0.04	1.37	0.39	4.61	5.05	2.07	1.85	6.74	7.181	ns
6 mA	STD	0.64	5.22	0.05	1.61	0.46	5.09	5.22	2.11	1.93	7.59	7.718	ns
	-1	0.55	4.44	0.04	1.37	0.39	4.33	4.44	2.11	1.93	6.45	6.566	ns
8 mA	STD	0.64	4.56	0.05	1.61	0.46	2.25	1.98	4.41	4.70	3.46	3.211	ns
	-1	0.55	3.88	0.04	1.37	0.39	2.25	1.98	3.75	4.00	3.46	3.213	ns
12 mA	STD	0.64	4.56	0.05	1.61	0.46	2.25	1.98	4.41	4.70	3.46	3.211	ns
	-1	0.55	3.88	0.04	1.37	0.39	2.25	1.98	3.75	4.00	3.46	3.213	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-69 • 1.5 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	14.29	0.05	1.45	0.46	14.32	14.29	1.88	1.43	16.82	16.794	ns
	-1	0.55	12.16	0.04	1.23	0.39	12.18	12.16	1.88	1.43	14.31	14.286	ns
4 mA	STD	0.64	11.19	0.05	1.45	0.46	11.40	10.67	2.07	1.77	13.90	13.175	ns
	-1	0.55	9.52	0.04	1.23	0.39	9.70	9.08	2.07	1.77	11.82	11.207	ns
6 mA	STD	0.64	10.44	0.05	1.45	0.46	10.63	9.94	2.12	1.86	13.13	12.442	ns
	-1	0.55	8.88	0.04	1.23	0.39	9.04	8.46	2.12	1.86	11.17	10.584	ns
8 mA	STD	0.64	9.96	0.05	1.45	0.46	10.15	9.94	2.18	2.19	12.65	12.445	ns
	-1	0.55	8.47	0.04	1.23	0.39	8.63	8.46	2.19	2.20	10.76	10.586	ns
12 mA	STD	0.64	9.96	0.05	1.45	0.46	10.15	9.94	2.18	2.19	12.65	12.445	ns
	-1	0.55	8.47	0.04	1.23	0.39	8.63	8.46	2.19	2.20	10.76	10.586	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-90 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{iCLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{iSUD}	Data Setup Time for the Input Data Register	C, A
t_{iHD}	Data Hold Time for the Input Data Register	C, A
t_{iSUE}	Enable Setup Time for the Input Data Register	B, A
t_{iHE}	Enable Hold Time for the Input Data Register	B, A
t_{iPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-15 on page 2-53 for more information.

Table 2-93 • Input Data Register Propagation Delays
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Input Data Register	0.29	0.34	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.31	0.37	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.44	0.52	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.54	0.64	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.54	0.64	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.27	0.31	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.27	0.31	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Input Data Register	0.41	0.48	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Input Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

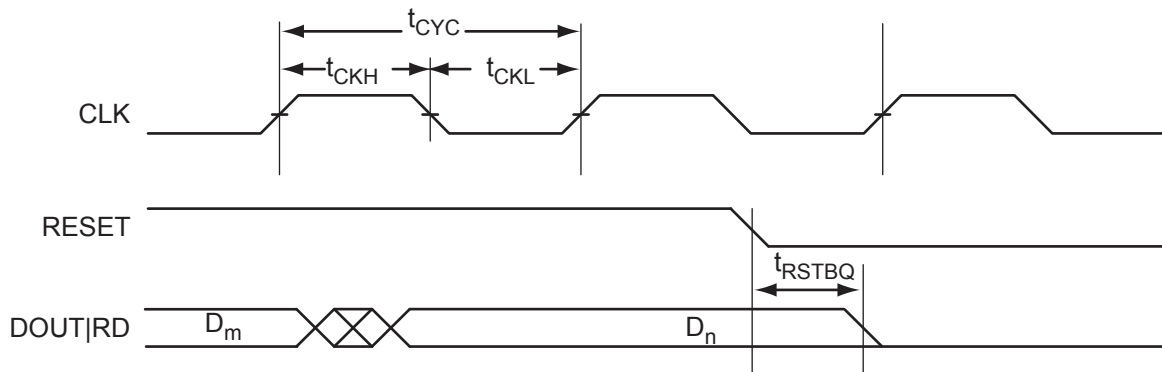


Figure 2-35 • RAM Reset. Applicable to Both RAM4K9 and RAM512x18

insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP **Programming Supply Voltage**

Automotive ProASIC3 devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the [Automotive ProASIC3 FPGA Fabric User's Guide](#). All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

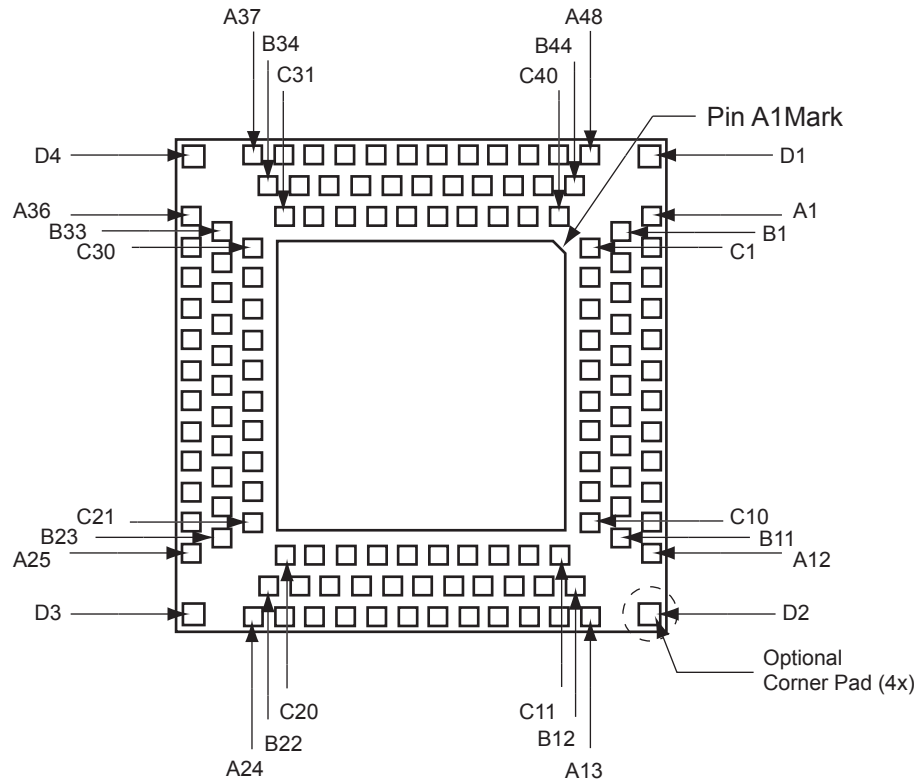
Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter of the [Automotive ProASIC3 FPGA Fabric User's Guide](#) for an explanation of the naming of global pins.

VQ100	
Pin Number	A3P060 Function
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1

VQ100	
Pin Number	A3P060 Function
35	IO62RSB1
36	IO61RSB1
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC

VQ100	
Pin Number	A3P060 Function
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

QN132



Notes:

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

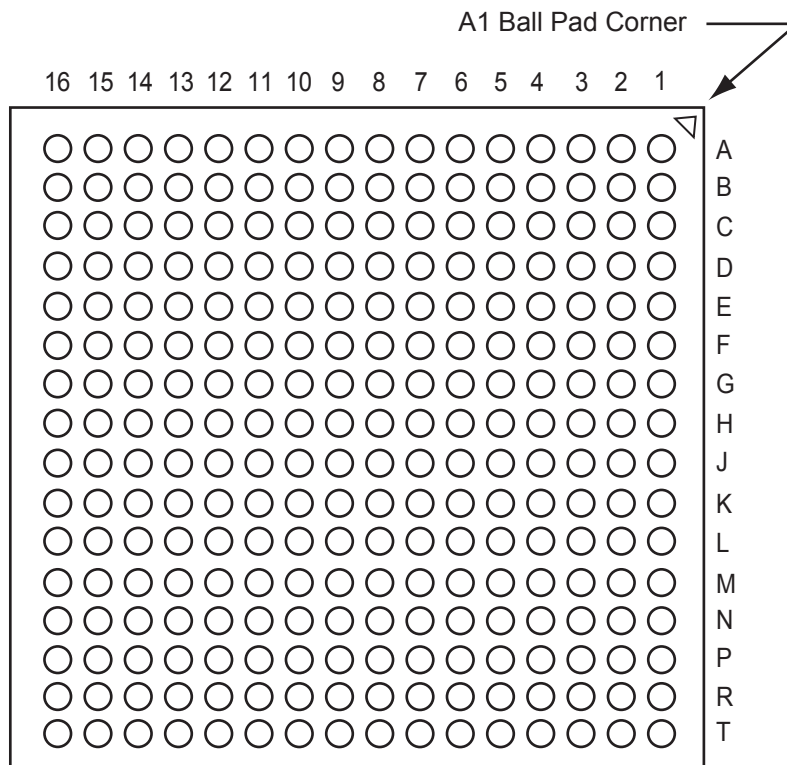
Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

FG144		FG144		FG144	
Pin Number	A3P060 Function	Pin Number	A3P060 Function	Pin Number	A3P060 Function
A1	GNDQ	D1	IO91RSB1	G1	GFA1/IO84RSB1
A2	VMV0	D2	IO92RSB1	G2	GND
A3	GAB0/IO04RSB0	D3	IO93RSB1	G3	VCCPLF
A4	GAB1/IO05RSB0	D4	GAA2/IO51RSB1	G4	GFA0/IO85RSB1
A5	IO08RSB0	D5	GAC0/IO06RSB0	G5	GND
A6	GND	D6	GAC1/IO07RSB0	G6	GND
A7	IO11RSB0	D7	GBC0/IO19RSB0	G7	GND
A8	VCC	D8	GBC1/IO20RSB0	G8	GDC1/IO45RSB0
A9	IO16RSB0	D9	GBB2/IO27RSB0	G9	IO32RSB0
A10	GBA0/IO23RSB0	D10	IO18RSB0	G10	GCC2/IO43RSB0
A11	GBA1/IO24RSB0	D11	IO28RSB0	G11	IO31RSB0
A12	GNDQ	D12	GCB1/IO37RSB0	G12	GCB2/IO42RSB0
B1	GAB2/IO53RSB1	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO88RSB1	H2	GFB2/IO82RSB1
B3	GAA0/IO02RSB0	E3	GFC1/IO89RSB1	H3	GFC2/IO81RSB1
B4	GAA1/IO03RSB0	E4	VCCIB1	H4	GEC1/IO77RSB1
B5	IO00RSB0	E5	IO52RSB1	H5	VCC
B6	IO10RSB0	E6	VCCIB0	H6	IO34RSB0
B7	IO12RSB0	E7	VCCIB0	H7	IO44RSB0
B8	IO14RSB0	E8	GCC1/IO35RSB0	H8	GDB2/IO55RSB1
B9	GBB0/IO21RSB0	E9	VCCIB0	H9	GDC0/IO46RSB0
B10	GBB1/IO22RSB0	E10	VCC	H10	VCCIB0
B11	GND	E11	GCA0/IO40RSB0	H11	IO33RSB0
B12	VMV0	E12	IO30RSB0	H12	VCC
C1	IO95RSB1	F1	GFB0/IO86RSB1	J1	GEB1/IO75RSB1
C2	GFA2/IO83RSB1	F2	VCOMPLF	J2	IO78RSB1
C3	GAC2/IO94RSB1	F3	GFB1/IO87RSB1	J3	VCCIB1
C4	VCC	F4	IO90RSB1	J4	GEC0/IO76RSB1
C5	IO01RSB0	F5	GND	J5	IO79RSB1
C6	IO09RSB0	F6	GND	J6	IO80RSB1
C7	IO13RSB0	F7	GND	J7	VCC
C8	IO15RSB0	F8	GCC0/IO36RSB0	J8	TCK
C9	IO17RSB0	F9	GCB0/IO38RSB0	J9	GDA2/IO54RSB1
C10	GBA2/IO25RSB0	F10	GND	J10	TDO
C11	IO26RSB0	F11	GCA1/IO39RSB0	J11	GDA1/IO49RSB0
C12	GBC2/IO29RSB0	F12	GCA2/IO41RSB0	J12	GDB1/IO47RSB0

FG144	
Pin Number	A3P250 Function
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	GEB2/IO96RSB2
L4	IO91RSB2
L5	VCCIB2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG256



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

FG256		FG256		FG256	
Pin Number	A3P250 Function	Pin Number	A3P250 Function	Pin Number	A3P250 Function
G13	GCC1/IO48PPB1	K1	GFC2/IO105PDB3	M5	VMV3
G14	IO47NPB1	K2	IO107NPB3	M6	VCCIB2
G15	IO54PDB1	K3	IO104PPB3	M7	VCCIB2
G16	IO54NDB1	K4	NC	M8	NC
H1	GFB0/IO109NPB3	K5	VCCIB3	M9	IO74RSB2
H2	GFA0/IO108NDB3	K6	VCC	M10	VCCIB2
H3	GFB1/IO109PPB3	K7	GND	M11	VCCIB2
H4	VCOMPLF	K8	GND	M12	VMV2
H5	GFC0/IO110NPB3	K9	GND	M13	NC
H6	VCC	K10	GND	M14	GDB1/IO59UPB1
H7	GND	K11	VCC	M15	GDC1/IO58UDB1
H8	GND	K12	VCCIB1	M16	IO56NDB1
H9	GND	K13	IO52NPB1	N1	IO103NDB3
H10	GND	K14	IO55RSB1	N2	IO101PPB3
H11	VCC	K15	IO53NPB1	N3	GEC1/IO100PPB3
H12	GCC0/IO48NPB1	K16	IO51NDB1	N4	NC
H13	GCB1/IO49PPB1	L1	IO105NDB3	N5	GNDQ
H14	GCA0/IO50NPB1	L2	IO104NPB3	N6	GEA2/IO97RSB2
H15	NC	L3	NC	N7	IO86RSB2
H16	GCB0/IO49NPB1	L4	IO102RSB3	N8	IO82RSB2
J1	GFA2/IO107PPB3	L5	VCCIB3	N9	IO75RSB2
J2	GFA1/IO108PDB3	L6	GND	N10	IO69RSB2
J3	VCCPLF	L7	VCC	N11	IO64RSB2
J4	IO106NDB3	L8	VCC	N12	GNDQ
J5	GFB2/IO106PDB3	L9	VCC	N13	NC
J6	VCC	L10	VCC	N14	VJTAG
J7	GND	L11	GND	N15	GDC0/IO58VDB1
J8	GND	L12	VCCIB1	N16	GDA1/IO60UDB1
J9	GND	L13	GDB0/IO59VPB1	P1	GEB1/IO99PDB3
J10	GND	L14	IO57VDB1	P2	GEB0/IO99NDB3
J11	VCC	L15	IO57UDB1	P3	NC
J12	GCB2/IO52PPB1	L16	IO56PDB1	P4	NC
J13	GCA1/IO50PPB1	M1	IO103PDB3	P5	IO92RSB2
J14	GCC2/IO53PPB1	M2	NC	P6	IO89RSB2
J15	NC	M3	IO101NPB3	P7	IO85RSB2
J16	GCA2/IO51PDB1	M4	GEC0/IO100NPB3	P8	IO81RSB2

FG256	
Pin Number	A3P1000 Function
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1

FG256	
Pin Number	A3P1000 Function
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3

FG256	
Pin Number	A3P1000 Function
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2