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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	97
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p125-1fg144t

Automotive ProASIC3 Ordering Information

A3P1000 – 1 FG G 144 Y T

- **Part Number**
  - **Automotive ProASIC3 Devices**
    - A3P060 = 60,000 System Gates
    - A3P125 = 125,000 System Gates
    - A3P250 = 250,000 System Gates
    - A3P1000 = 1,000,000 System Gates
- **Speed Grade**
  - Blank = Standard
  - 1 = 15% Faster than Standard
- **Package Type**
  - VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
  - FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
  - QN = Quad Flat Pack (0.5 mm pitch)
- **Lead-Free Packaging**
  - Blank = Standard Packaging
  - G = RoHS-Compliant (Green) Packaging
- **Package Lead Count**
- **Security Feature**
  - Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
  - Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

LICENSED DPA COUNTERMEASURES

- **Application (Temperature Range)**
  - T = Grade 2 and Grade 1 AEC-Q100
    Grade 2 = 105°C T_A and 115°C T_J[1]
    Grade 1 = 125°C T_A and 135°C T_J[1]

Notes:

1. *T_A = Ambient temperature and T_J = Junction temperature.*
2. *Minimum order quantities apply. Contact your local Microsemi SoC Products Group sales office for details.*

Advanced Architecture

The proprietary Automotive ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The Automotive ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM memory
- Extensive CCCs and PLLs
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the Automotive ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

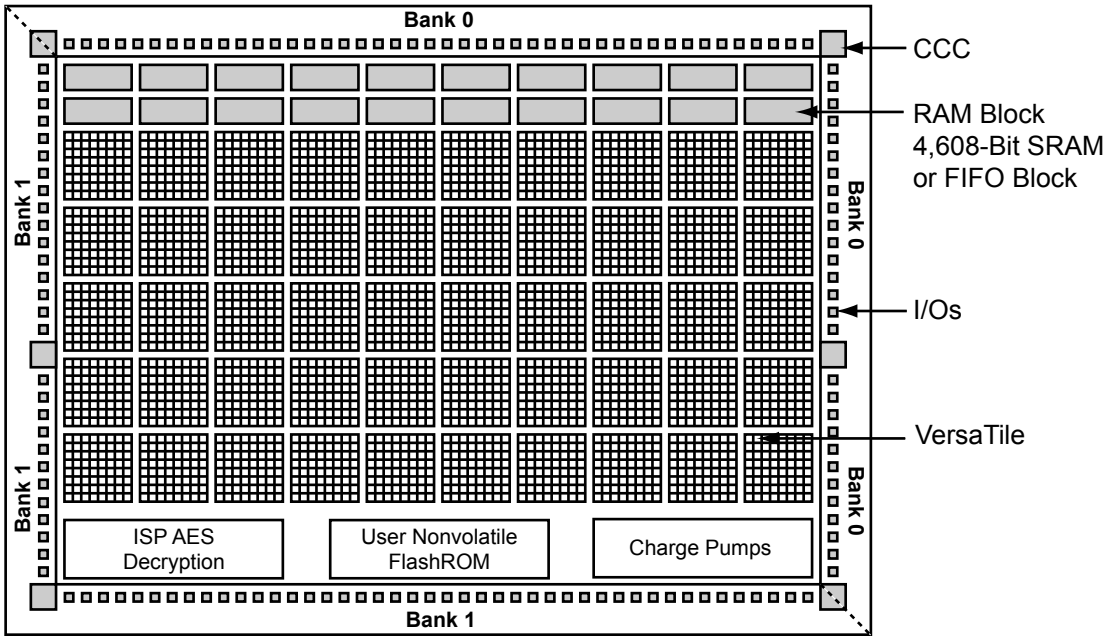


Figure 1-1 • **Automotive ProASIC3 Device Architecture Overview with Two I/O Banks (A3P060 and A3P125)**

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 350 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

Automotive ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The Automotive ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Automotive ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

Automotive ProASIC3 banks for the A3P250 and A3P1000 devices support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-7).

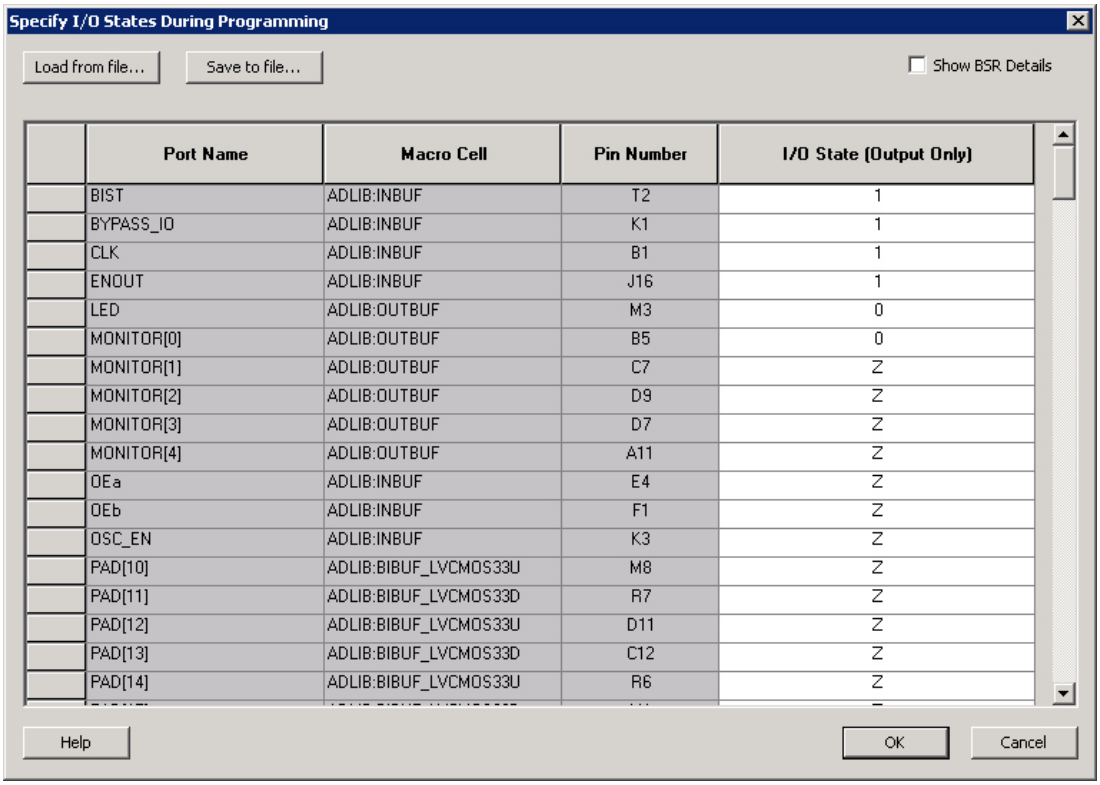
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tristate: I/O is tristated



	Port Name	Macro Cell	Pin Number	I/O State (Output Only)
	BIST	ADLIB:INBUF	T2	1
	BYPASS_IO	ADLIB:INBUF	K1	1
	CLK	ADLIB:INBUF	B1	1
	ENOUT	ADLIB:INBUF	J16	1
	LED	ADLIB:OUTBUF	M3	0
	MONITOR[0]	ADLIB:OUTBUF	B5	0
	MONITOR[1]	ADLIB:OUTBUF	C7	Z
	MONITOR[2]	ADLIB:OUTBUF	D9	Z
	MONITOR[3]	ADLIB:OUTBUF	D7	Z
	MONITOR[4]	ADLIB:OUTBUF	A11	Z
	OEa	ADLIB:INBUF	E4	Z
	OEb	ADLIB:INBUF	F1	Z
	OSC_EN	ADLIB:INBUF	K3	Z
	PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
	PAD[11]	ADLIB:BIBUF_LVCMOS33D	R7	Z
	PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
	PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
	PAD[14]	ADLIB:BIBUF_LVCMOS33U	R6	Z

Figure 1-4 • **I/O States During Programming Window**

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

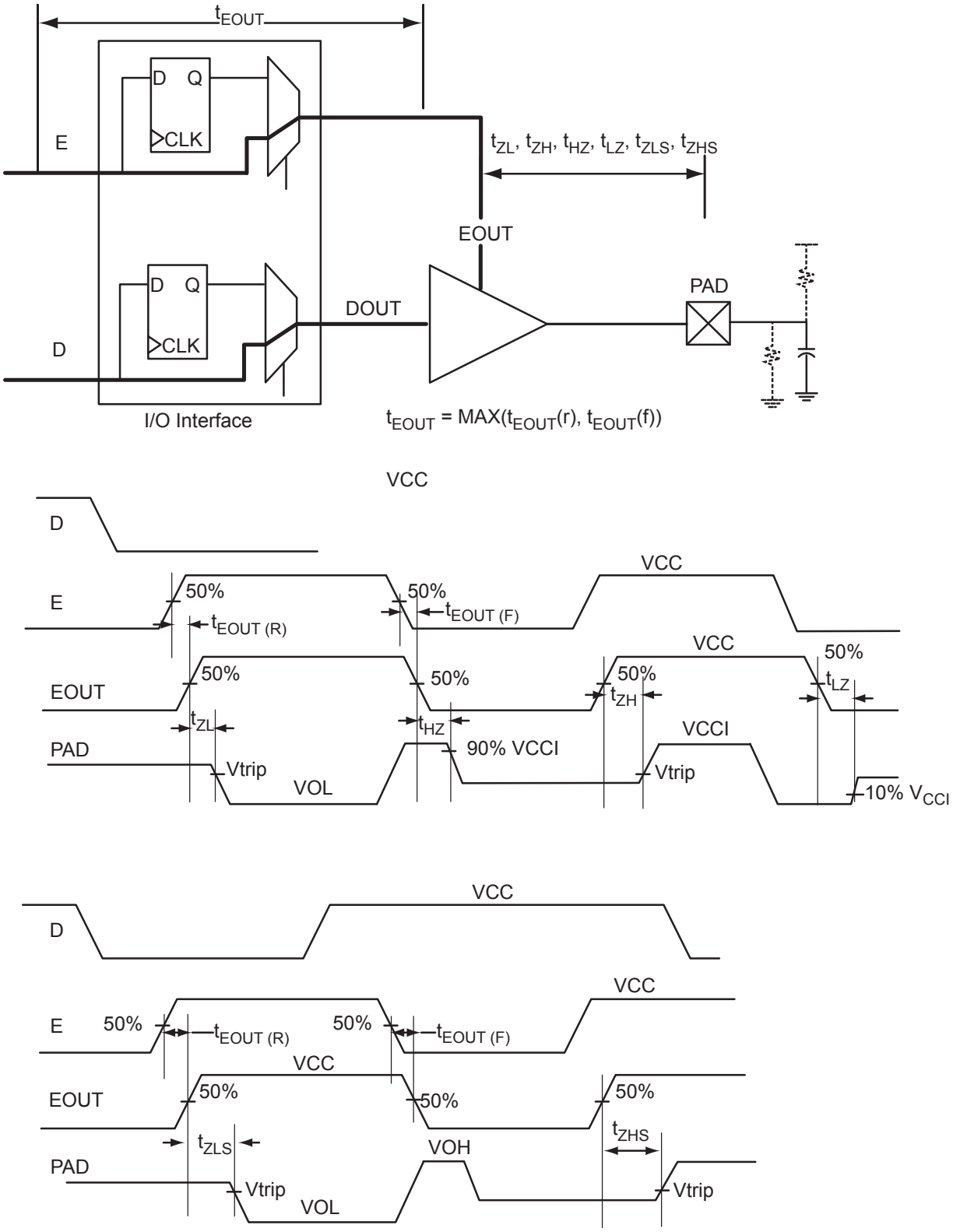


Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Table 2-22 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Automotive-Case Conditions: T_J = 135°C, Worst Case VCC = 1.425 V
Worst Case VCCI = 3.0 V
Advanced I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.80	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.39	0.04	1.23	0.39	3.45	3.27	1.83	1.86	5.58	5.39	ns
1.8 V LVCMOS	12 mA	High	35 pF	–	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.92	ns
1.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.88	0.04	1.37	0.39	2.25	1.98	3.75	4.00	3.46	3.21	ns
3.3 V PCI	Per PCI spec	High	10 pF	25 [2]	0.55	2.19	0.04	0.81	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25 [2]	0.55	2.55	0.04	0.79	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns
LVDS	24 mA	High	–	–	0.55	1.74	0.04	1.52	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.55	1.71	0.04	1.34	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-48 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 2-24 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-25 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to Advanced I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	6 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / I_{OLspec}*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / I_{OHspec}*

Table 2-31 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.*

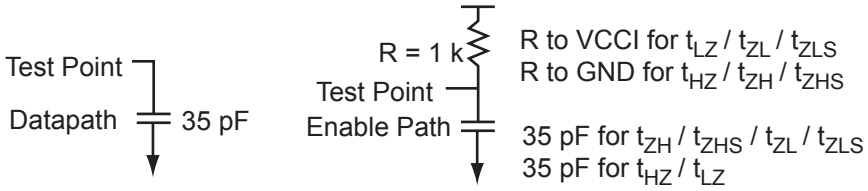


Figure 2-7 • **AC Loading**

Table 2-34 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	35

*Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.*

Timing Characteristics

Table 2-35 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	8.56	0.05	1.14	0.46	8.72	7.37	1.46	1.42	11.22	9.866	ns
	-1	0.55	7.28	0.04	0.97	0.39	7.42	6.27	1.46	1.42	9.54	8.393	ns
6 mA	STD	0.64	5.49	0.05	1.14	0.46	5.59	4.55	1.65	1.74	8.09	7.05	ns
	-1	0.55	4.67	0.04	0.97	0.39	4.75	3.87	1.65	1.74	6.88	5.997	ns
8 mA	STD	0.64	5.49	0.05	1.14	0.46	5.59	4.55	1.65	1.74	8.09	7.05	ns
	-1	0.55	4.67	0.04	0.97	0.39	4.75	3.87	1.65	1.74	6.88	5.997	ns
12 mA	STD	0.64	3.95	0.05	1.14	0.46	4.02	1.56	3.59	1.94	6.52	2.795	ns
	-1	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.797	ns
16 mA	STD	0.64	3.73	0.05	1.14	0.46	1.84	1.42	3.65	4.11	3.05	2.651	ns
	-1	0.55	3.17	0.04	0.97	0.39	1.84	1.42	3.10	3.50	3.05	2.653	ns
24 mA	STD	0.64	3.44	0.05	1.14	0.46	1.70	1.17	3.72	4.54	2.91	2.405	ns
	-1	0.55	2.92	0.04	0.97	0.39	1.70	1.17	3.16	3.86	2.91	2.407	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	11.47	0.05	1.14	0.46	11.68	9.95	1.46	1.33	14.18	12.449	ns
	-1	0.55	9.75	0.04	0.97	0.39	9.94	8.46	1.46	1.33	12.06	10.59	ns
6 mA	STD	0.64	8.13	0.05	1.14	0.46	8.28	7.03	1.65	1.65	10.79	9.526	ns
	-1	0.55	6.92	0.04	0.97	0.39	7.05	5.98	1.65	1.65	9.17	8.103	ns
8 mA	STD	0.64	8.13	0.05	1.14	0.46	8.28	7.03	1.65	1.65	10.79	9.526	ns
	-1	0.55	6.92	0.04	0.97	0.39	7.05	5.98	1.65	1.65	9.17	8.103	ns
12 mA	STD	0.64	6.24	0.05	1.14	0.46	6.36	5.45	1.77	1.85	8.86	7.946	ns
	-1	0.55	5.31	0.04	0.97	0.39	5.41	4.63	1.77	1.85	7.53	6.76	ns
16 mA	STD	0.64	5.82	0.05	1.14	0.46	5.93	5.10	1.80	1.90	8.43	7.604	ns
	-1	0.55	4.95	0.04	0.97	0.39	5.04	4.34	1.80	1.90	7.17	6.468	ns
24 mA	STD	0.64	5.42	0.05	1.14	0.46	5.52	5.08	1.83	2.10	8.02	7.581	ns
	-1	0.55	4.61	0.04	0.97	0.39	4.70	4.32	1.83	2.11	6.82	6.449	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	8.06	0.05	1.12	0.46	8.20	7.03	1.26	1.27	8.20	7.027	ns
	-1	0.55	6.85	0.04	.095	0.39	6.98	5.98	1.26	1.27	6.98	5.978	ns
6 mA	STD	0.64	5.03	0.05	1.12	0.46	5.13	4.27	1.42	1.56	5.13	4.267	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
8 mA	STD	0.64	5.03	0.05	1.12	0.46	5.13	4.27	1.42	1.56	5.13	4.267	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
12 mA	STD	0.64	3.53	0.05	1.12	0.46	1.74	1.43	3.12	3.60	1.74	1.427	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.428	ns
16 mA	STD	0.64	3.53	0.05	1.12	0.46	1.74	1.43	3.12	3.60	1.74	1.427	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.428	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	10.82	0.05	1.12	0.46	11.02	9.42	1.26	1.20	11.02	9.419	ns
	-1	0.55	9.21	0.04	0.95	0.39	9.38	8.01	1.26	1.20	9.38	8.012	ns
6 mA	STD	0.64	7.49	0.05	1.12	0.46	7.63	6.58	1.43	1.48	7.63	6.58	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.598	ns
8 mA	STD	0.64	7.49	0.05	1.12	0.46	7.63	6.58	1.43	1.48	7.63	6.58	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.598	ns
12 mA	STD	0.64	5.64	0.05	1.12	0.46	5.75	5.04	1.54	1.67	5.75	5.042	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.289	ns
16 mA	STD	0.64	5.64	0.05	1.12	0.46	5.75	5.04	1.54	1.67	5.75	5.042	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.289	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-41 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	7.79	0.05	1.08	0.45	7.94	6.80	1.22	1.23	7.94	6.80	ns
	-1	0.55	6.85	0.04	0.95	0.39	6.98	5.98	1.26	1.27	6.98	5.98	ns
6 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
8 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
12 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns
16 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-42 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	10.47	0.05	1.08	0.45	10.66	9.11	1.22	1.16	10.66	9.11	ns
	-1	0.55	9.21	0.04	0.95	0.39	9.38	8.01	1.26	1.20	9.38	8.01	ns
6 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
8 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
12 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns
16 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

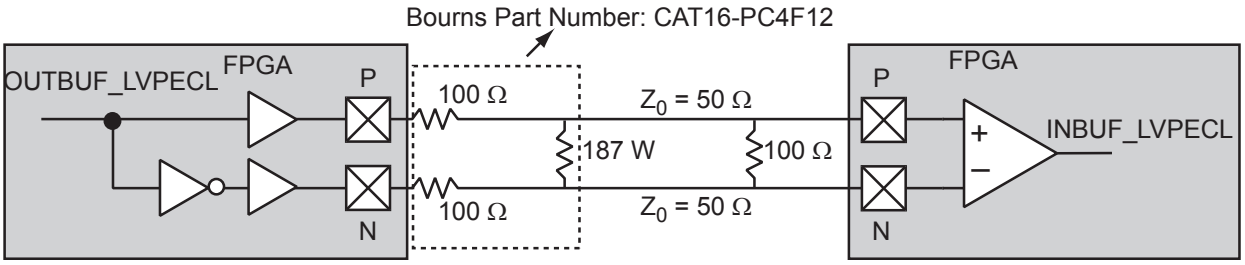


Figure 2-14 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-86 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-87 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

*Note: *Measuring point = Vtrip. See Table 2-18 on page 2-17 for a complete table of trip points.*

Timing Characteristics

Table 2-88 • **LVPECL**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.64	2.01	0.05	1.57	ns
–1	0.55	1.71	0.04	1.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-89 • **LVPECL**
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.63	1.95	0.05	1.52	ns
–1	0.53	1.66	0.04	1.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-90 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

*Note: *See Figure 2-15 on page 2-53 for more information.*

Table 2-97 • Output Enable Register Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.53	0.62	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.37	0.44	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.52	0.61	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.79	0.93	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.79	0.93	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.31	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.31	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Timing Characteristics

Table 2-104 • Combinatorial Cell Propagation Delays
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.49	0.57	ns
AND2	Y = A · B	t_{PD}	0.57	0.67	ns
NAND2	Y = !(A · B)	t_{PD}	0.57	0.67	ns
OR2	Y = A + B	t_{PD}	0.59	0.69	ns
NOR2	Y = !(A + B)	t_{PD}	0.59	0.69	ns
XOR2	Y = A ⊕ B	t_{PD}	0.90	1.05	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.85	1.00	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.06	1.25	ns
MUX2	Y = A !S + B S	t_{PD}	0.62	0.72	ns
AND3	Y = A · B · C	t_{PD}	0.68	0.80	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-105 • Combinatorial Cell Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.48	0.56	ns
AND2	Y = A · B	t_{PD}	0.56	0.66	ns
NAND2	Y = !(A · B)	t_{PD}	0.56	0.66	ns
OR2	Y = A + B	t_{PD}	0.58	0.68	ns
NOR2	Y = !(A + B)	t_{PD}	0.58	0.68	ns
XOR2	Y = A ⊕ B	t_{PD}	0.88	1.03	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.83	0.98	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.04	1.23	ns
MUX2	Y = A !S + B S	t_{PD}	0.60	0.71	ns
AND3	Y = A · B · C	t_{PD}	0.67	0.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-107 • Register Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.66	0.77	ns
t_{SUD}	Data Setup Time for the Core Register	0.51	0.60	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.54	0.64	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.48	0.56	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.48	0.56	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.27	0.31	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.27	0.31	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.41	0.48	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-110 • A3P125 Global Resource
Commercial-Case Conditions: T_J = 135°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.93	1.22	1.09	1.43	ns
t_{RCKH}	Input High Delay for Global Clock	0.92	1.26	1.08	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35		0.41	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-111 • A3P125 Global Resource
Commercial-Case Conditions: T_J = 115°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.90	1.19	1.06	1.40	ns
t_{RCKH}	Input High Delay for Global Clock	0.90	1.23	1.05	1.45	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.34		0.40	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

JTAG Pins

Automotive ProASIC3 devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Actel recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-1 for more information.

***Table 3-1* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-1 and must satisfy the parallel resistance value requirement. The values in Table 3-1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Actel recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Revision	Changes	Page
Revision 2 (continued)	The "Pin Descriptions and Packaging" chapter has been added (SAR 34767),	3-1
	The "VQ100" pin table for A3P125 has been added (SAR 37944).	4-3
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34767).	4-1
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Automotive ProASIC3 Device Status" table on page II indicates the status for each device in the device family.	N/A

Revision	Changes	Page
Revision 1 (Dec 2009) Product Brief v1.1	The QNG132 package was added to the "Automotive ProASIC3 Product Family" table, "I/Os Per Package" table, "Automotive ProASIC3 Ordering Information", and "Temperature Grade Offerings".	I – IV
Packaging v1.1	Pin tables for A3P125 and A3P250 were added for the "QN132" package.	4-6