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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	97
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p125-1fgg144t

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Automotive ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

The Microsemi flash-based Automotive ProASIC3 devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based Automotive ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and external clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the Automotive ProASIC3 device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based Automotive ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of Automotive ProASIC3 flash-based FPGAs. Once it is programmed, the flash cell configuration element of Automotive ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Automotive ProASIC3 devices exhibit very low power characteristics, similar to those of an ASIC, making them an ideal choice for power-sensitive applications. Automotive ProASIC3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

Automotive ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The Automotive ProASIC3 family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVC MOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

I/O Output Buffer Contribution— P_{OUTPUTS}

$$P_{\text{OUTPUTS}} = N_{\text{OUTPUTS}} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{\text{CLK}}$$

N_{OUTPUTS} is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-13 on page 2-12.

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{\text{MEMORY}} = PAC11 * N_{\text{BLOCKS}} * F_{\text{READ-CLOCK}} * \beta_2 + PAC12 * N_{\text{BLOCK}} * F_{\text{WRITE-CLOCK}} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{\text{READ-CLOCK}}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{\text{WRITE-CLOCK}}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-13 on page 2-12.

PLL Contribution— P_{PLL}

$$P_{\text{PLL}} = PAC13 + PAC14 * F_{\text{CLKOUT}}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-12 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($PAC14 * F_{\text{CLKOUT}}$ product) to the total PLL contribution.

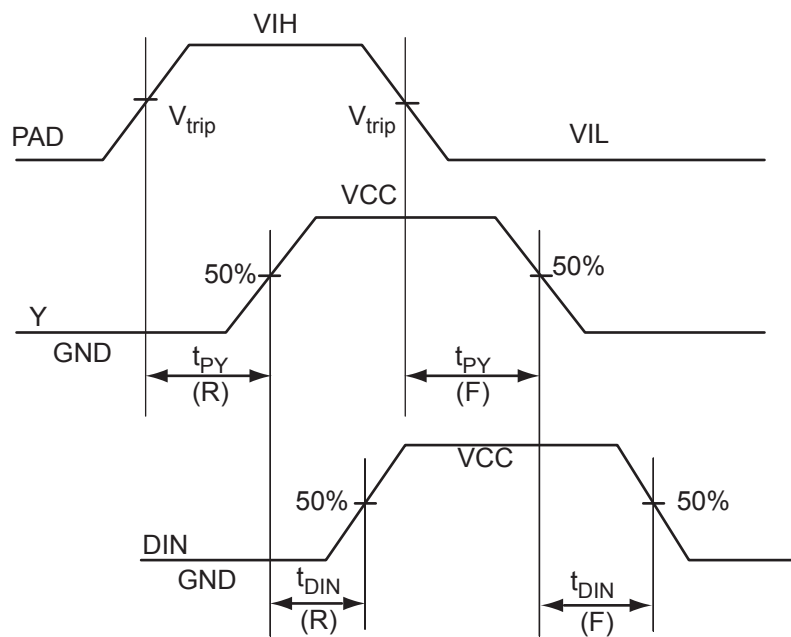
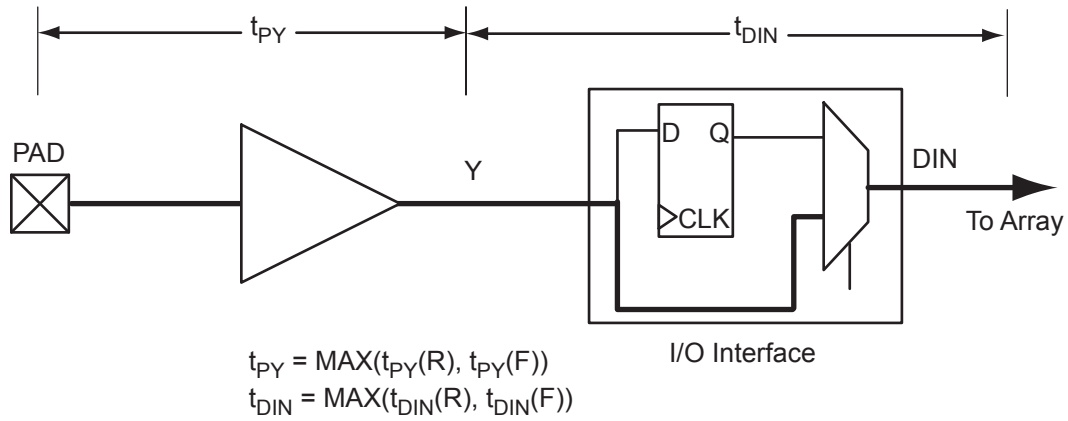


Figure 2-4 • Input Buffer Timing Model and Delays (example)

Table 2-16 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Standard I/O Banks

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	High	−0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	−0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4
1.5 V LVCMOS	2 mA	High	−0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2

Note: Currents are measured at 125°C junction temperature.

Table 2-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Automotive Grade 1 and Grade 2

DC I/O Standards	Automotive Grade 1 ¹		Automotive Grade 2 ²	
	IIL	IIH	IIL	IIH
	μA	μA	μA	μA
3.3 V LVTTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. Automotive range Grade 1 (−40°C < T_J < 135°C)
2. Automotive range Grade 2 (−40°C < T_J < 115°C)

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-18 • Summary of AC Measuring Points

Standard	Measuring Trip Point (Vtrip)
3.3 V LVTTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * VCCI (RR)
	0.615 * VCCI (FF)
3.3 V PCI-X	0.285 * VCCI (RR)
	0.615 * VCCI (FF)

Table 2-23 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$
Worst Case $V_{CCI} = 3.0\text{ V}$
Standard Plus I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{BOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.80	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.11	ns
1.8 V LVCMOS	8 mA	High	35 pF	–	0.55	3.73	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.99	ns
1.5 V LVCMOS	4 mA	High	35 pF	–	0.55	4.60	0.04	1.35	0.39	4.61	5.05	2.07	1.85	6.74	7.18	ns
3.3 V PCI	Per PCI spec	High	10 pF	25^2	0.55	2.55	0.04	0.82	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25^2	0.55	2.55	0.04	0.79	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns

Notes:

1. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-48](#) for connectivity. This resistor is not required during normal operation.

Table 2-29 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to Standard Plus I/O Banks

	Drive Strength	I _{OSL} (mA)*	I _{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
2.5 V LVCMOS	2 mA	18	16
	6 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: *T_J = 100°C

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-30 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months
125°C	25 days
135°	12 days

Table 2-48 • 2.5 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.26	0.05	1.45	0.46	8.28	9.26	1.24	1.12	10.78	11.756	ns
	-1	0.55	7.87	0.04	1.23	0.39	7.05	7.87	1.24	1.13	9.17	10	ns
6 mA	STD	0.64	5.43	0.05	1.45	0.46	5.19	5.43	1.43	1.47	7.69	7.926	ns
	-1	0.55	4.62	0.04	1.23	0.39	4.42	4.62	1.43	1.47	6.55	6.743	ns
12 mA	STD	0.64	3.59	0.05	1.45	0.46	3.65	3.51	1.56	1.69	6.15	6.012	ns
	-1	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.114	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-49 • 2.5 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	12.12	0.05	1.45	0.46	11.89	12.12	1.25	1.08	14.39	14.622	ns
	-1	0.55	10.31	0.04	1.23	0.39	10.12	10.31	1.25	1.08	12.24	12.438	ns
6 mA	STD	0.64	8.24	0.05	1.45	0.46	8.39	8.23	1.43	1.42	10.89	10.73	ns
	-1	0.55	7.01	0.04	1.23	0.39	7.14	7.00	1.43	1.42	9.26	9.128	ns
12 mA	STD	0.64	6.30	0.05	1.45	0.46	6.41	6.16	1.56	1.63	8.91	8.656	ns
	-1	0.55	5.35	0.04	1.23	0.39	5.45	5.24	1.56	1.63	7.58	7.364	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-58 • 1.8 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	17.36	0.05	1.45	0.46	15.78	17.36	1.53	0.87	18.28	19.864	ns
	-1	0.55	14.77	0.04	1.23	0.39	13.42	14.77	1.54	0.87	15.55	16.897	ns
4 mA	STD	0.64	11.71	0.05	1.45	0.46	11.64	11.71	1.78	1.48	14.14	14.214	ns
	-1	0.55	9.96	0.04	1.23	0.39	9.90	9.96	1.78	1.48	12.03	12.091	ns
6 mA	STD	0.64	9.00	0.05	1.45	0.46	9.17	8.77	1.95	1.77	11.67	11.267	ns
	-1	0.55	7.66	0.04	1.23	0.39	7.80	7.46	1.95	1.77	9.92	9.585	ns
8 mA	STD	0.64	8.39	0.05	1.45	0.46	8.54	8.16	1.99	1.85	11.04	10.66	ns
	-1	0.55	7.14	0.04	1.23	0.39	7.27	6.94	1.99	1.85	9.40	9.068	ns
12 mA	STD	0.64	8.15	0.05	1.45	0.46	8.09	8.15	2.05	2.14	10.59	10.654	ns
	-1	0.55	6.94	0.04	1.23	0.39	6.88	6.94	2.05	2.14	9.01	9.063	ns
16 mA	STD	0.64	8.15	0.05	1.45	0.46	8.09	8.15	2.05	2.14	10.59	10.654	ns
	-1	0.55	6.94	0.04	1.23	0.39	6.88	6.94	2.05	2.14	9.01	9.063	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-59 • 1.8 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.26	0.05	1.36	0.46	9.75	12.67	1.24	0.82	12.26	15.17	ns
	-1	0.55	11.28	0.04	1.16	0.39	8.30	10.78	1.24	0.83	10.43	12.905	ns
4 mA	STD	0.64	7.73	0.05	1.36	0.46	6.13	7.25	1.46	1.41	8.63	9.749	ns
	-1	0.55	6.58	0.04	1.16	0.39	5.21	6.17	1.46	1.41	7.34	8.293	ns
6 mA	STD	0.64	4.97	0.05	1.36	0.46	4.29	4.54	1.62	1.68	6.79	7.039	ns
	-1	0.55	4.23	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.987	ns
8 mA	STD	0.64	4.39	0.05	1.36	0.46	4.29	4.54	1.62	1.68	6.79	7.039	ns
	-1	0.55	3.73	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.987	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-80 • 3.3 V PCI/PCI-X

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.628	2.50	0.05	0.92	0.45	1.23	0.91	3.02	3.48	2.40	2.11	ns
–1	0.53	2.12	0.04	0.78	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-81 • 3.3 V PCI/PCI-X

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.628	2.90	0.05	0.90	0.45	1.23	0.91	3.02	3.48	2.40	2.11	ns
–1	0.53	2.47	0.04	0.77	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-12 on page 2-50](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

Table 2-103 • Output DDR Propagation Delays
Commercial-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.84	0.98	ns
t_{DDROSUD1}	Data_F Data Setup for Output DDR	0.45	0.53	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.45	0.53	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	0.96	1.12	ns
$t_{\text{DDROREMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{\text{DDRORECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.27	0.31	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.25	0.30	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width High for the Output DDR	0.41	0.48	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width Low for the Output DDR	0.37	0.43	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Embedded SRAM and FIFO Characteristics

SRAM

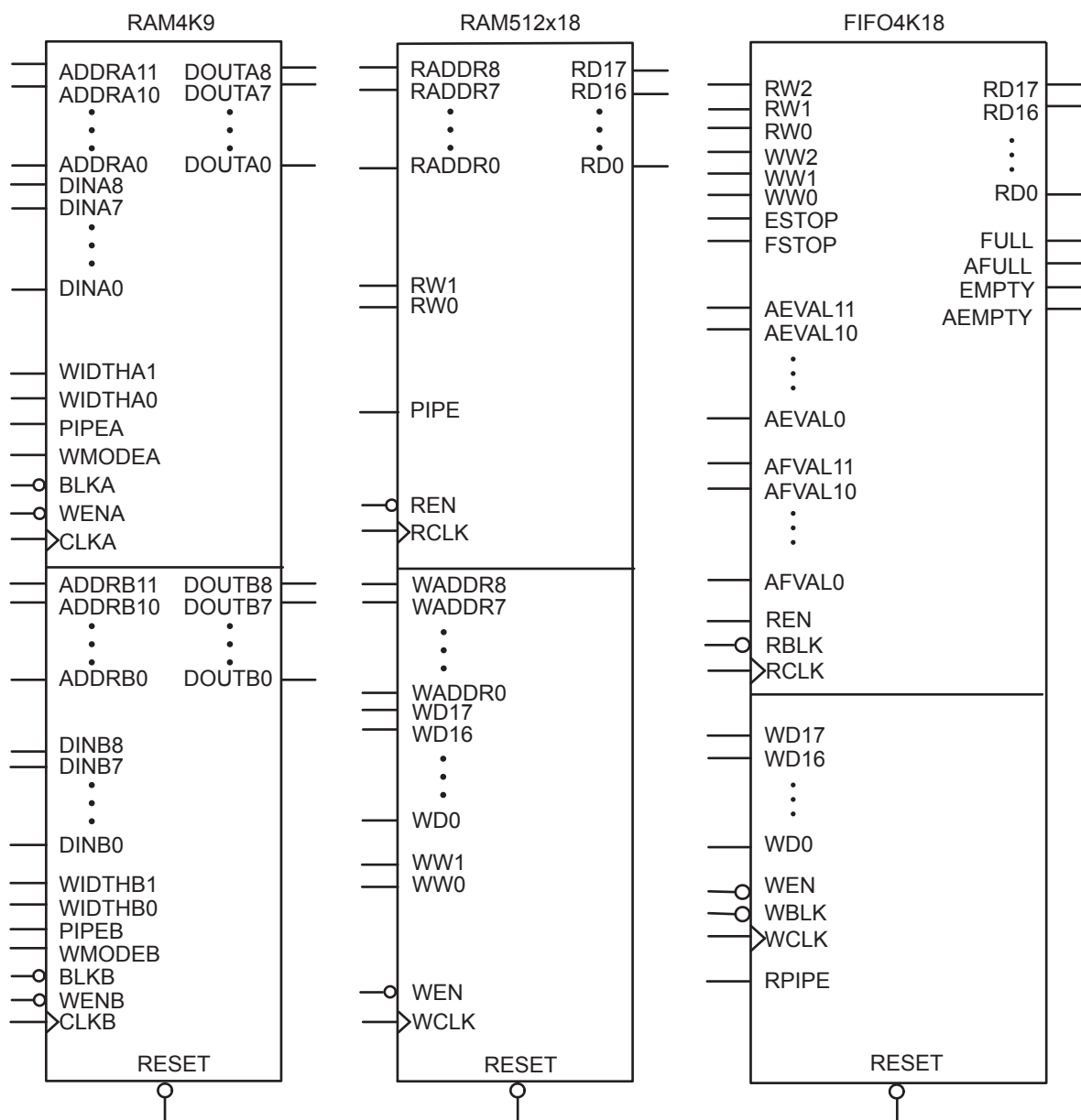


Figure 2-30 • RAM Models

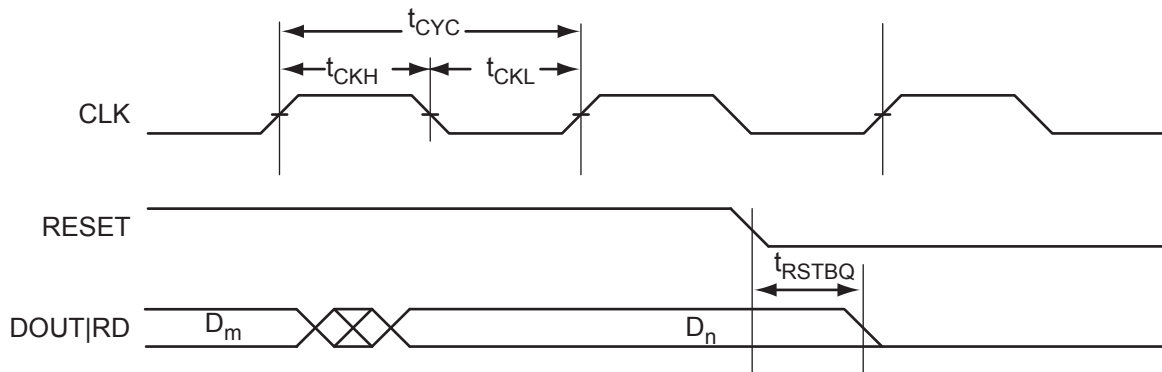


Figure 2-35 • RAM Reset. Applicable to Both RAM4K9 and RAM512x18

Timing Waveforms

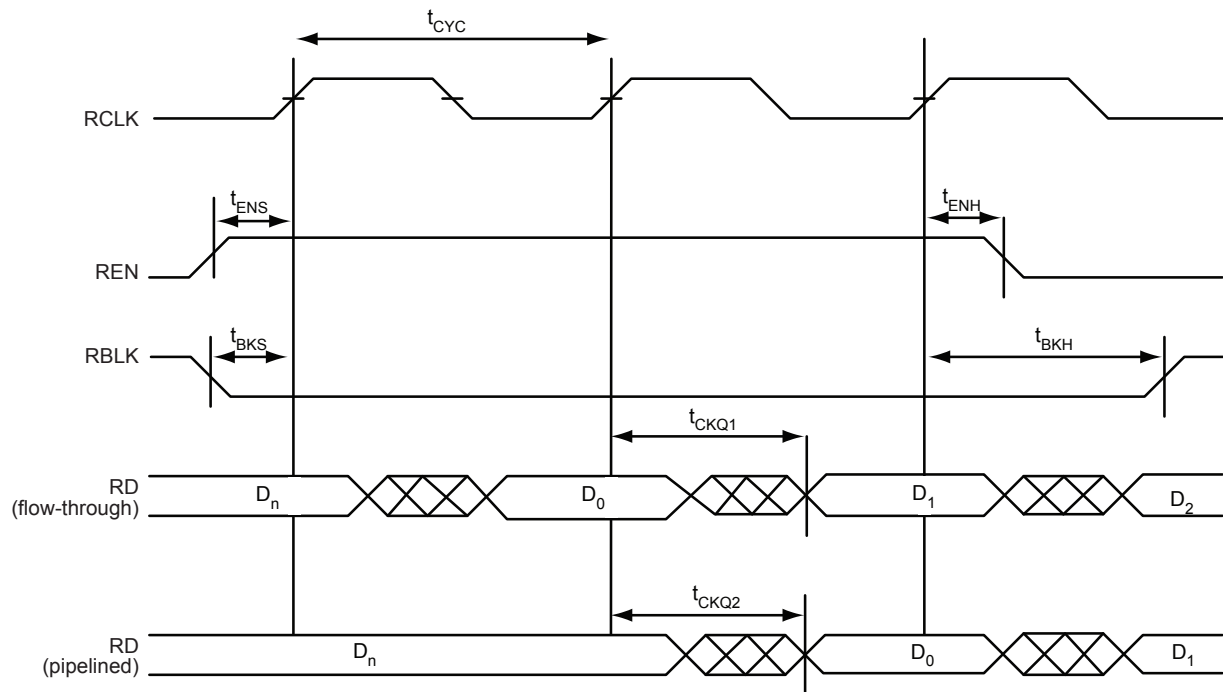


Figure 2-37 • FIFO Read

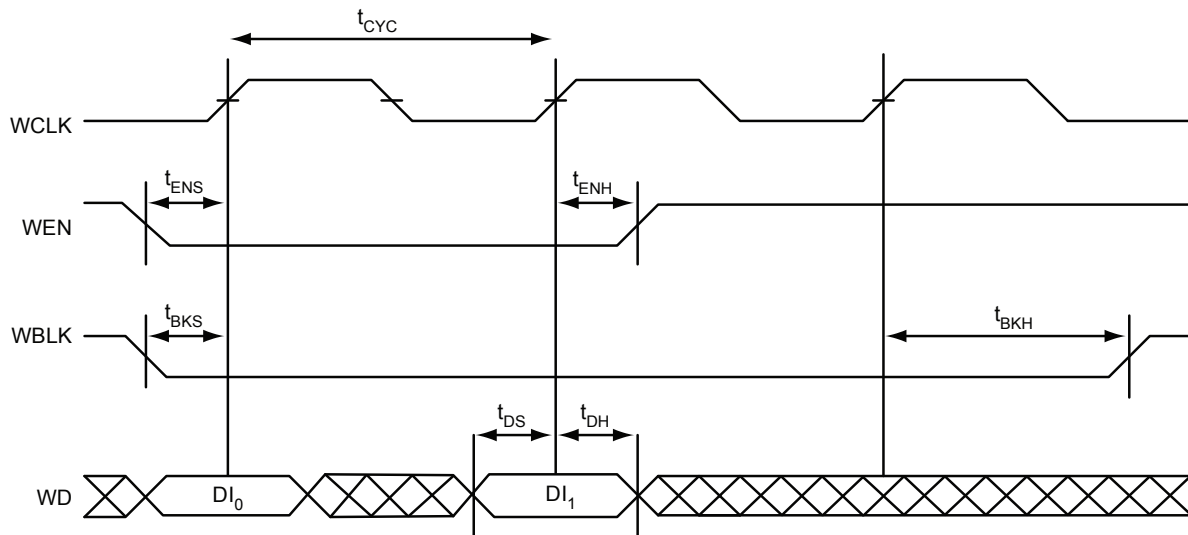


Figure 2-38 • FIFO Write

Embedded FlashROM Characteristics

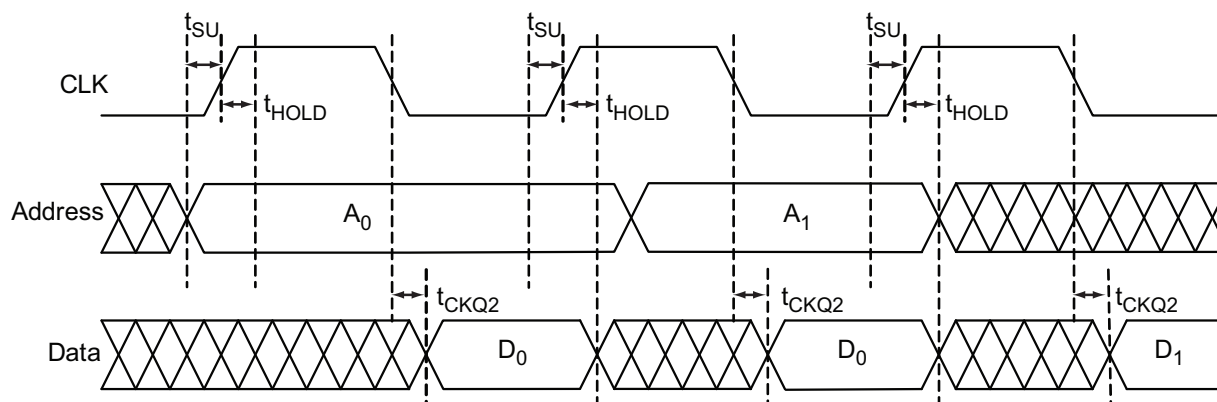


Figure 2-44 • Timing Diagram

Timing Characteristics

Table 2-123 • Embedded FlashROM Access Time

Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t _{SU}	Address Setup Time	0.65	0.76	ns
t _{HOLD}	Address Hold Time	0.00	0.00	ns
t _{CK2Q}	Clock to Out	19.73	23.20	ns
F _{MAX}	Maximum Clock Frequency	15	15	MHz

Table 2-124 • Embedded FlashROM Access Time

Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t _{SU}	Address Setup Time	0.64	0.75	ns
t _{HOLD}	Address Hold Time	0.00	0.00	ns
t _{CK2Q}	Clock to Out	19.35	22.74	ns
F _{MAX}	Maximum Clock Frequency	15	15	MHz

Special Function Pins

NC

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

No Connect

DC

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Do Not Connect

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Actel offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

User's Guides

Automotive ProASIC FPGA Fabric User's Guide

http://www.microsemi.com/soc/documents/PA3_Auto_UG.pdf

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

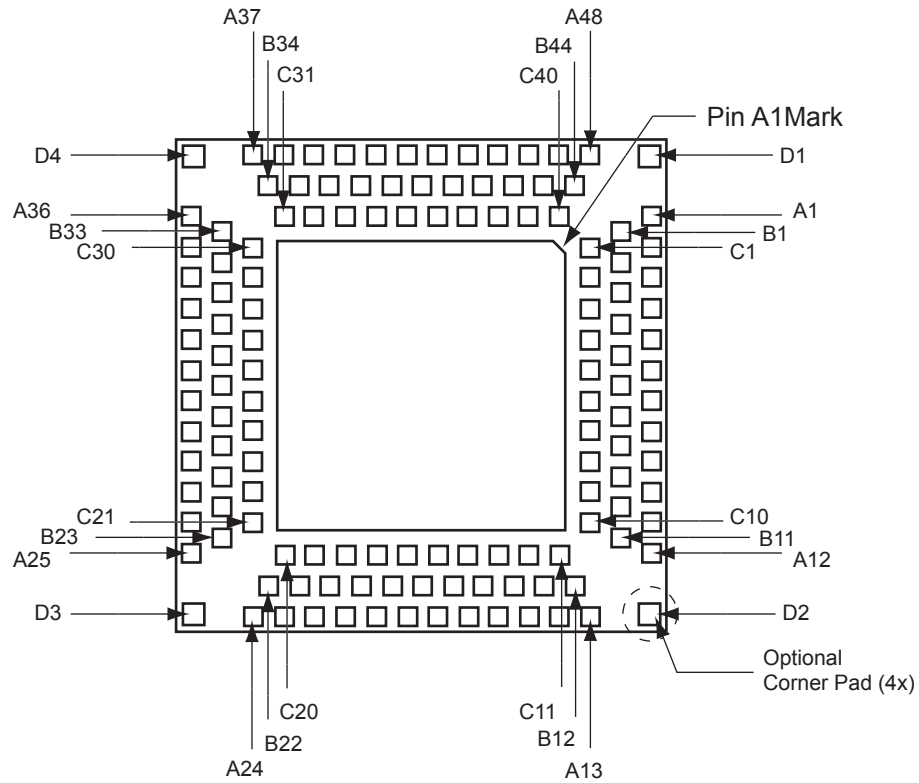
Package Mechanical Drawings

<http://www.microsemi.com/soc/documents/PckgMechDrwns.pdf>

This document contains the package mechanical drawings for all packages currently or previously supplied by Actel. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials: <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

QN132



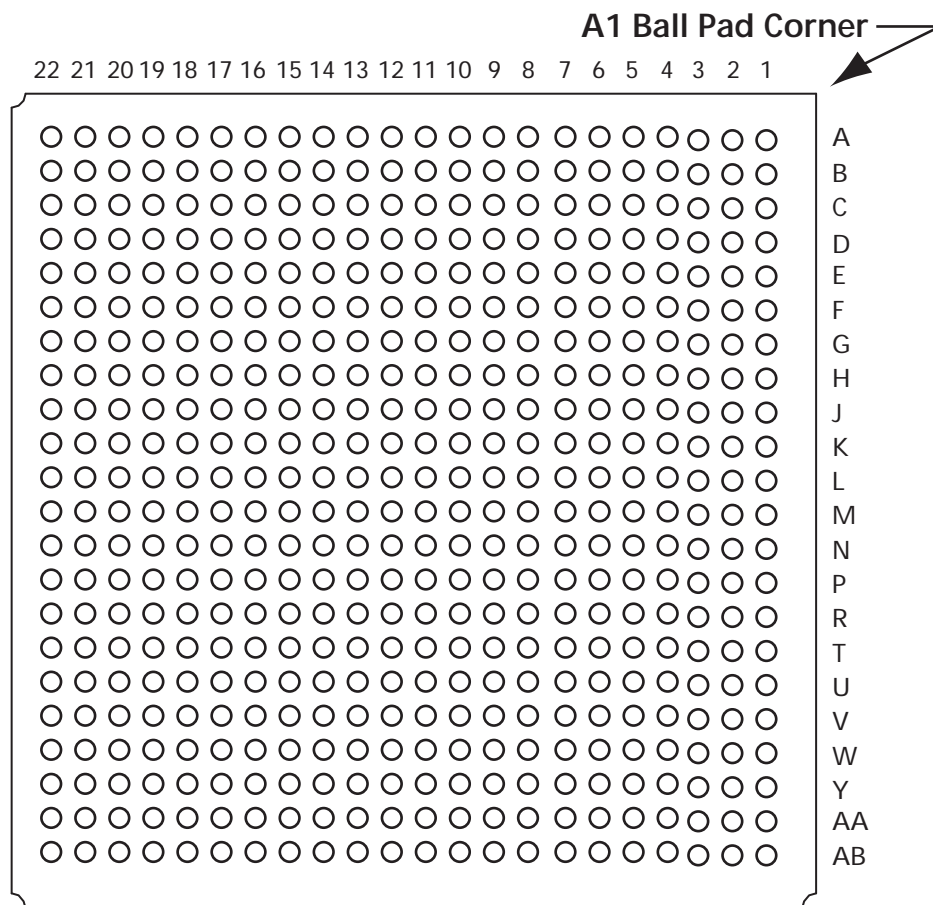
Notes:

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

FG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

FG484		FG484		FG484	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
K19	IO88NDB1	M11	GND	P3	IO199NDB3
K20	IO94NPB1	M12	GND	P4	IO202NDB3
K21	IO98NDB1	M13	GND	P5	IO202PDB3
K22	IO98PDB1	M14	VCC	P6	IO196PPB3
L1	NC	M15	GCB2/IO95PPB1	P7	IO193PPB3
L2	IO200PDB3	M16	GCA1/IO93PPB1	P8	VCCIB3
L3	IO210NPB3	M17	GCC2/IO96PPB1	P9	GND
L4	GFB0/IO208NPB3	M18	IO100PPB1	P10	VCC
L5	GFA0/IO207NDB3	M19	GCA2/IO94PPB1	P11	VCC
L6	GFB1/IO208PPB3	M20	IO101PPB1	P12	VCC
L7	VCOMPLF	M21	IO99PPB1	P13	VCC
L8	GFC0/IO209NPB3	M22	NC	P14	GND
L9	VCC	N1	IO201NDB3	P15	VCCIB1
L10	GND	N2	IO201PDB3	P16	GDB0/IO112NPB1
L11	GND	N3	NC	P17	IO106NDB1
L12	GND	N4	GFC2/IO204PDB3	P18	IO106PDB1
L13	GND	N5	IO204NDB3	P19	IO107PDB1
L14	VCC	N6	IO203NDB3	P20	NC
L15	GCC0/IO91NPB1	N7	IO203PDB3	P21	IO104PDB1
L16	GCB1/IO92PPB1	N8	VCCIB3	P22	IO103NDB1
L17	GCA0/IO93NPB1	N9	VCC	R1	NC
L18	IO96NPB1	N10	GND	R2	IO197PPB3
L19	GCB0/IO92NPB1	N11	GND	R3	VCC
L20	IO97PDB1	N12	GND	R4	IO197NPB3
L21	IO97NDB1	N13	GND	R5	IO196NPB3
L22	IO99NPB1	N14	VCC	R6	IO193NPB3
M1	NC	N15	VCCIB1	R7	GEC0/IO190NPB3
M2	IO200NDB3	N16	IO95NPB1	R8	VMV3
M3	IO206NDB3	N17	IO100NPB1	R9	VCCIB2
M4	GFA2/IO206PDB3	N18	IO102NDB1	R10	VCCIB2
M5	GFA1/IO207PDB3	N19	IO102PDB1	R11	IO147RSB2
M6	VCCPLF	N20	NC	R12	IO136RSB2
M7	IO205NDB3	N21	IO101NPB1	R13	VCCIB2
M8	GFB2/IO205PDB3	N22	IO103PDB1	R14	VCCIB2
M9	VCC	P1	NC	R15	VMV2
M10	GND	P2	IO199PDB3	R16	IO110NDB1

