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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	84
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	132-WFQFN
Supplier Device Package	132-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a3p125-1qng132t

Temperature Grade Offerings

Package	A3P060	A3P125	A3P250	A3P1000
VQ100	C, I, T	C, I, T	C, I, T	–
FG144	C, I, T	C, I, T	C, I, T	C, I, T
FG256	–	–	C, I, T	C, I, T
FG484	–	–	–	C, I, T
QNG132	–	C, I, T	C, I, T	–

Notes:
1. *C = Commercial temperature range: 0°C to 70°C*
2. *I = Industrial temperature range: –40°C to 85°C*
3. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
4. *Specifications for Commercial and Industrial grade devices can be found in the ProASIC3 Flash Family FPGAs datasheet.*

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
T (Grade 1 and Grade 2), Commercial, Industrial	3	3

Notes:
1. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
2. *Specifications for Commercial and Industrial grade devices can be found in the ProASIC3 Flash Family FPGAs datasheet.*

Contact your local Microsemi SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

User Nonvolatile FlashROM

Automotive ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Unique protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, infotainment systems)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard Automotive ProASIC3 IEEE 1532 JTAG programming interface.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

Automotive ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM

Automotive ProASIC3 devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

PLL and CCC

Automotive ProASIC3 devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the Automotive ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

2 – Automotive ProASIC3 DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximums are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V_{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+150	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-3 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Figure 2-1 on page 2-2. For recommended operating limits, refer to Table 2-2 on page 2-2.*

Table 2-19 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t_{DP}	Data-to-Pad delay through the Output Buffer
t_{PY}	Pad-to-Data delay through the Input Buffer
t_{DOUT}	Data–to–Output Buffer delay through the I/O interface
t_{EOUT}	Enable–to–Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer–to–Data delay through the I/O interface
t_{HZ}	Enable-to-Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable-to-Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable-to-Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable-to-Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable-to-Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable-to-Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-20 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Automotive-Case Conditions: T_J = 115°C, Worst Case VCC = 1.425 V
Worst Case VCCI = 3.0 V
Advanced I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.53	3.25	0.04	0.94	0.38	3.31	1.51	2.96	1.88	5.37	2.71	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.53	3.28	0.04	1.19	0.38	3.34	3.16	1.77	1.80	5.39	5.22	ns
1.8 V LVCMOS	12 mA	High	35 pF	–	0.53	3.25	0.04	1.12	0.38	1.89	1.63	3.41	3.75	3.06	2.82	ns
1.5 V LVCMOS	12 mA	High	35 pF	–	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns
3.3 V PCI	Per PCI spec	High	10 pF	25 [2]	0.53	2.12	0.04	0.78	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25 [2]	0.53	2.47	0.04	0.77	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns
LVDS	24 mA	High	–	–	0.53	1.68	0.04	1.47	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.53	1.66	0.04	1.29	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-48 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 2-24 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-25 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to Advanced I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	6 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / I_{OLspec}*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / I_{OHspec}*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-43 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		V_{OL}	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-44 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	VIL		VIH		V_{OL}	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

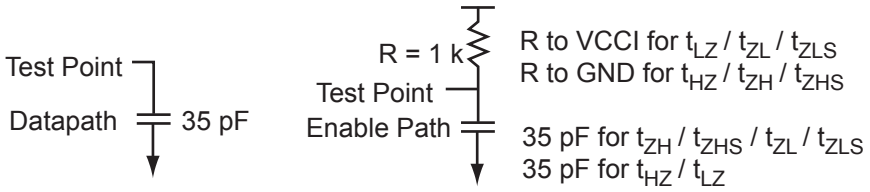


Figure 2-8 • AC Loading

Table 2-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	35

*Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.*

Timing Characteristics

Table 2-57 • 1.8 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.26	0.05	1.36	0.46	10.22	13.26	1.53	0.90	12.72	15.764	ns
	-1	0.55	11.28	0.04	1.16	0.39	8.69	11.28	1.53	0.90	10.82	13.41	ns
4 mA	STD	0.64	7.73	0.05	1.36	0.46	6.55	7.73	1.78	1.54	9.05	10.232	ns
	-1	0.55	6.58	0.04	1.16	0.39	5.58	6.58	1.78	1.54	7.70	8.704	ns
6 mA	STD	0.64	4.97	0.05	1.36	0.46	4.67	4.97	1.95	1.83	7.17	7.472	ns
	-1	0.55	4.23	0.04	1.16	0.39	3.98	4.23	1.95	1.83	6.10	6.356	ns
8 mA	STD	0.64	4.39	0.05	1.36	0.46	4.39	4.39	1.99	1.91	6.89	6.888	ns
	-1	0.55	3.73	0.04	1.16	0.39	3.74	3.73	1.99	1.91	5.86	5.859	ns
12 mA	STD	0.64	3.95	0.05	1.36	0.46	1.95	1.68	4.14	4.56	3.16	2.915	ns
	-1	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.918	ns
16 mA	STD	0.64	3.95	0.05	1.36	0.46	1.95	1.68	4.14	4.56	3.16	2.915	ns
	-1	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.918	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-58 • 1.8 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	17.36	0.05	1.45	0.46	15.78	17.36	1.53	0.87	18.28	19.864	ns
	-1	0.55	14.77	0.04	1.23	0.39	13.42	14.77	1.54	0.87	15.55	16.897	ns
4 mA	STD	0.64	11.71	0.05	1.45	0.46	11.64	11.71	1.78	1.48	14.14	14.214	ns
	-1	0.55	9.96	0.04	1.23	0.39	9.90	9.96	1.78	1.48	12.03	12.091	ns
6 mA	STD	0.64	9.00	0.05	1.45	0.46	9.17	8.77	1.95	1.77	11.67	11.267	ns
	-1	0.55	7.66	0.04	1.23	0.39	7.80	7.46	1.95	1.77	9.92	9.585	ns
8 mA	STD	0.64	8.39	0.05	1.45	0.46	8.54	8.16	1.99	1.85	11.04	10.66	ns
	-1	0.55	7.14	0.04	1.23	0.39	7.27	6.94	1.99	1.85	9.40	9.068	ns
12 mA	STD	0.64	8.15	0.05	1.45	0.46	8.09	8.15	2.05	2.14	10.59	10.654	ns
	-1	0.55	6.94	0.04	1.23	0.39	6.88	6.94	2.05	2.14	9.01	9.063	ns
16 mA	STD	0.64	8.15	0.05	1.45	0.46	8.09	8.15	2.05	2.14	10.59	10.654	ns
	-1	0.55	6.94	0.04	1.23	0.39	6.88	6.94	2.05	2.14	9.01	9.063	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-59 • 1.8 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.26	0.05	1.36	0.46	9.75	12.67	1.24	0.82	12.26	15.17	ns
	-1	0.55	11.28	0.04	1.16	0.39	8.30	10.78	1.24	0.83	10.43	12.905	ns
4 mA	STD	0.64	7.73	0.05	1.36	0.46	6.13	7.25	1.46	1.41	8.63	9.749	ns
	-1	0.55	6.58	0.04	1.16	0.39	5.21	6.17	1.46	1.41	7.34	8.293	ns
6 mA	STD	0.64	4.97	0.05	1.36	0.46	4.29	4.54	1.62	1.68	6.79	7.039	ns
	-1	0.55	4.23	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.987	ns
8 mA	STD	0.64	4.39	0.05	1.36	0.46	4.29	4.54	1.62	1.68	6.79	7.039	ns
	-1	0.55	3.73	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.987	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-66 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	0	0	10	10
4 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	0	0	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

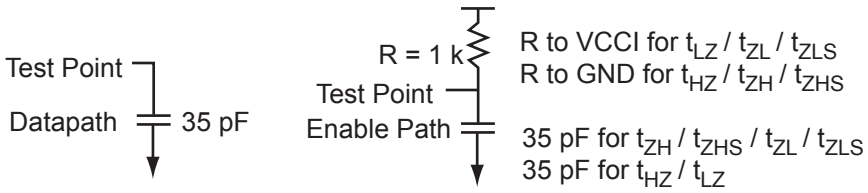


Figure 2-10 • AC Loading

Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	35

*Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.*

3.3 V PCI, 3.3 V PCI-X

The Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-76 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-11.

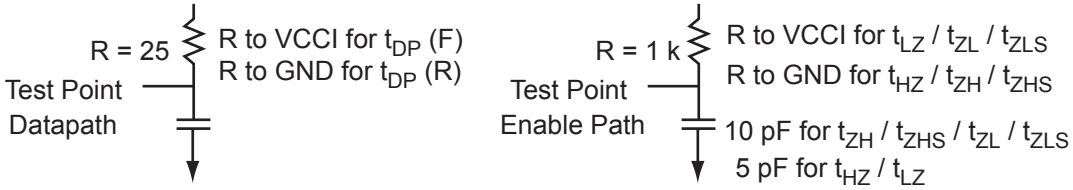


Figure 2-11 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 2-77.

Table 2-77 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for tDP(R) 0.615 * VCCI for tDP(F)	10

*Note: *Measuring point = Vtrip. See Table 2-18 on page 2-17 for a complete table of trip points.*

Timing Characteristics

Table 2-78 • 3.3 V PCI/PCI-X
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.64	2.58	0.05	0.95	0.46	1.27	0.94	3.12	3.60	2.49	2.18	ns
–1	0.55	2.19	0.04	0.81	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-79 • 3.3 V PCI/PCI-X
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.64	3.00	0.05	0.93	0.46	1.27	0.94	3.12	3.60	2.49	2.18	ns
–1	0.55	2.55	0.04	0.79	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Output Enable Register

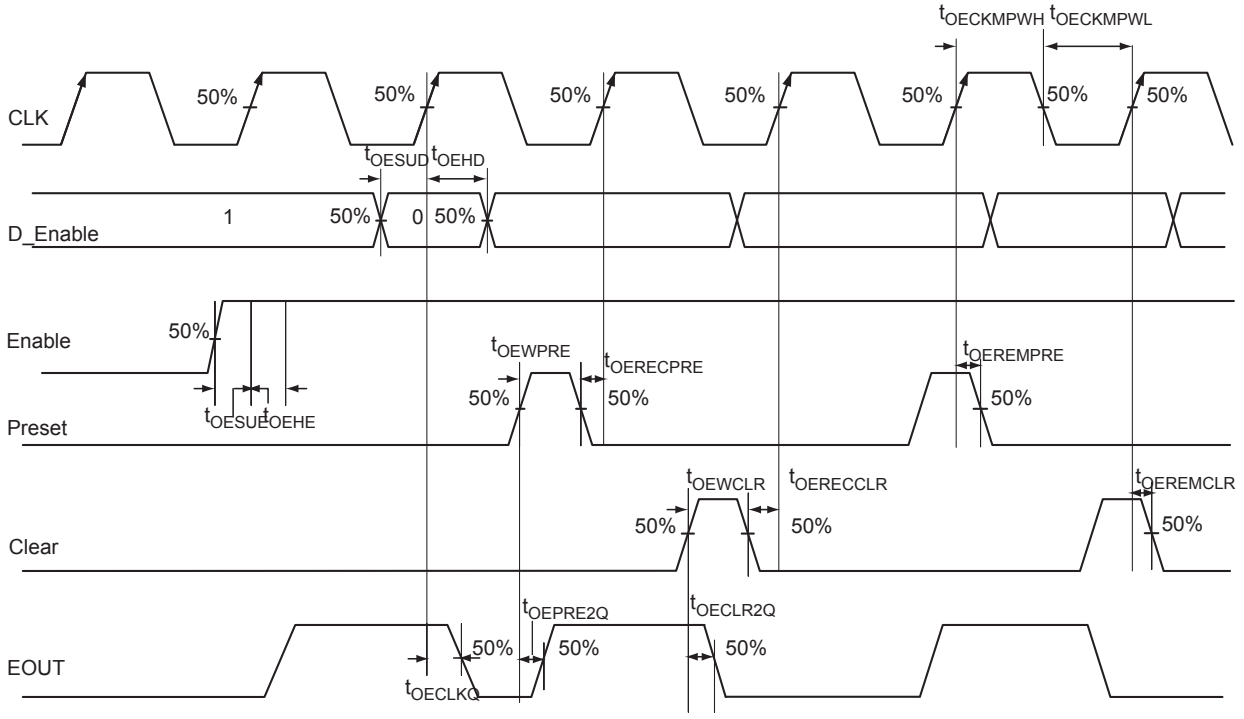


Figure 2-19 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-96 • **Output Enable Register Propagation Delays**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.54	0.64	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.38	0.45	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.53	0.62	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.32	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.32	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

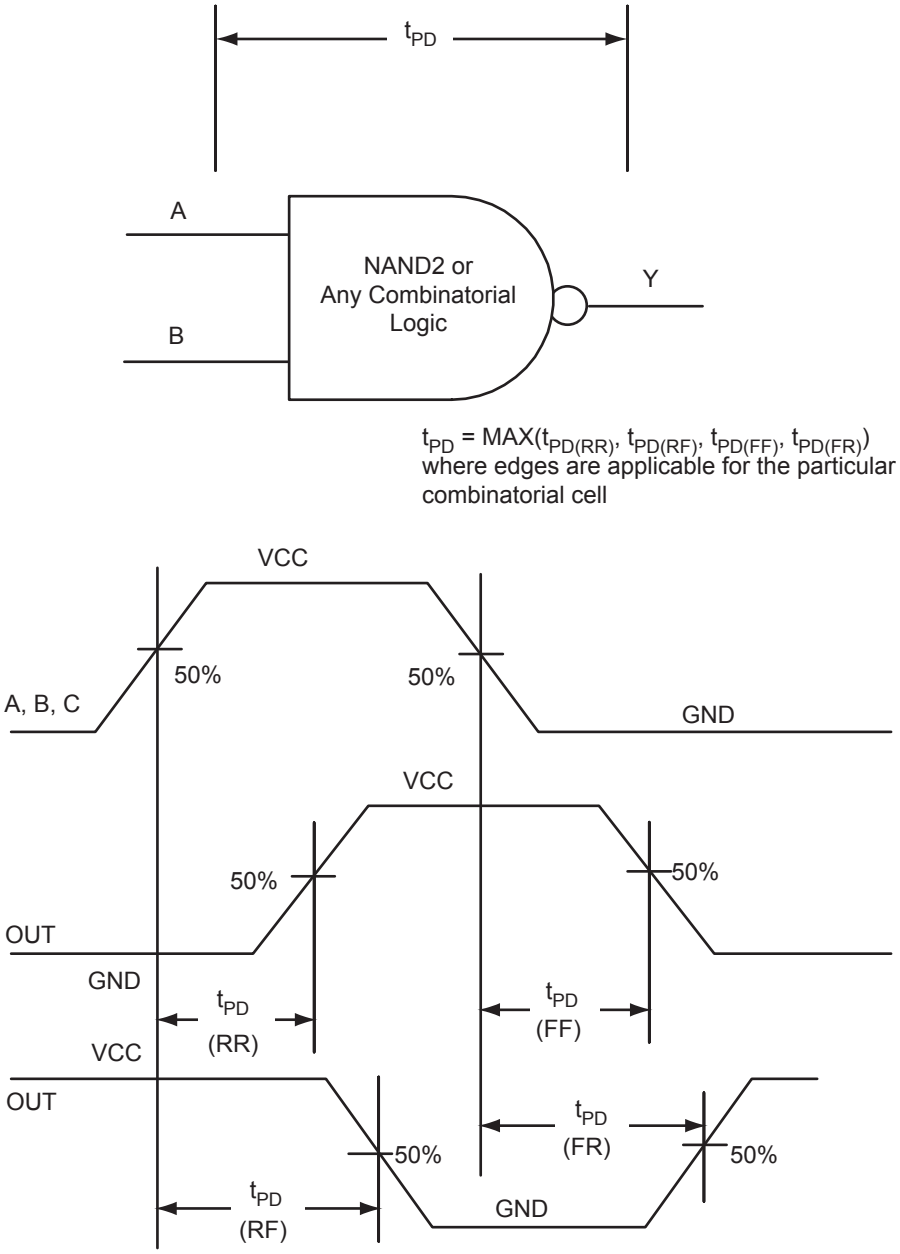


Figure 2-25 • **Timing Model and Waveforms**

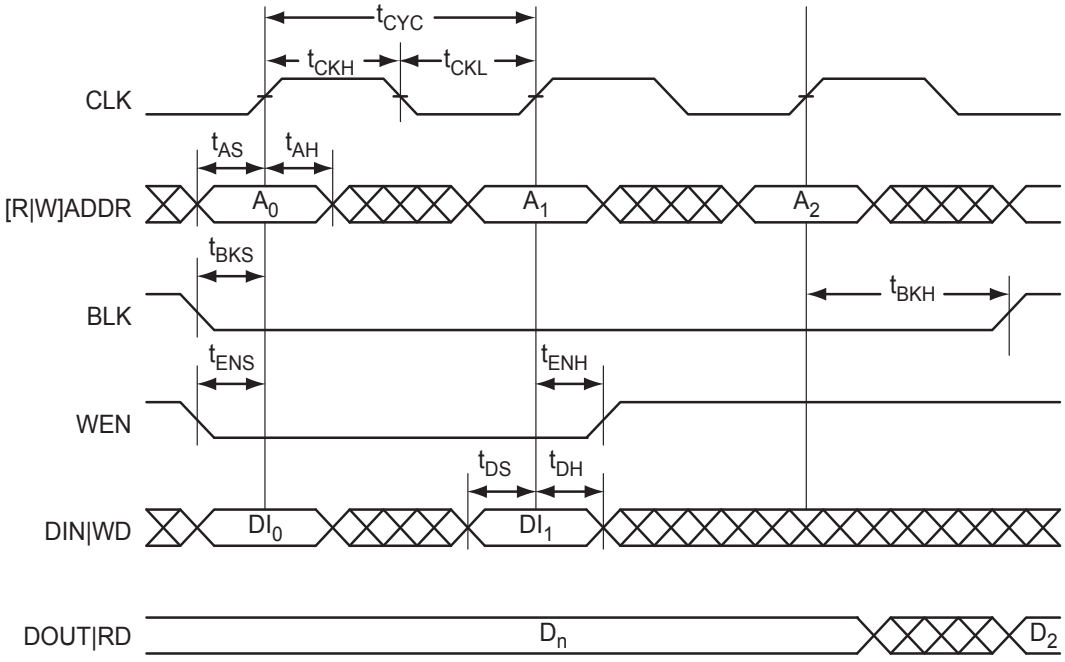


Figure 2-33 • **RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

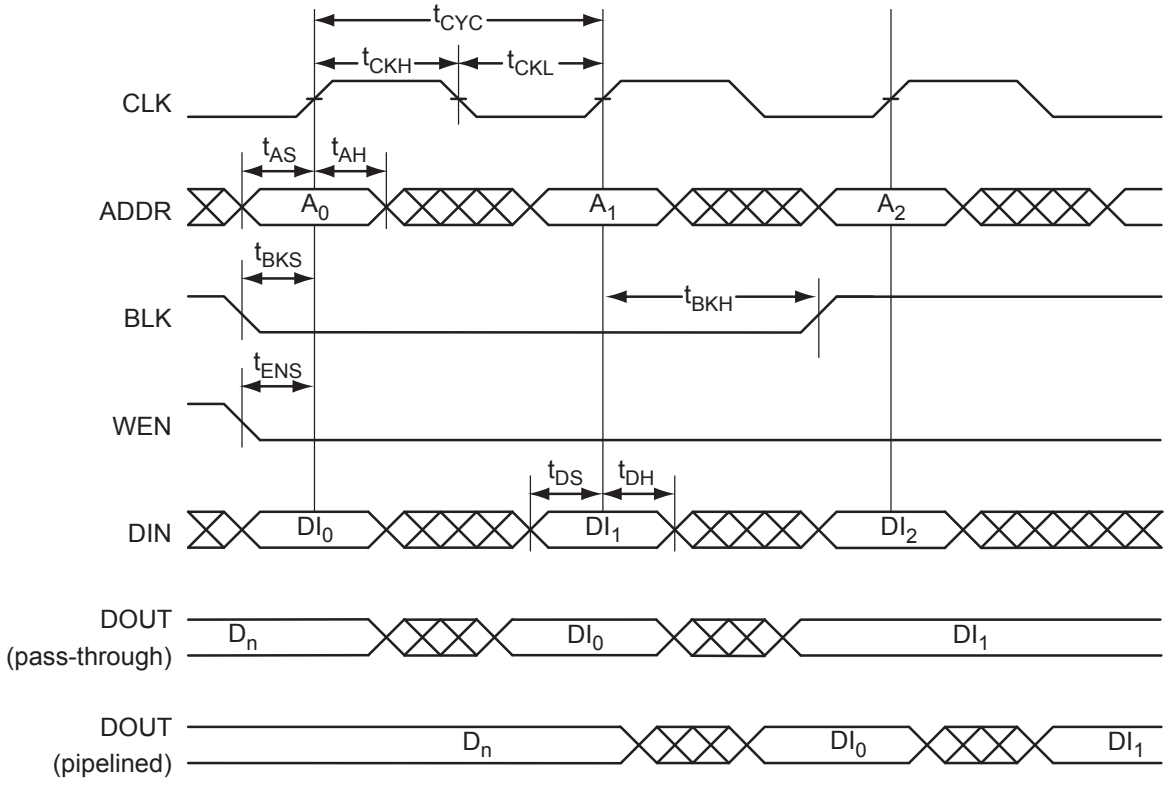


Figure 2-34 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

Table 2-120 • RAM512X18
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.35	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN, WEN Setup Time	0.11	0.13	ns
t_{ENH}	REN, WEN Hold Time	0.07	0.08	ns
t_{DS}	Input data (WD) Setup Time	0.22	0.26	ns
t_{DH}	Input data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (output retained, WMODE = 0)	2.58	3.03	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.07	1.26	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.43	0.50	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.50	0.59	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.10	1.29	ns
	RESET Low to Data Out Low on RD (pipelined)	1.10	1.29	ns
$t_{REMRSTB}$	RESET Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET Recovery	1.79	2.10	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.25	0.30	ns
t_{CYC}	Clock Cycle Time	3.85	4.53	ns
F_{MAX}	Maximum Frequency	260	221	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

VQ100	
Pin Number	A3P250 Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2

VQ100	
Pin Number	A3P250 Function
35	IO85RSB2
36	IO84RSB2
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC

VQ100	
Pin Number	A3P250 Function
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

QN132	
Pin Number	A3P125 Function
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0

QN132	
Pin Number	A3P125 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0

QN132	
Pin Number	A3P125 Function
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1

FG144	
Pin Number	A3P250 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO29RSB0
A8	VCC
A9	IO33RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO117UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO22RSB0
B8	IO30RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV1
C1	IO117VDB3
C2	GFA2/IO107PPB3
C3	GAC2/IO116UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO24RSB0
C8	IO31RSB0
C9	IO34RSB0
C10	GBA2/IO41PDB1
C11	IO41NDB1
C12	GBC2/IO43PPB1

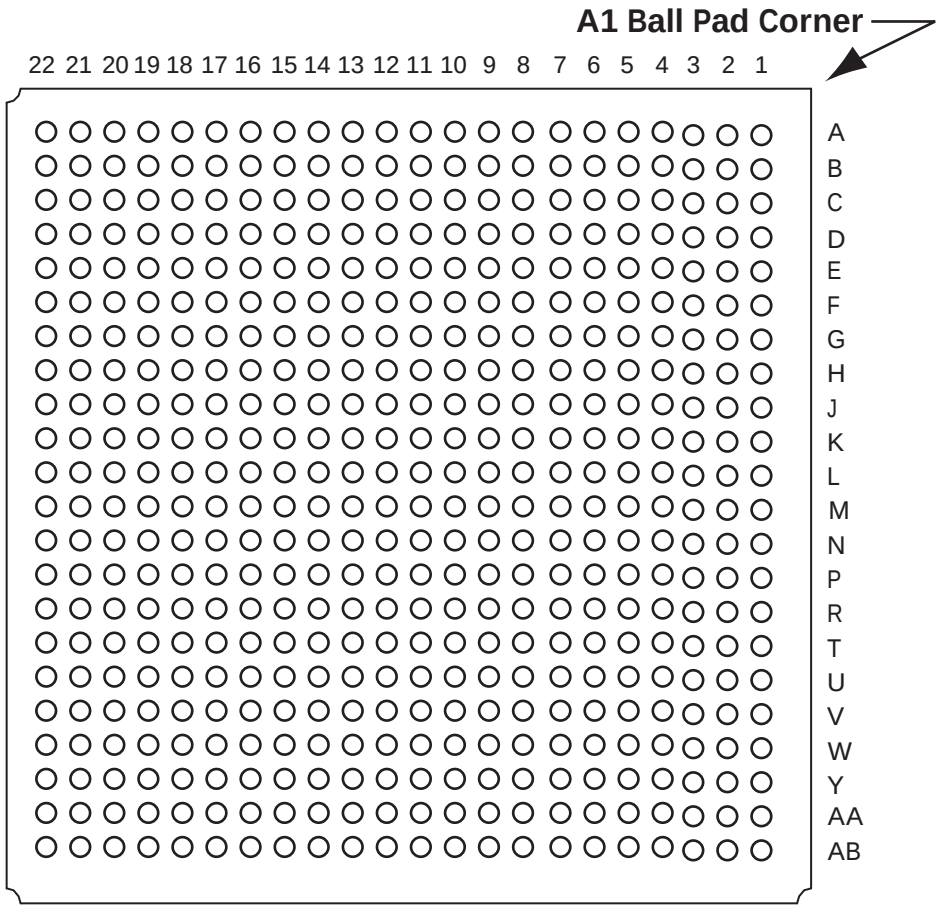
FG144	
Pin Number	A3P250 Function
D1	IO112NDB3
D2	IO112PDB3
D3	IO116VDB3
D4	GAA2/IO118UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO42PDB1
D10	IO42NDB1
D11	IO43NPB1
D12	GCB1/IO49PPB1
E1	VCC
E2	GFC0/IO110NDB3
E3	GFC1/IO110PDB3
E4	VCCIB3
E5	IO118VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO48PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO50NDB1
E12	IO51NDB1
F1	GFB0/IO109NPB3
F2	VCOMPLF
F3	GFB1/IO109PPB3
F4	IO107NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO48NDB1
F9	GCB0/IO49NPB1
F10	GND
F11	GCA1/IO50PDB1
F12	GCA2/IO51PDB1

FG144	
Pin Number	A3P250 Function
G1	GFA1/IO108PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO108NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO58UPB1
G9	IO53NDB1
G10	GCC2/IO53PDB1
G11	IO52NDB1
G12	GCB2/IO52PDB1
H1	VCC
H2	GFB2/IO106PDB3
H3	GFC2/IO105PSB3
H4	GEC1/IO100PDB3
H5	VCC
H6	IO79RSB2
H7	IO65RSB2
H8	GDB2/IO62RSB2
H9	GDC0/IO58VPB1
H10	VCCIB1
H11	IO54PSB1
H12	VCC
J1	GEB1/IO99PDB3
J2	IO106NDB3
J3	VCCIB3
J4	GEC0/IO100NDB3
J5	IO88RSB2
J6	IO81RSB2
J7	VCC
J8	TCK
J9	GDA2/IO61RSB2
J10	TDO
J11	GDA1/IO60UDB1
J12	GDB1/IO59UDB1

FG256	
Pin Number	**A3P1000 Function**
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2

FG256	
Pin Number	**A3P1000 Function**
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the Automotive ProASIC3 datasheet.

Revision	Changes	Page
Revision 5 (January 2013)	The "Automotive ProASIC3 Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43222).	1-III
	Added a note to Table 2-2 • Recommended Operating Conditions (SAR 43675): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-2
	The note in Table 2-116 • Automotive ProASIC3 CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42560).	2-80
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 4 (September 2012)	The "Specifying I/O States During Programming" section is new (SAR 34691).	1-6
	Table 2-2 • Recommended Operating Conditions was revised to change VPUMP values for programming mode from "3.0 to 3.6" to "3.15 to 3.45" (SAR 34703).	2-2
	Maximum values for VIL and VIH were corrected in LVPECL Table 2-86 • Minimum and Maximum DC Input and Output Levels (SAR 37693).	2-52
	Values were added for $F_{DDRIMAX}$ and F_{DDOMAX} in the following tables (SAR 34804): Table 2-99 • Input DDR Propagation Delays (T_J = 135°C) Table 2-100 • Input DDR Propagation Delays (T_J = 115°C) Table 2-102 • Output DDR Propagation Delays (T_J = 135°C) Table 2-103 • Output DDR Propagation Delays (T_J = 115°C)	2-64 to 2-68
	Added values for minimum pulse width and removed the FRMAX row from Table 2-108 through Table 2-115 in the "Global Tree Timing Characteristics" section. Use the software to determine the FRMAX for the device you are using (SAR 36966).	2-76
	SRAM collision data was added to Table 2-117 • RAM4K9 through Table 2-120 • RAM512X18. Maximum frequency, F_{MAX}, was updated in Table 2-118 • RAM512X18 (SAR 40859).	2-86 to 2-89
	The "VMVx I/O Supply Voltage (quiet)" section was revised. The sentence, "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" was replaced with, "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38323). VMV pins must be connected to the corresponding VCCI pins, as noted in the "VMVx I/O Supply Voltage (quiet)" section, for an ESD enhancement.	3-1
	Libero Integrated Design Environment (IDE) was changed to Libero Systeom-on-Chip (SoC) throughout the document (SAR 40266).	N/A
Revision 3 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1