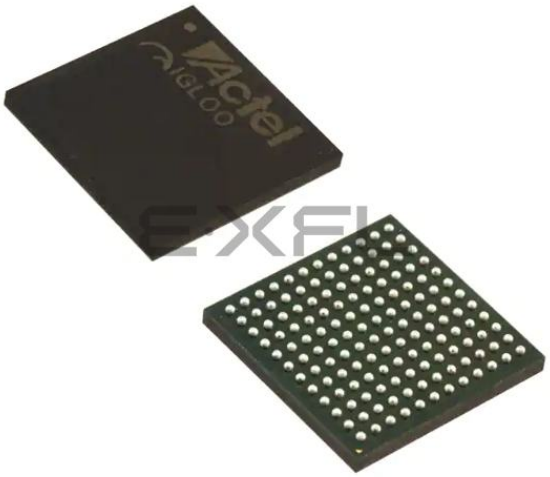

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	97
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p125-fgg144t

I/Os Per Package

ProASIC3 Devices	A3P060	A3P125	A3P250		A3P1000	
	I/O Type					
Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O [2]	Differential I/O Pairs	Single-Ended I/O [2]	Differential I/O Pairs
VQ100	71	71	68	13	–	–
FG144	96	97	97	24	97	25
FG256	–	–	157	38	177	44
FG484	–	–	–	–	300	74
QNG132	–	84	87	19	–	–

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the ProASIC3 FPGA Fabric User's Guide to ensure complying with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of available single-ended I/Os by two.*
3. *FG256 and FG484 are footprint-compatible packages.*

Automotive ProASIC3 Device Status

Automotive ProASIC3 Devices	Status
A3P060	Production
A3P125	Production
A3P250	Production
A3P1000	Production

Temperature Grade Offerings

Package	A3P060	A3P125	A3P250	A3P1000
VQ100	C, I, T	C, I, T	C, I, T	–
FG144	C, I, T	C, I, T	C, I, T	C, I, T
FG256	–	–	C, I, T	C, I, T
FG484	–	–	–	C, I, T
QNG132	–	C, I, T	C, I, T	–

Notes:
1. *C = Commercial temperature range: 0°C to 70°C*
2. *I = Industrial temperature range: –40°C to 85°C*
3. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
4. *Specifications for Commercial and Industrial grade devices can be found in the ProASIC3 Flash Family FPGAs datasheet.*

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
T (Grade 1 and Grade 2), Commercial, Industrial	3	3

Notes:
1. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
2. *Specifications for Commercial and Industrial grade devices can be found in the ProASIC3 Flash Family FPGAs datasheet.*

Contact your local Microsemi SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{110\text{°C} - 70\text{°C}}{20.5\text{°C/W}} = 1.951\ \text{W}$$

EQ 2

Table 2-4 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft./min.	θ_{ja} 500 ft./min.	Units
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	°C/W
Fine Pitch Ball Grid Array (FBGA)	See note*	144	3.8	26.9	22.9	21.5	°C/W
	See note*	256	3.8	26.6	22.8	21.5	°C/W
	See note*	484	3.2	20.5	17.0	15.9	°C/W
	A3P1000	144	6.3	31.6	26.2	24.2	°C/W
	A3P1000	256	6.6	28.1	24.4	22.7	°C/W
	A3P1000	484	8.0	23.3	19.0	16.7	°C/W

*Note: *This information applies to all ProASIC3 devices except the A3P1000. Detailed device/package thermal information will be available in future revisions of the datasheet.*

Temperature and Voltage Derating Factors

Table 2-5 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 115°C, VCC = 1.425 V)**

Array Voltage VCC (V)	–40°C	0°C	25°C	70°C	85°C	115°C	125°C	135°C
1.425	0.83	0.88	0.90	0.95	0.97	1.00	1.01	1.02
1.5	0.79	0.83	0.85	0.90	0.92	0.95	0.96	0.97
1.575	0.76	0.80	0.82	0.87	0.88	0.91	0.93	0.94

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Standard Plus I/O Banks

	VMV (V)	Static Power PDC2 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.72
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	18.13

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on VMV.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI} and VMV.*

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-13 on page 2-12.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-13 on page 2-12.

PLL Contribution—P_{PLL}

$$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-12 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

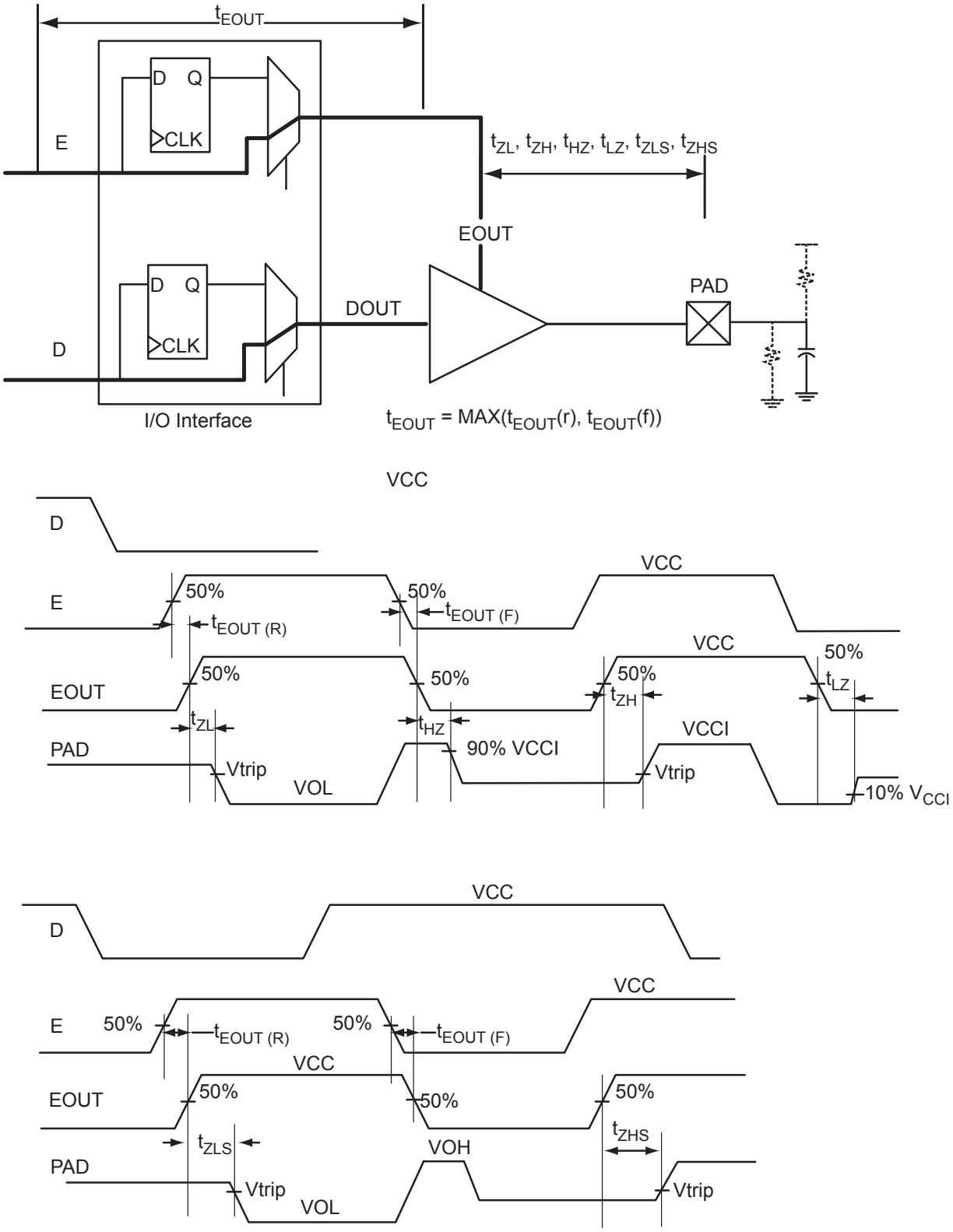

Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-14 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 125°C junction temperature.

Table 2-15 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	High	–0.3	0.30 * VCCI	0.7 * V_{CCI}	3.6	0.25 * VCCI	0.75 * V_{CCI}	4	4
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 125°C junction temperature.

**Table 2-28 • I/O Short Currents IOSH/IOSL
Applicable to Advanced I/O Banks**

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	6 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

*Note: *T_J = 100°C*

Table 2-29 • I/O Short Currents IOSH/IOSL Applicable to Standard Plus I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
2.5 V LVCMOS	2 mA	18	16
	6 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

*Note: *T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-30 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months
125°C	25 days
135°	12 days

Timing Characteristics

Table 2-46 • 2.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.69	0.05	1.45	0.46	8.76	9.69	1.48	1.25	11.26	12.187	ns
	-1	0.55	8.24	0.04	1.23	0.39	7.45	8.24	1.48	1.25	9.58	10.367	ns
6 mA	STD	0.64	5.78	0.05	1.45	0.46	5.63	5.78	1.68	1.62	8.13	8.277	ns
	-1	0.55	4.91	0.04	1.23	0.39	4.79	4.91	1.69	1.63	6.92	7.04	ns
12 mA	STD	0.64	3.98	0.05	1.45	0.46	4.05	3.84	1.82	1.86	6.55	6.338	ns
	-1	0.55	3.39	0.04	1.23	0.39	3.45	3.27	1.83	1.86	5.58	5.392	ns
16 mA	STD	0.64	3.75	0.05	1.45	0.46	1.85	1.69	3.76	3.97	3.06	2.926	ns
	-1	0.55	3.19	0.04	1.23	0.39	1.85	1.69	3.20	3.38	3.06	2.929	ns
24 mA	STD	0.64	3.45	0.05	1.45	0.46	1.70	1.35	3.84	4.47	2.92	2.585	ns
	-1	0.55	2.94	0.04	1.23	0.39	1.71	1.35	3.27	3.80	2.92	2.586	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-47 • 2.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	12.12	0.05	1.45	0.46	12.54	12.74	1.48	1.19	15.04	15.243	ns
	-1	0.55	10.31	0.04	1.23	0.39	10.67	10.84	1.48	1.20	12.80	12.966	ns
6 mA	STD	0.64	8.24	0.05	1.45	0.46	9.07	8.74	1.68	1.57	11.57	11.237	ns
	-1	0.55	7.01	0.04	1.23	0.39	7.71	7.43	1.69	1.57	9.84	9.559	ns
12 mA	STD	0.64	6.91	0.05	1.45	0.46	7.04	6.62	1.82	1.80	9.54	9.117	ns
	-1	0.55	5.88	0.04	1.23	0.39	5.99	5.63	1.83	1.80	8.11	7.756	ns
16 mA	STD	0.64	6.44	0.05	1.45	0.46	6.56	6.18	1.86	1.86	9.06	8.678	ns
	-1	0.55	5.48	0.04	1.23	0.39	5.58	5.26	1.86	1.86	7.71	7.382	ns
24 mA	STD	0.64	6.16	0.05	1.45	0.46	6.15	6.16	1.90	2.10	8.65	8.657	ns
	-1	0.55	5.24	0.04	1.23	0.39	5.23	5.24	1.90	2.10	7.36	7.364	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-90 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

*Note: *See Figure 2-15 on page 2-53 for more information.*

Table 2-100 • Input DDR Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.33	0.38	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.46	0.54	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.34	0.40	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.55	0.65	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.68	0.80	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.27	0.31	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.37	0.43	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

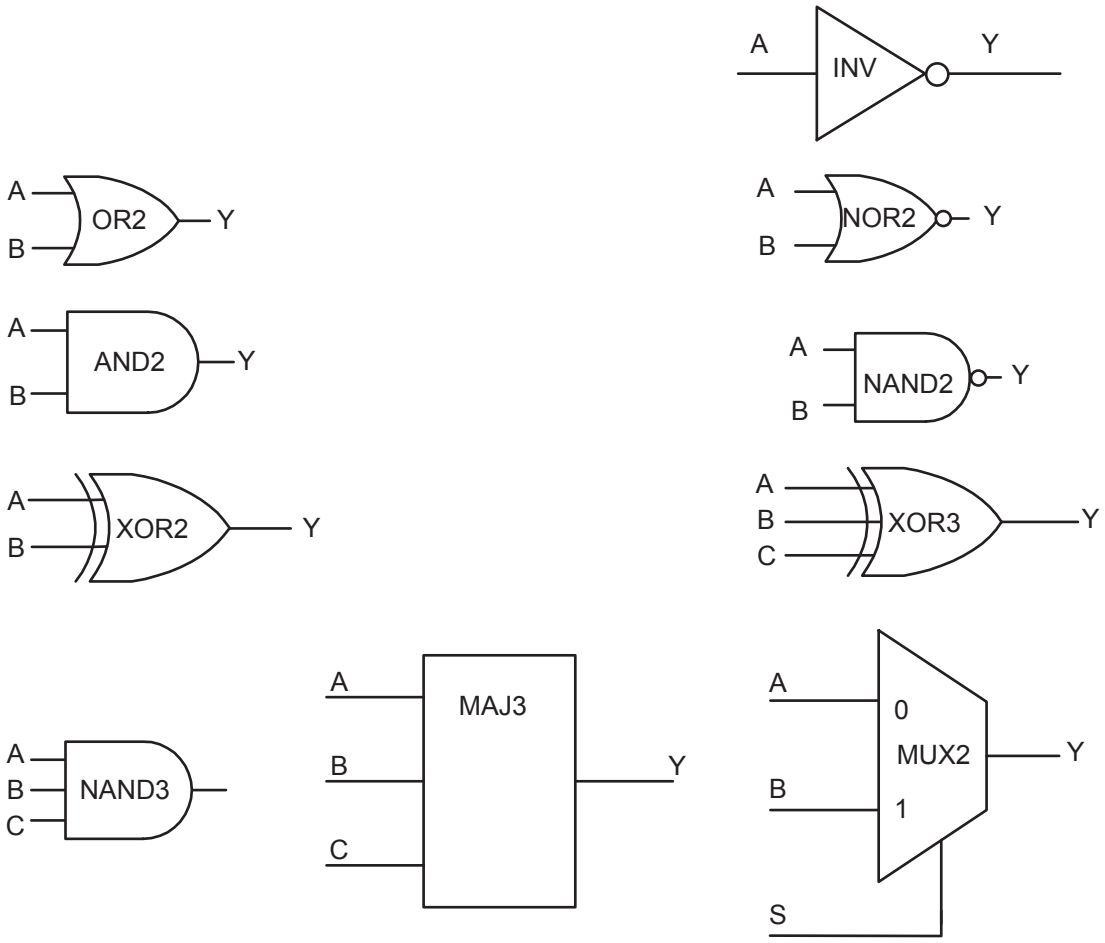

Figure 2-24 • **Sample of Combinatorial Cells**

Table 2-112 • A3P250 Global Resource
Commercial-Case Conditions: T_J = 135°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.96	1.25	1.13	1.47	ns
t_{RCKH}	Input High Delay for Global Clock	0.94	1.28	1.10	1.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35		0.41	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-113 • A3P250 Global Resource
Commercial-Case Conditions: T_J = 115°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.94	1.22	1.10	1.44	ns
t_{RCKH}	Input High Delay for Global Clock	0.92	1.25	1.08	1.47	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.34		0.40	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

FG144	
Pin Number	A3P060 Function
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO57RSB1
K9	GDC2/IO56RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	VCCIB1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG144	
Pin Number	A3P125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	A3P125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	A3P125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG484	
Pin Number	**A3P1000 Function**
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	IO181RSB2
AA5	IO178RSB2
AA6	IO175RSB2
AA7	IO169RSB2
AA8	IO166RSB2
AA9	IO160RSB2
AA10	IO152RSB2
AA11	IO146RSB2
AA12	IO139RSB2
AA13	IO133RSB2
AA14	NC
AA15	NC
AA16	IO122RSB2
AA17	IO119RSB2
AA18	IO117RSB2
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	IO180RSB2
AB5	IO176RSB2
AB6	IO173RSB2

FG484	
Pin Number	**A3P1000 Function**
AB7	IO167RSB2
AB8	IO162RSB2
AB9	IO156RSB2
AB10	IO150RSB2
AB11	IO145RSB2
AB12	IO144RSB2
AB13	IO132RSB2
AB14	IO127RSB2
AB15	IO126RSB2
AB16	IO123RSB2
AB17	IO121RSB2
AB18	IO118RSB2
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND

Revision	Changes	Page
Revision 2 (May 2012)	The "Extended Temperature AEC-Q100–Qualified Devices" section was modified to include the low end of the temperature range, –40°C, for Grade 1 and Grade 2 AEC-Q100 qualified devices (SAR 34915).	I
	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34674).	I, 1-1
	The Y security option and Licensed DPA Logo were added to the "Automotive ProASIC3 Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34719).	III
	A note defining T_A and T_J was added to the "Automotive ProASIC3 Ordering Information" section (SAR 37547).	III
	The following sentence was deleted from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of Automotive ProASIC3 devices via an IEEE 1532 JTAG interface" (SAR 34682).	1-3
	In Table 2-2 • Recommended Operating Conditions, VCCPLL analog power supply (PLL) was changed from "1.4 to 1.6" to "1.425 to 1.575" (SAR 34718).	2-2
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *Automotive ProASIC3 FPGA Fabric User's Guide* (SAR 34738).	2-10
	t_{DOUT} was corrected to t_{DIN} in Figure 2-4 • Input Buffer Timing Model and Delays (example) (SAR 37111).	2-13
	The equations in the notes for Table 2-27 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34754).	2-23
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34882).	2-27
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34795): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-33
	The table notes for Table 2-82 • Minimum and Maximum DC Input and Output Levels were not necessary and were removed (SAR 34811).	2-50
	The following figures were deleted (SAR 29991). Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34861). Figure 2-35 • Write Access after Write to Same Address Figure 2-36 • Read Access after Write to Same Address Figure 2-35 • Read Access after Write to Same Address The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-39 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35744).	2-83, 2-86, 2-92, 2-94
	Figure 2-37 • FIFO Read and Figure 2-38 • FIFO Write are new (SAR 34838).	2-91
	Table 2-116 • Automotive ProASIC3 CCC/PLL Specification was updated. A note was added to indicate that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34822).	2-80