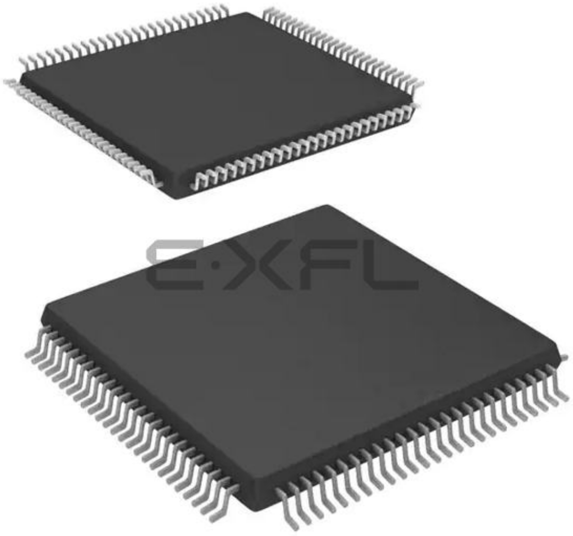


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	71
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p125-vq100t

Temperature Grade Offerings

Package	A3P060	A3P125	A3P250	A3P1000
VQ100	C, I, T	C, I, T	C, I, T	–
FG144	C, I, T	C, I, T	C, I, T	C, I, T
FG256	–	–	C, I, T	C, I, T
FG484	–	–	–	C, I, T
QNG132	–	C, I, T	C, I, T	–

Notes:

1. *C = Commercial temperature range: 0°C to 70°C*
2. *I = Industrial temperature range: –40°C to 85°C*
3. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A *and 115°C* T_J
   Grade 1 = 125°C T_A *and 135°C* T_J
4. *Specifications for Commercial and Industrial grade devices can be found in the* ProASIC3 Flash Family FPGAs *datasheet.*

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
T (Grade 1 and Grade 2), Commercial, Industrial	3	3

Notes:

1. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A *and 115°C* T_J
   Grade 1 = 125°C T_A *and 135°C* T_J
2. *Specifications for Commercial and Industrial grade devices can be found in the* ProASIC3 Flash Family FPGAs *datasheet.*

Contact your local Microsemi SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

Advanced Architecture

The proprietary Automotive ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The Automotive ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM memory
- Extensive CCCs and PLLs
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the Automotive ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

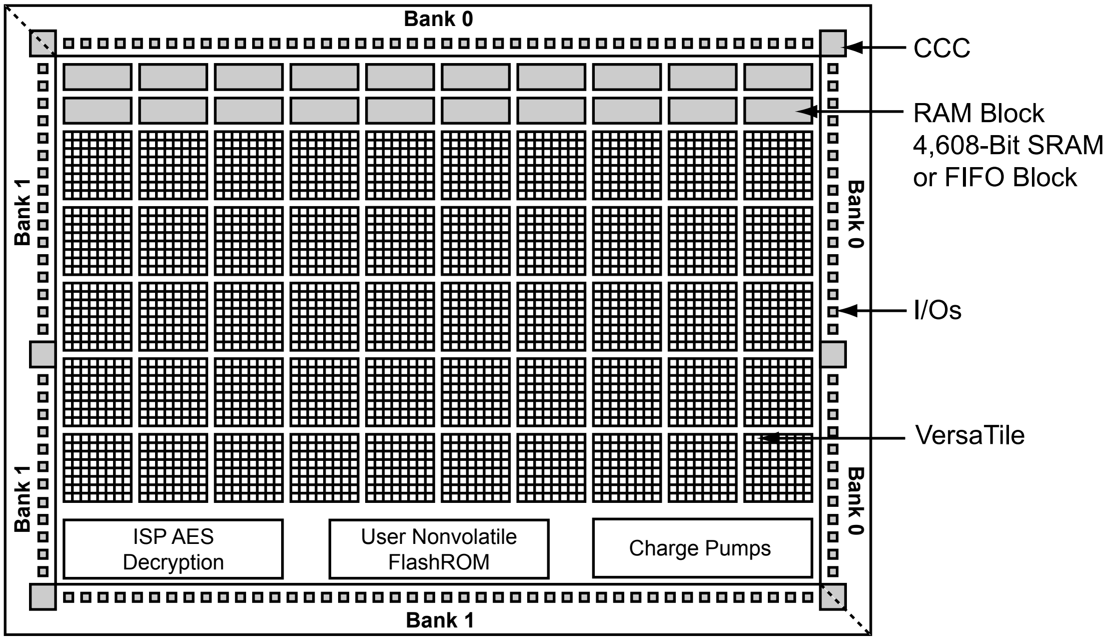


Figure 1-1 • **Automotive ProASIC3 Device Architecture Overview with Two I/O Banks (A3P060 and A3P125)**

Calculating Power Dissipation

Quiescent Supply Current

Table 2-6 • **Quiescent Supply Current Characteristics**

	A3P060	A3P125	A3P250	A3P1000
Typical (25°C)	2 mA	2 mA	3 mA	8 mA
Maximum (Automotive Grade 1) – 135°C	53 mA	53 mA	106 mA	265 mA
Maximum (Automotive Grade 2) – 115°C	26 mA	26 mA	53 mA	131 mA

Note: IDD Includes VCC, VPUMP, VCCI, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-7 and Table 2-10 on page 2-8.

Power per I/O Pin

Table 2-7 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Advanced I/O Banks**

	VMV (V)	Static Power PDC2 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.69
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

1. P_{DC2} *is the static power (where applicable) measured on VMV.*
2. P_{AC9} *is the total dynamic power measured on* V_{CC} *and VMV.*

Table 2-21 • **Summary of I/O Timing Characteristics—Software Default Settings**
–1 Speed Grade, Automotive-Case Conditions: T_J = 115°C, Worst Case VCC = 1.425 V
Worst Case VCCI = 3.0 V
Standard Plus I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.11	ns
1.8 V LVCMOS	8 mA	High	35 pF	–	0.55	3.73	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.99	ns
1.5 V LVCMOS	4 mA	High	35 pF	–	0.55	4.60	0.04	1.35	0.39	4.61	5.05	2.07	1.85	6.74	7.18	ns
3.3 V PCI	Per PCI spec	High	10 pF	25 [2]	0.55	2.19	0.04	0.81	0.39	1.27	0.94	2.65	3.06	1.27	0.94	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25 [2]	0.55	2.19	0.04	0.79	0.39	1.27	0.94	2.65	3.06	1.27	0.94	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-48 for connectivity. This resistor is not required during normal operation.*

Table 2-29 • I/O Short Currents IOSH/IOSL Applicable to Standard Plus I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
2.5 V LVCMOS	2 mA	18	16
	6 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: *T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-30 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months
125°C	25 days
135°	12 days

Table 2-41 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	7.79	0.05	1.08	0.45	7.94	6.80	1.22	1.23	7.94	6.80	ns
	-1	0.55	6.85	0.04	0.95	0.39	6.98	5.98	1.26	1.27	6.98	5.98	ns
6 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
8 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
12 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns
16 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-42 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	10.47	0.05	1.08	0.45	10.66	9.11	1.22	1.16	10.66	9.11	ns
	-1	0.55	9.21	0.04	0.95	0.39	9.38	8.01	1.26	1.20	9.38	8.01	ns
6 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
8 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
12 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns
16 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-58 • 1.8 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	17.36	0.05	1.45	0.46	15.78	17.36	1.53	0.87	18.28	19.864	ns
	-1	0.55	14.77	0.04	1.23	0.39	13.42	14.77	1.54	0.87	15.55	16.897	ns
4 mA	STD	0.64	11.71	0.05	1.45	0.46	11.64	11.71	1.78	1.48	14.14	14.214	ns
	-1	0.55	9.96	0.04	1.23	0.39	9.90	9.96	1.78	1.48	12.03	12.091	ns
6 mA	STD	0.64	9.00	0.05	1.45	0.46	9.17	8.77	1.95	1.77	11.67	11.267	ns
	-1	0.55	7.66	0.04	1.23	0.39	7.80	7.46	1.95	1.77	9.92	9.585	ns
8 mA	STD	0.64	8.39	0.05	1.45	0.46	8.54	8.16	1.99	1.85	11.04	10.66	ns
	-1	0.55	7.14	0.04	1.23	0.39	7.27	6.94	1.99	1.85	9.40	9.068	ns
12 mA	STD	0.64	8.15	0.05	1.45	0.46	8.09	8.15	2.05	2.14	10.59	10.654	ns
	-1	0.55	6.94	0.04	1.23	0.39	6.88	6.94	2.05	2.14	9.01	9.063	ns
16 mA	STD	0.64	8.15	0.05	1.45	0.46	8.09	8.15	2.05	2.14	10.59	10.654	ns
	-1	0.55	6.94	0.04	1.23	0.39	6.88	6.94	2.05	2.14	9.01	9.063	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-59 • 1.8 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.26	0.05	1.36	0.46	9.75	12.67	1.24	0.82	12.26	15.17	ns
	-1	0.55	11.28	0.04	1.16	0.39	8.30	10.78	1.24	0.83	10.43	12.905	ns
4 mA	STD	0.64	7.73	0.05	1.36	0.46	6.13	7.25	1.46	1.41	8.63	9.749	ns
	-1	0.55	6.58	0.04	1.16	0.39	5.21	6.17	1.46	1.41	7.34	8.293	ns
6 mA	STD	0.64	4.97	0.05	1.36	0.46	4.29	4.54	1.62	1.68	6.79	7.039	ns
	-1	0.55	4.23	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.987	ns
8 mA	STD	0.64	4.39	0.05	1.36	0.46	4.29	4.54	1.62	1.68	6.79	7.039	ns
	-1	0.55	3.73	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.987	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-73 • **1.5 V LVCMOS Low Slew**
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.83	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.76	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.83	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	9.21	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns
6 mA	STD	0.63	10.10	0.05	1.40	0.45	10.28	9.62	2.05	1.80	12.70	12.04	ns
	-1	0.53	8.59	0.04	1.19	0.38	8.75	8.18	2.05	1.80	10.81	10.24	ns
8 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns
12 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-74 • **1.5 V LVCMOS High Slew**
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	8.47	0.05	1.54	0.45	7.38	9.05	1.81	1.45	9.80	11.47	ns
	-1	0.53	7.21	0.04	1.31	0.38	6.28	7.70	1.81	1.45	8.34	9.75	ns
4 mA	STD	0.63	5.24	0.05	1.54	0.45	5.25	5.75	2.00	1.78	7.67	8.17	ns
	-1	0.53	4.45	0.04	1.31	0.38	4.46	4.89	2.00	1.78	6.52	6.95	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-75 • **1.5 V LVCMOS Low Slew**
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.07	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.12	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.04	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	8.54	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Input Register

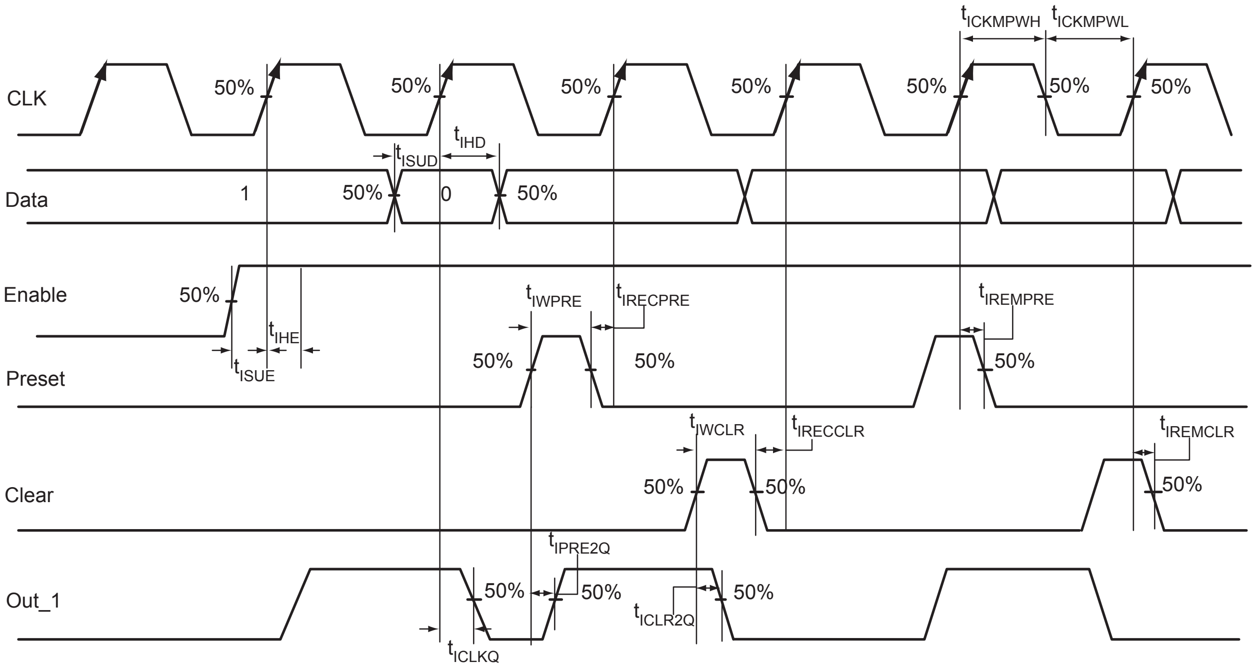


Figure 2-17 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-92 • **Input Data Register Propagation Delays**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.29	0.34	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.32	0.38	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.45	0.53	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.55	0.65	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.55	0.65	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.27	0.32	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.27	0.32	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Output Enable Register

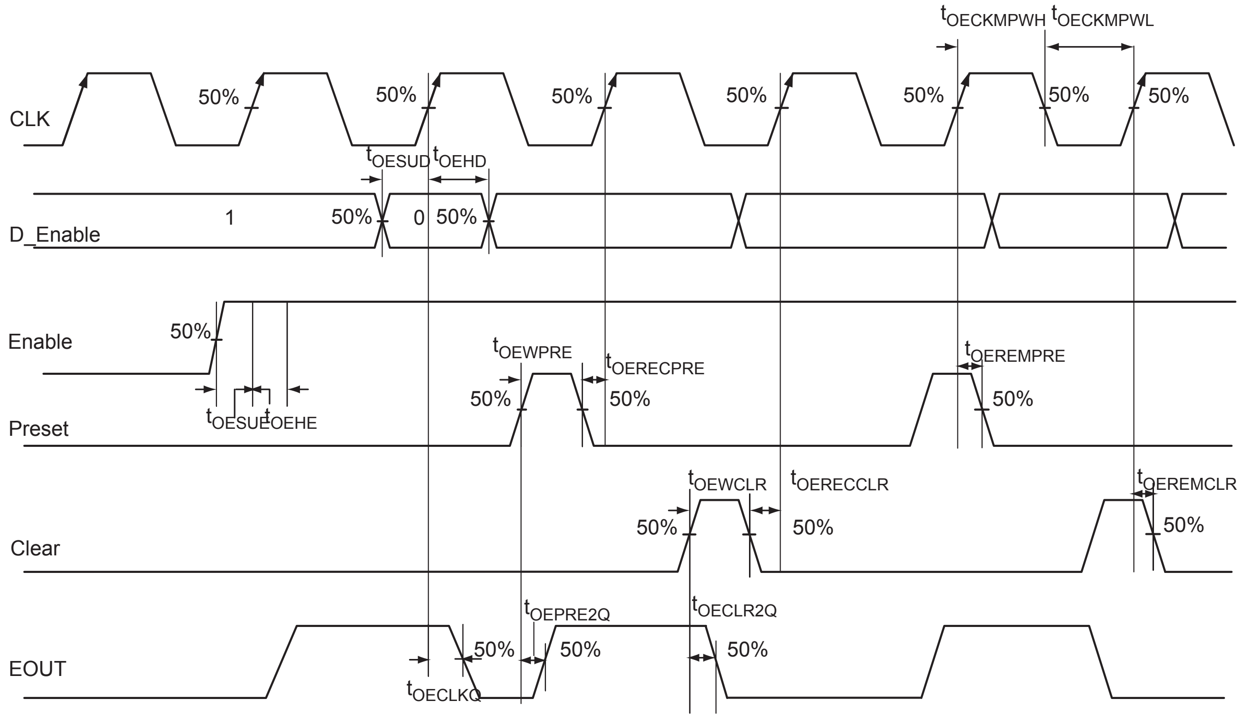


Figure 2-19 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-96 • Output Enable Register Propagation Delays
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.54	0.64	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.38	0.45	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.53	0.62	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.32	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.32	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

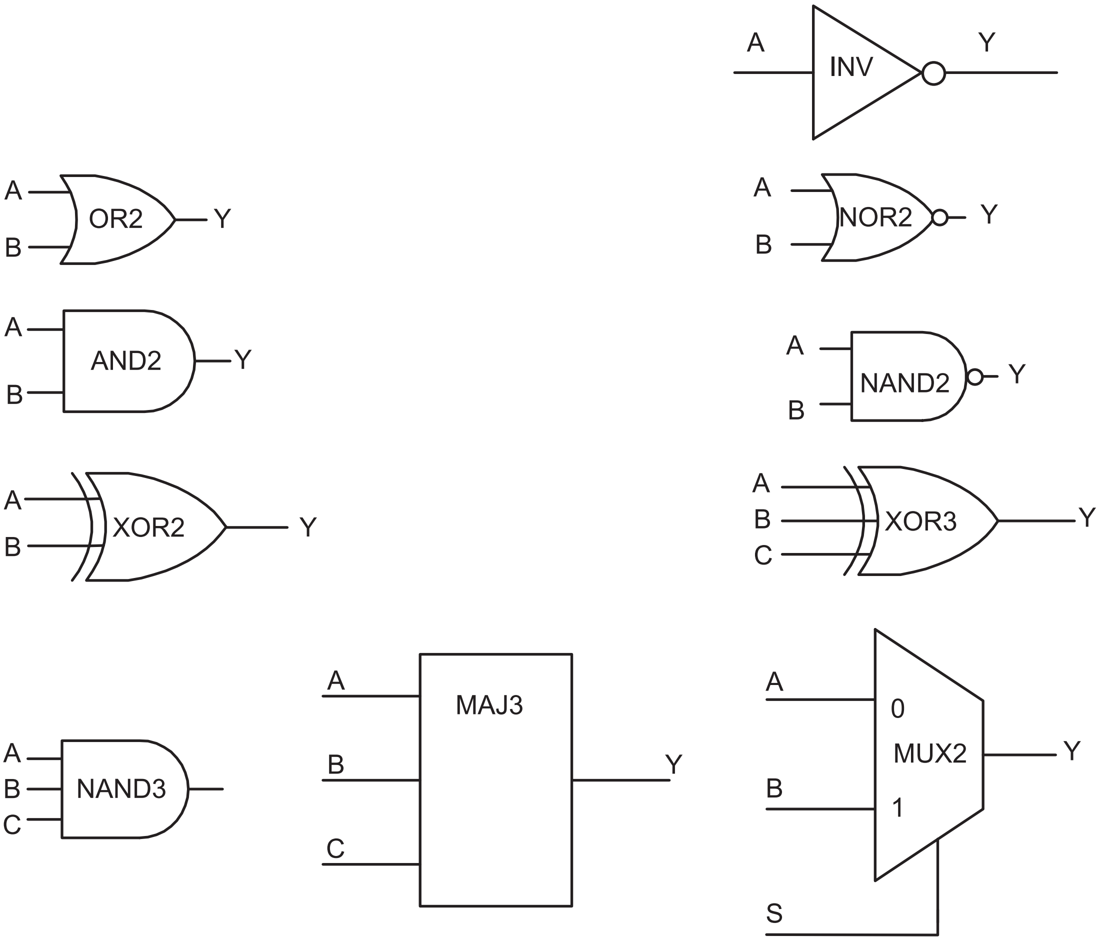


Figure 2-24 • **Sample of Combinatorial Cells**

Timing Characteristics

***Table 2-104* • Combinatorial Cell Propagation Delays**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.49	0.57	ns
AND2	Y = A · B	t_{PD}	0.57	0.67	ns
NAND2	Y = !(A · B)	t_{PD}	0.57	0.67	ns
OR2	Y = A + B	t_{PD}	0.59	0.69	ns
NOR2	Y = !(A + B)	t_{PD}	0.59	0.69	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.90	1.05	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.85	1.00	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.06	1.25	ns
MUX2	Y = A !S + B S	t_{PD}	0.62	0.72	ns
AND3	Y = A · B · C	t_{PD}	0.68	0.80	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

***Table 2-105* • Combinatorial Cell Propagation Delays**
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.48	0.56	ns
AND2	Y = A · B	t_{PD}	0.56	0.66	ns
NAND2	Y = !(A · B)	t_{PD}	0.56	0.66	ns
OR2	Y = A + B	t_{PD}	0.58	0.68	ns
NOR2	Y = !(A + B)	t_{PD}	0.58	0.68	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.88	1.03	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.83	0.98	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.04	1.23	ns
MUX2	Y = A !S + B S	t_{PD}	0.60	0.71	ns
AND3	Y = A · B · C	t_{PD}	0.67	0.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Embedded SRAM and FIFO Characteristics

SRAM

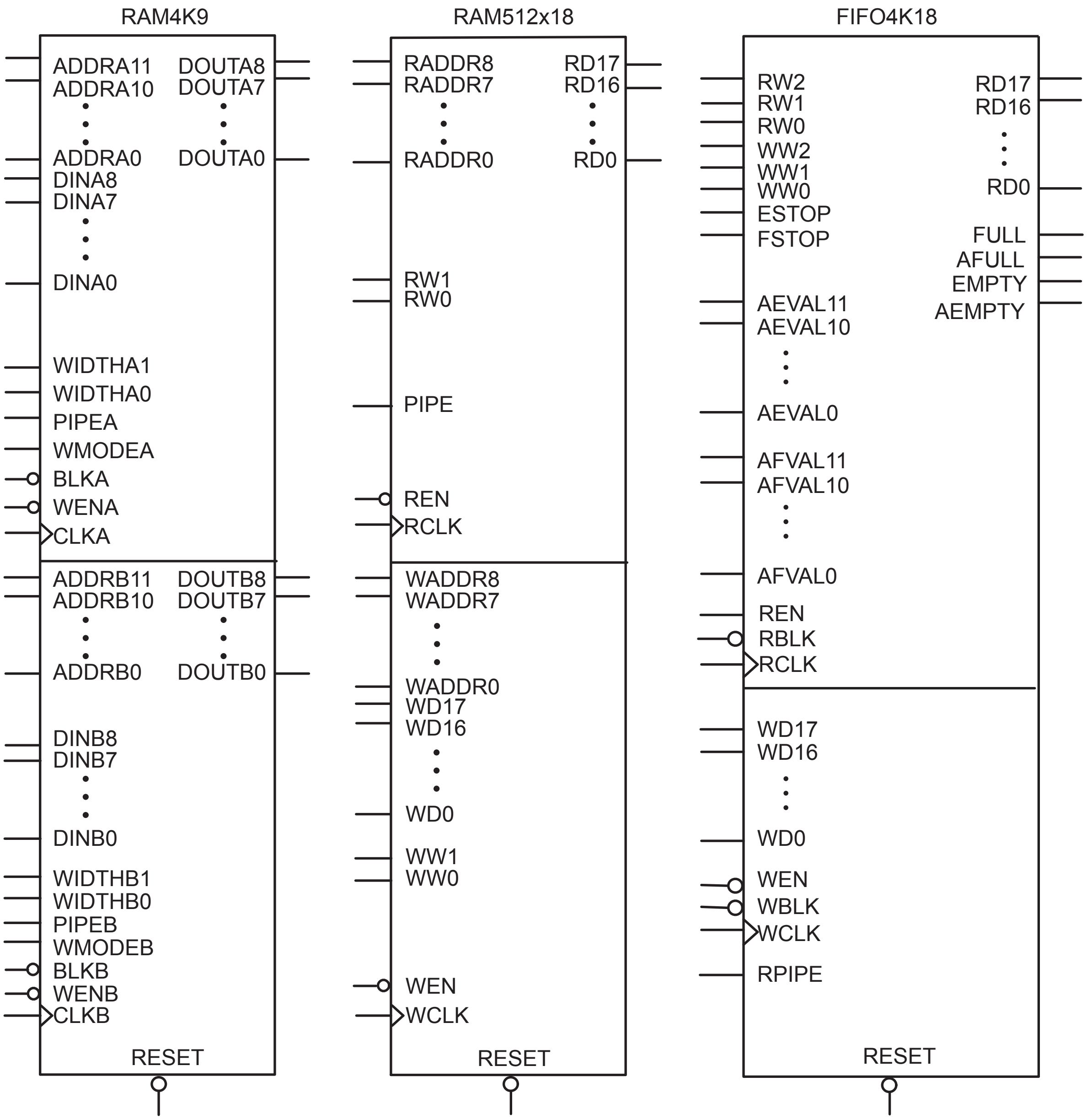


Figure 2-30 • **RAM Models**

Timing Waveforms

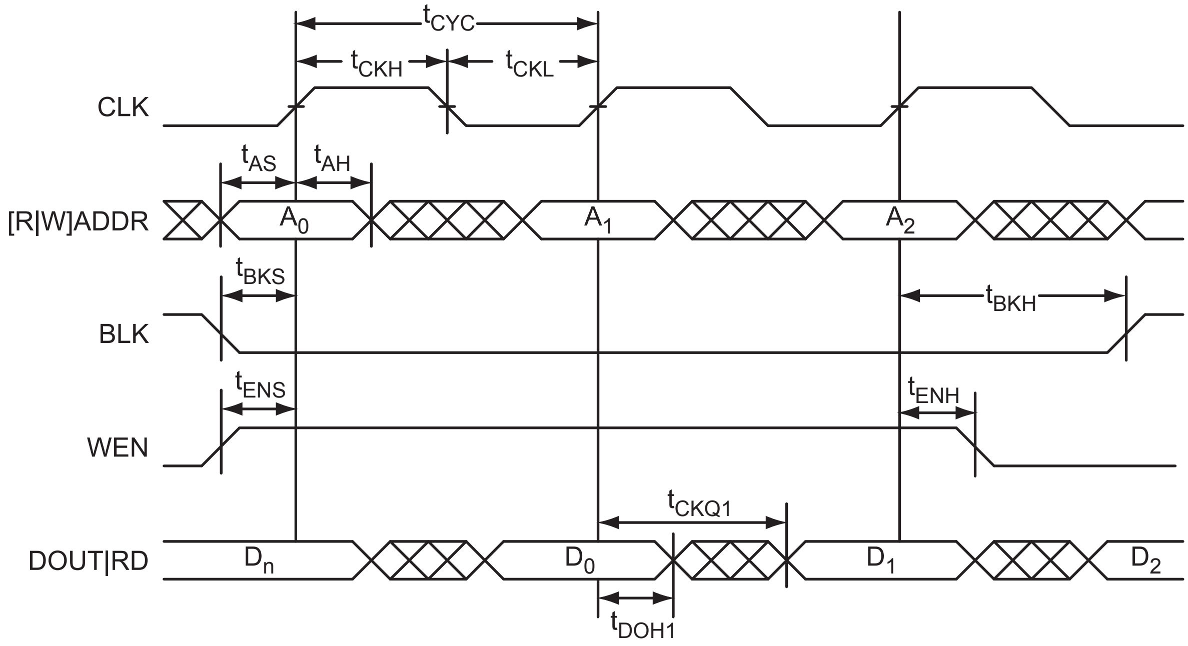


Figure 2-31 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

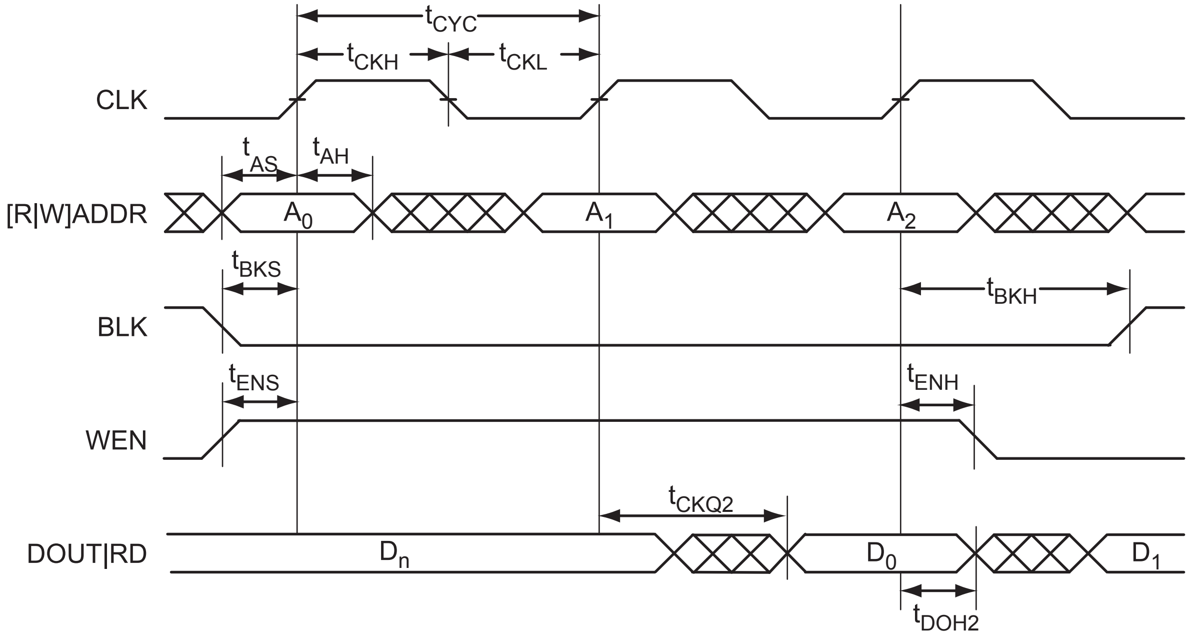


Figure 2-32 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

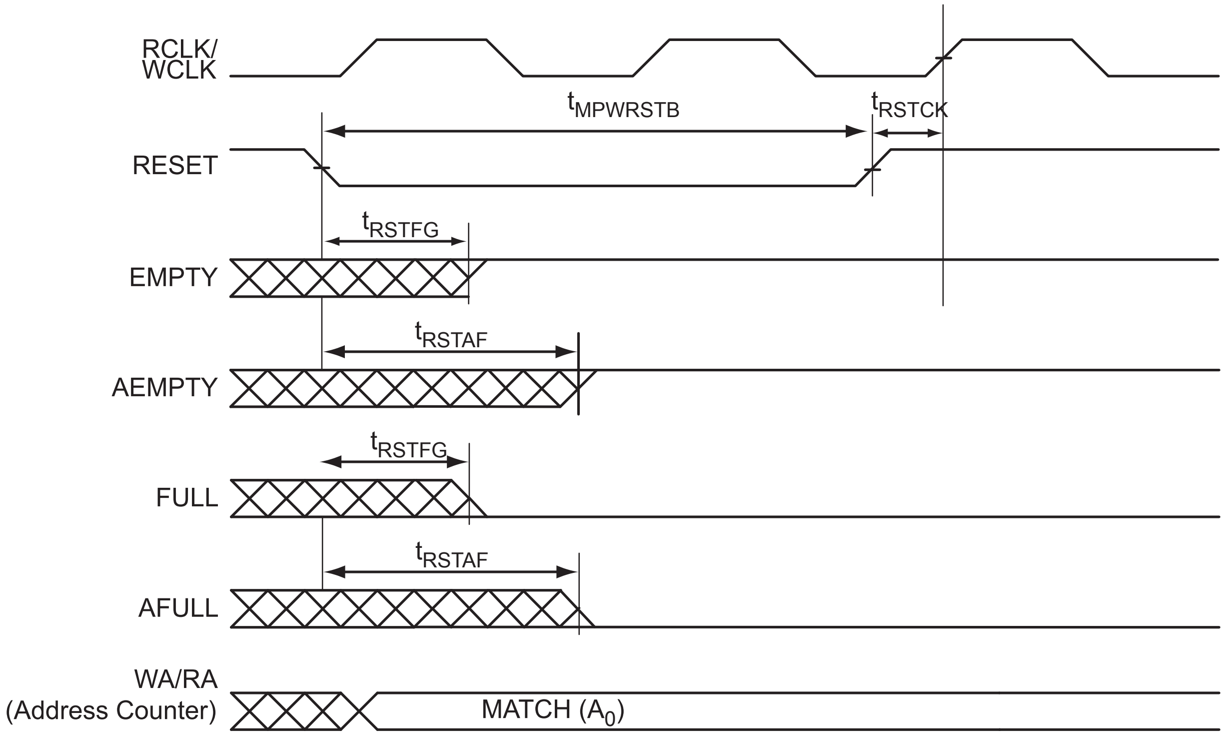


Figure 2-39 **• FIFO Reset**

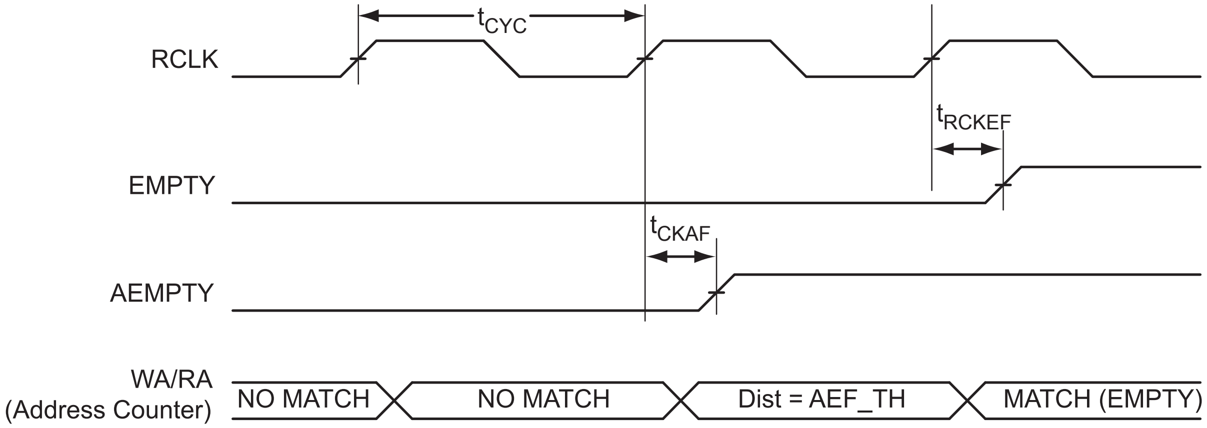


Figure 2-40 **• FIFO EMPTY Flag and AEMPTY Flag Assertion**

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-12 for more details.

Timing Characteristics

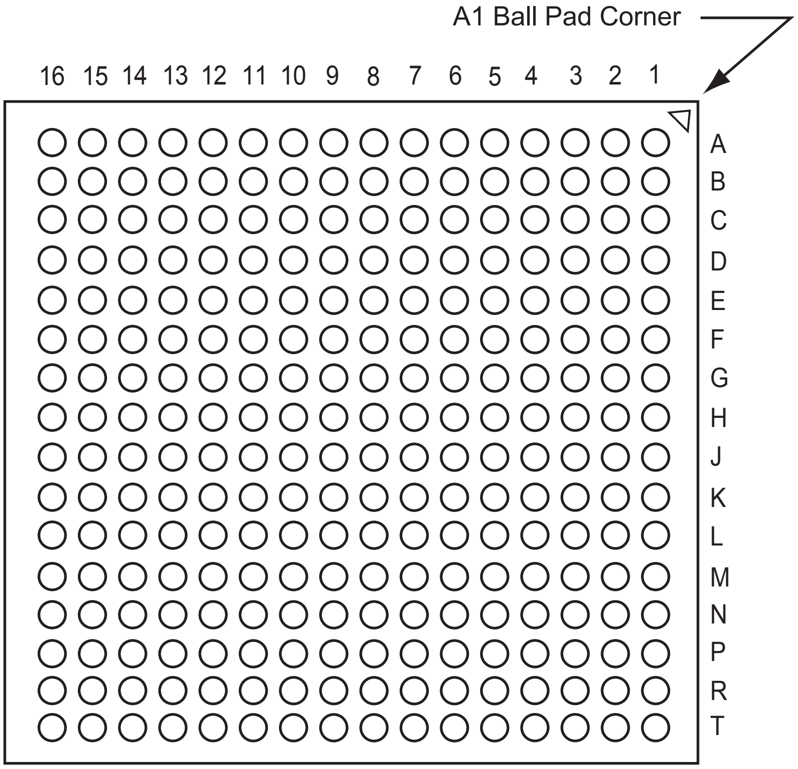
***Table 2-125* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time				ns
t_{DIHD}	Test Data Input Hold Time				ns
t_{TMSSU}	Test Mode Select Setup Time				ns
t_{TMDHD}	Test Mode Select Hold Time				ns
t_{TCK2Q}	Clock to Q (data out)				ns
t_{RSTB2Q}	Reset to Q (data out)				ns
F_{TCKMAX}	TCK Maximum Frequency	20	20	20	MHz
$t_{TRSTREM}$	ResetB Removal Time				ns
$t_{TRSTREC}$	ResetB Recovery Time				ns
$t_{TRSTMPW}$	ResetB Minimum Pulse				ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

QN132	
Pin Number	A3P125 Function
C17	IO83RSB1
C18	VCCIB1
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO55RSB0
C27	GCC0/IO52RSB0
C28	VCCIB0
C29	IO42RSB0
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

FG256



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

FG256	
Pin Number	**A3P1000 Function**
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2

FG484	
Pin Number	**A3P1000 Function**
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2

FG484	
Pin Number	**A3P1000 Function**
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1

FG484	
Pin Number	**A3P1000 Function**
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC