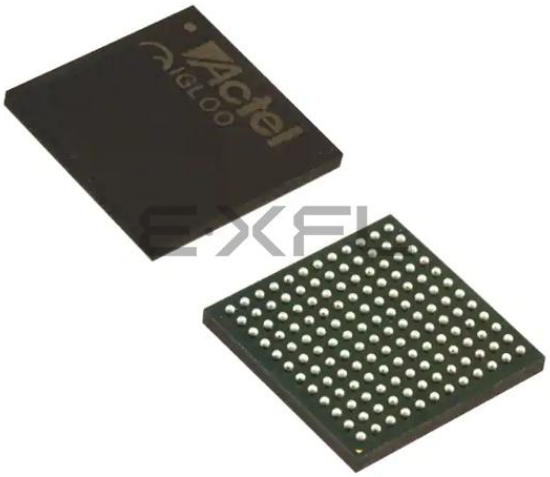

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	97
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p250-1fgg144t

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Standard Plus I/O Banks

	VMV (V)	Static Power PDC2 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.72
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	18.13

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on VMV.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI} and VMV.*

Total Static Power Consumption—P_{STAT}

$$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution—P_{CLOCK}

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Automotive ProASIC3 FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the *Automotive ProASIC3 FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-13 on page 2-12.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-13 on page 2-12.

PLL Contribution—P_{PLL}

$$P_{PLL} = PAC13 + PAC14 * F_{CLKOUT}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-12 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Table 2-16 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard I/O Banks

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2

Note: Currents are measured at 125°C junction temperature.

Table 2-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Automotive Grade 1 and Grade 2

DC I/O Standards	Automotive Grade 1 [1]		Automotive Grade 2 [2]	
	IIL	IIH	IIL	IIH
	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. *Automotive range Grade 1 (–40°C < T_J < 135°C)*
2. *Automotive range Grade 2 (–40°C < T_J < 115°C)*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-18 • Summary of AC Measuring Points

Standard	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * VCCI (RR)
	0.615 * VCCI (FF)
3.3 V PCI-X	0.285 * VCCI (RR)
	0.615 * VCCI (FF)

Timing Characteristics

Table 2-35 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	8.56	0.05	1.14	0.46	8.72	7.37	1.46	1.42	11.22	9.866	ns
	-1	0.55	7.28	0.04	0.97	0.39	7.42	6.27	1.46	1.42	9.54	8.393	ns
6 mA	STD	0.64	5.49	0.05	1.14	0.46	5.59	4.55	1.65	1.74	8.09	7.05	ns
	-1	0.55	4.67	0.04	0.97	0.39	4.75	3.87	1.65	1.74	6.88	5.997	ns
8 mA	STD	0.64	5.49	0.05	1.14	0.46	5.59	4.55	1.65	1.74	8.09	7.05	ns
	-1	0.55	4.67	0.04	0.97	0.39	4.75	3.87	1.65	1.74	6.88	5.997	ns
12 mA	STD	0.64	3.95	0.05	1.14	0.46	4.02	1.56	3.59	1.94	6.52	2.795	ns
	-1	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.797	ns
16 mA	STD	0.64	3.73	0.05	1.14	0.46	1.84	1.42	3.65	4.11	3.05	2.651	ns
	-1	0.55	3.17	0.04	0.97	0.39	1.84	1.42	3.10	3.50	3.05	2.653	ns
24 mA	STD	0.64	3.44	0.05	1.14	0.46	1.70	1.17	3.72	4.54	2.91	2.405	ns
	-1	0.55	2.92	0.04	0.97	0.39	1.70	1.17	3.16	3.86	2.91	2.407	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	11.47	0.05	1.14	0.46	11.68	9.95	1.46	1.33	14.18	12.449	ns
	-1	0.55	9.75	0.04	0.97	0.39	9.94	8.46	1.46	1.33	12.06	10.59	ns
6 mA	STD	0.64	8.13	0.05	1.14	0.46	8.28	7.03	1.65	1.65	10.79	9.526	ns
	-1	0.55	6.92	0.04	0.97	0.39	7.05	5.98	1.65	1.65	9.17	8.103	ns
8 mA	STD	0.64	8.13	0.05	1.14	0.46	8.28	7.03	1.65	1.65	10.79	9.526	ns
	-1	0.55	6.92	0.04	0.97	0.39	7.05	5.98	1.65	1.65	9.17	8.103	ns
12 mA	STD	0.64	6.24	0.05	1.14	0.46	6.36	5.45	1.77	1.85	8.86	7.946	ns
	-1	0.55	5.31	0.04	0.97	0.39	5.41	4.63	1.77	1.85	7.53	6.76	ns
16 mA	STD	0.64	5.82	0.05	1.14	0.46	5.93	5.10	1.80	1.90	8.43	7.604	ns
	-1	0.55	4.95	0.04	0.97	0.39	5.04	4.34	1.80	1.90	7.17	6.468	ns
24 mA	STD	0.64	5.42	0.05	1.14	0.46	5.52	5.08	1.83	2.10	8.02	7.581	ns
	-1	0.55	4.61	0.04	0.97	0.39	4.70	4.32	1.83	2.11	6.82	6.449	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	8.06	0.05	1.12	0.46	8.20	7.03	1.26	1.27	8.20	7.027	ns
	-1	0.55	6.85	0.04	.095	0.39	6.98	5.98	1.26	1.27	6.98	5.978	ns
6 mA	STD	0.64	5.03	0.05	1.12	0.46	5.13	4.27	1.42	1.56	5.13	4.267	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
8 mA	STD	0.64	5.03	0.05	1.12	0.46	5.13	4.27	1.42	1.56	5.13	4.267	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
12 mA	STD	0.64	3.53	0.05	1.12	0.46	1.74	1.43	3.12	3.60	1.74	1.427	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.428	ns
16 mA	STD	0.64	3.53	0.05	1.12	0.46	1.74	1.43	3.12	3.60	1.74	1.427	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.428	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	10.82	0.05	1.12	0.46	11.02	9.42	1.26	1.20	11.02	9.419	ns
	-1	0.55	9.21	0.04	0.95	0.39	9.38	8.01	1.26	1.20	9.38	8.012	ns
6 mA	STD	0.64	7.49	0.05	1.12	0.46	7.63	6.58	1.43	1.48	7.63	6.58	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.598	ns
8 mA	STD	0.64	7.49	0.05	1.12	0.46	7.63	6.58	1.43	1.48	7.63	6.58	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.598	ns
12 mA	STD	0.64	5.64	0.05	1.12	0.46	5.75	5.04	1.54	1.67	5.75	5.042	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.289	ns
16 mA	STD	0.64	5.64	0.05	1.12	0.46	5.75	5.04	1.54	1.67	5.75	5.042	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.289	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-50 • 2.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	9.37	0.05	1.40	0.45	8.47	9.37	1.43	1.21	10.89	11.79	ns
	-1	0.53	7.97	0.04	1.19	0.38	7.21	7.97	1.43	1.21	9.27	10.03	ns
6 mA	STD	0.63	5.59	0.05	1.40	0.45	5.45	5.59	1.63	1.57	7.87	8.01	ns
	-1	0.53	4.75	0.04	1.19	0.38	4.63	4.75	1.63	1.57	6.69	6.81	ns
12 mA	STD	0.63	3.85	0.05	1.40	0.45	3.92	3.71	1.77	1.80	6.34	6.13	ns
	-1	0.53	3.28	0.04	1.19	0.38	3.34	3.16	1.77	1.80	5.39	5.22	ns
16 mA	STD	0.63	3.63	0.05	1.40	0.45	1.79	1.64	3.64	3.84	2.96	2.83	ns
	-1	0.53	3.08	0.04	1.19	0.38	1.79	1.64	3.09	3.27	2.96	2.83	ns
24 mA	STD	0.63	3.34	0.05	1.40	0.45	1.65	1.31	3.72	4.32	2.82	2.50	ns
	-1	0.53	2.84	0.04	1.19	0.38	1.65	1.31	3.16	3.68	2.82	2.50	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-51 • 2.5 V LVCMOS Low Slew
Automotive-Case Conditions: TJ = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	11.73	0.05	1.40	0.45	12.14	12.33	1.43	1.16	14.55	14.75	ns
	-1	0.53	9.98	0.04	1.19	0.38	10.32	10.49	1.43	1.16	12.38	12.55	ns
6 mA	STD	0.63	7.97	0.05	1.40	0.45	8.77	8.45	1.63	1.51	11.19	10.87	ns
	-1	0.53	6.78	0.04	1.19	0.38	7.46	7.19	1.63	1.52	9.52	9.25	ns
12 mA	STD	0.63	6.68	0.05	1.40	0.45	6.81	6.40	1.77	1.74	9.23	8.82	ns
	-1	0.53	5.69	0.04	1.19	0.38	5.79	5.45	1.77	1.74	7.85	7.50	ns
16 mA	STD	0.63	6.24	0.05	1.40	0.45	6.35	5.98	1.80	1.80	8.77	8.40	ns
	-1	0.53	5.30	0.04	1.19	0.38	5.40	5.08	1.80	1.80	7.46	7.14	ns
24 mA	STD	0.63	5.96	0.05	1.40	0.45	5.95	5.96	1.84	2.03	8.37	8.38	ns
	-1	0.53	5.07	0.04	1.19	0.38	5.06	5.07	1.84	2.03	7.12	7.12	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Timing Characteristics

Table 2-57 • 1.8 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.26	0.05	1.36	0.46	10.22	13.26	1.53	0.90	12.72	15.764	ns
	-1	0.55	11.28	0.04	1.16	0.39	8.69	11.28	1.53	0.90	10.82	13.41	ns
4 mA	STD	0.64	7.73	0.05	1.36	0.46	6.55	7.73	1.78	1.54	9.05	10.232	ns
	-1	0.55	6.58	0.04	1.16	0.39	5.58	6.58	1.78	1.54	7.70	8.704	ns
6 mA	STD	0.64	4.97	0.05	1.36	0.46	4.67	4.97	1.95	1.83	7.17	7.472	ns
	-1	0.55	4.23	0.04	1.16	0.39	3.98	4.23	1.95	1.83	6.10	6.356	ns
8 mA	STD	0.64	4.39	0.05	1.36	0.46	4.39	4.39	1.99	1.91	6.89	6.888	ns
	-1	0.55	3.73	0.04	1.16	0.39	3.74	3.73	1.99	1.91	5.86	5.859	ns
12 mA	STD	0.64	3.95	0.05	1.36	0.46	1.95	1.68	4.14	4.56	3.16	2.915	ns
	-1	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.918	ns
16 mA	STD	0.64	3.95	0.05	1.36	0.46	1.95	1.68	4.14	4.56	3.16	2.915	ns
	-1	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.918	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-70 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	8.76	0.05	1.59	0.46	7.63	9.35	1.87	1.50	10.13	11.851	ns
	-1	0.55	7.45	0.04	1.35	0.39	6.49	7.95	1.87	1.50	8.62	10.081	ns
4 mA	STD	0.64	5.41	0.05	1.59	0.46	5.42	5.94	2.07	1.84	7.92	8.442	ns
	-1	0.55	4.60	0.04	1.35	0.39	4.61	5.05	2.07	1.85	6.74	7.181	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-71 • 1.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.51	0.05	1.45	0.46	14.32	14.29	1.88	1.43	16.82	16.794	ns
	-1	0.55	11.49	0.04	1.23	0.39	12.18	12.16	1.88	1.43	14.31	14.286	ns
4 mA	STD	0.64	10.38	0.05	1.45	0.46	11.40	10.67	2.07	1.77	13.90	13.175	ns
	-1	0.55	8.83	0.04	1.23	0.39	9.70	9.08	2.07	1.77	11.82	11.207	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-72 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	9.05	0.05	1.56	0.45	7.38	9.05	1.81	1.45	9.80	11.47	ns
	-1	0.53	7.70	0.04	1.32	0.38	6.28	7.70	1.81	1.45	8.34	9.75	ns
4 mA	STD	0.63	5.75	0.05	1.56	0.45	5.25	5.75	2.00	1.78	7.67	8.17	ns
	-1	0.53	4.89	0.04	1.32	0.38	4.46	4.89	2.00	1.78	6.52	6.95	ns
6 mA	STD	0.63	5.05	0.05	1.56	0.45	4.92	5.05	2.04	1.87	7.34	7.47	ns
	-1	0.53	4.29	0.04	1.32	0.38	4.19	4.29	2.04	1.87	6.24	6.35	ns
8 mA	STD	0.63	4.41	0.05	1.56	0.45	2.18	1.91	4.27	4.55	3.35	3.11	ns
	-1	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns
12 mA	STD	0.63	4.41	0.05	1.56	0.45	2.18	1.91	4.27	4.55	3.35	3.11	ns
	-1	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-13. The input and output buffer delays are available in the LVDS section in Table 2-84 on page 2-50.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

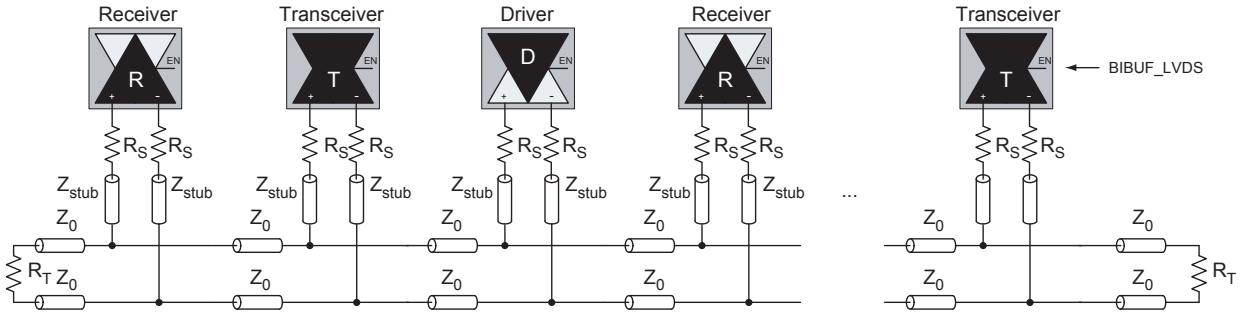


Figure 2-13 • **B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-14 on page 2-52. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

Table 2-100 • Input DDR Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.33	0.38	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.46	0.54	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.34	0.40	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.55	0.65	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.68	0.80	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.27	0.31	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.37	0.43	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

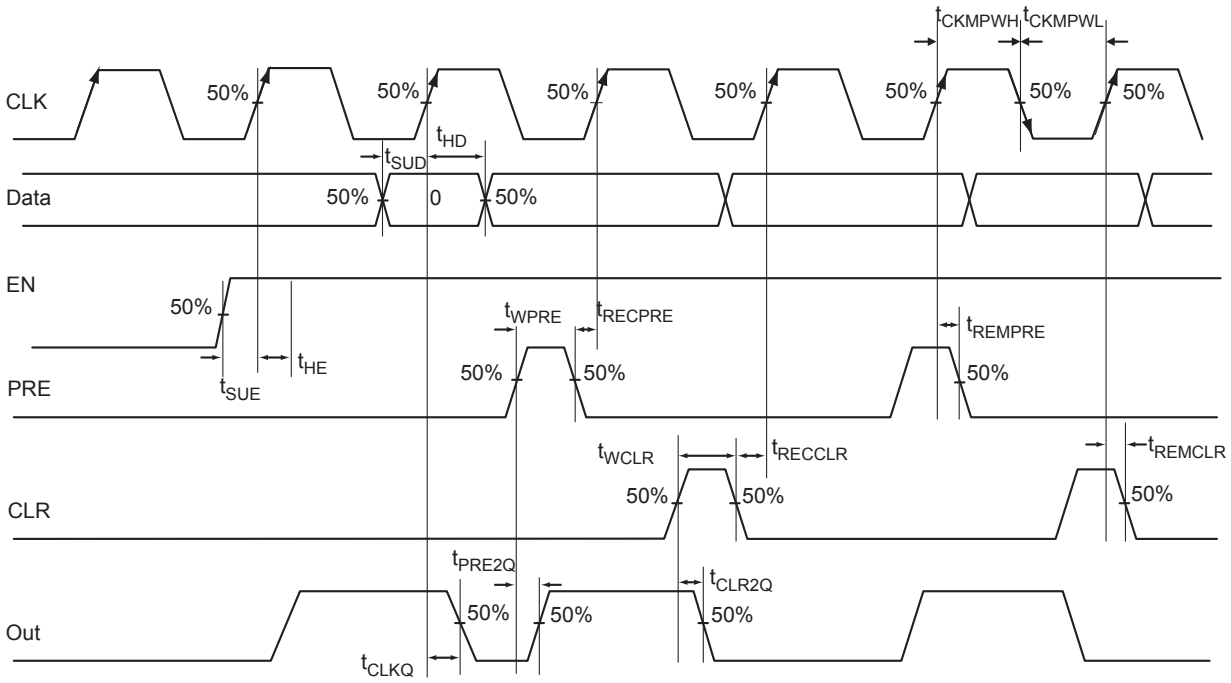


Figure 2-27 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-106 • **Register Delays**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.67	0.79	ns
t_{SUD}	Data Setup Time for the Core Register	0.52	0.61	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.55	0.65	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.49	0.57	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.49	0.57	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.27	0.32	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.27	0.32	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.41	0.48	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

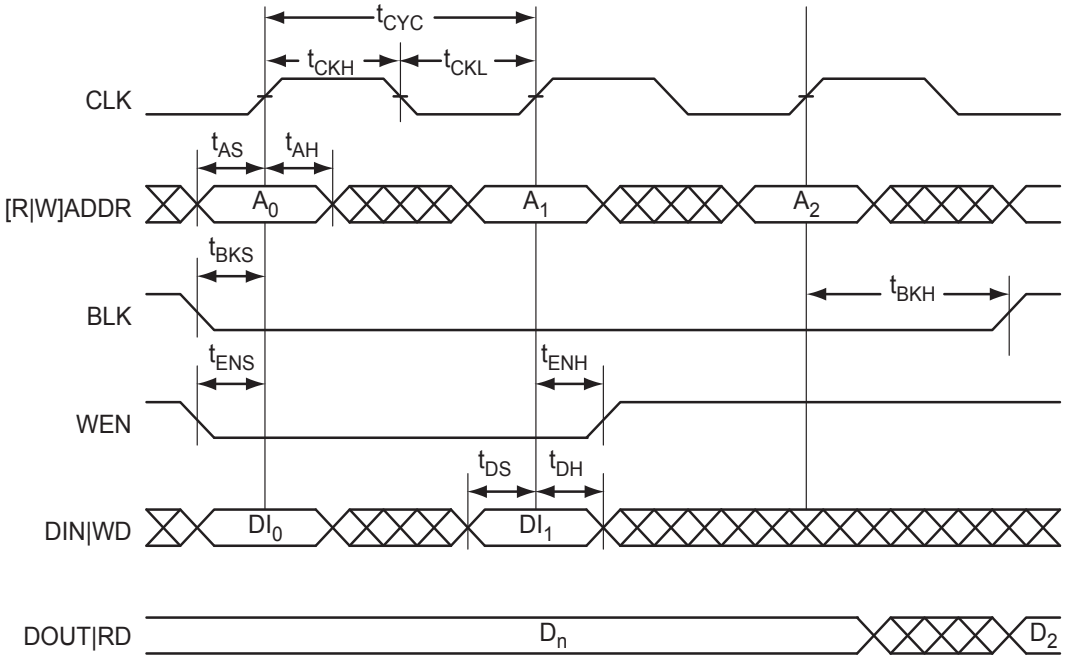


Figure 2-33 • **RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

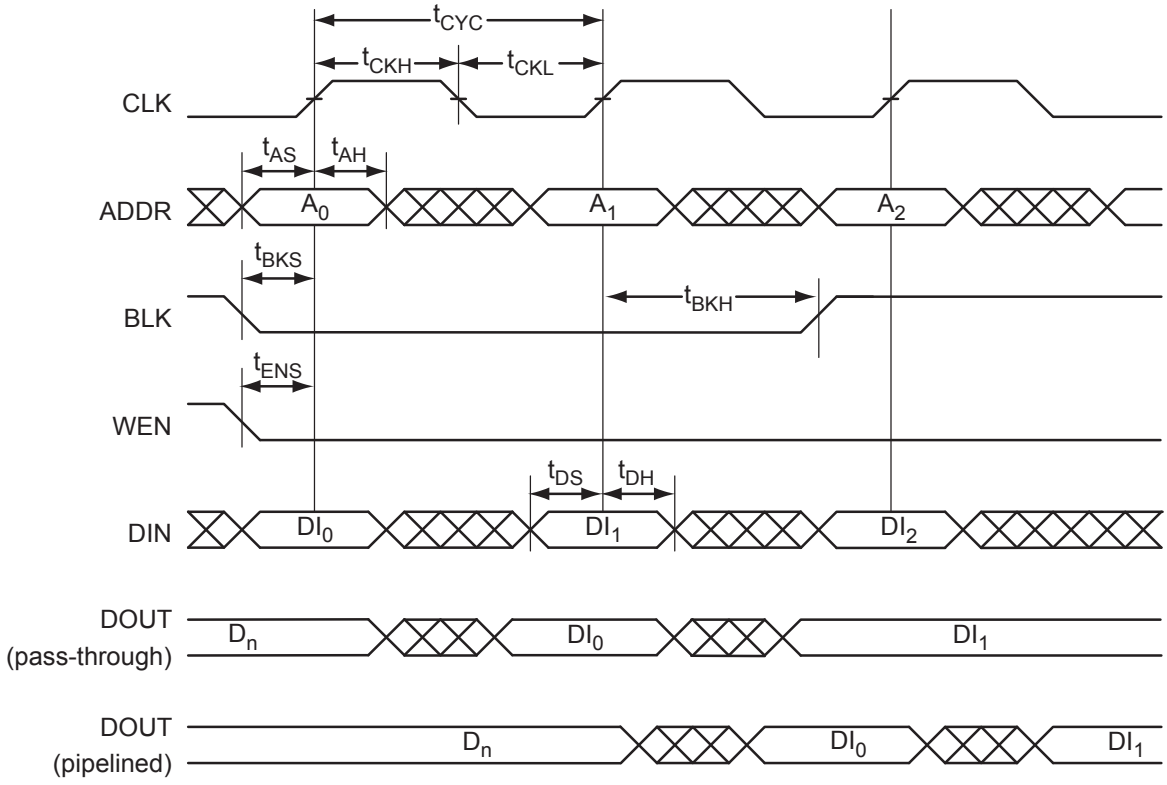


Figure 2-34 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

Table 2-122 • FIFO
Worst-Case Automotive Conditions: T_J = 115°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.93	1.64	ns
t_{ENH}	REN, WEN Hold Time	0.03	0.02	ns
t_{BKS}	BLK Setup Time	0.27	0.32	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.26	0.22	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	3.30	2.81	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.25	1.07	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.41	2.05	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.29	1.95	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	8.68	7.38	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.37	2.02	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	8.59	7.30	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.29	1.10	ns
	RESET Low to Data Out Low on RD (pipelined)	1.29	1.10	ns
$t_{REMRSTB}$	RESET Removal	0.40	0.34	ns
$t_{RECRSTB}$	RESET Recovery	2.10	1.79	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.30	0.25	ns
t_{CYC}	Clock Cycle Time	4.53	3.85	ns
F_{MAX}	Maximum Frequency for FIFO	221	260	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

3 – Pin Descriptions and Packaging

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to four I/O banks on Automotive ProASIC3 devices, plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *Automotive ProASIC3 FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on Automotive ProASIC3 devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on Automotive ProASIC3 devices.

VJTAG **JTAG Supply Voltage**

Automotive ProASIC3 devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is

JTAG Pins

Automotive ProASIC3 devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Actel recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-1 for more information.

***Table 3-1* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

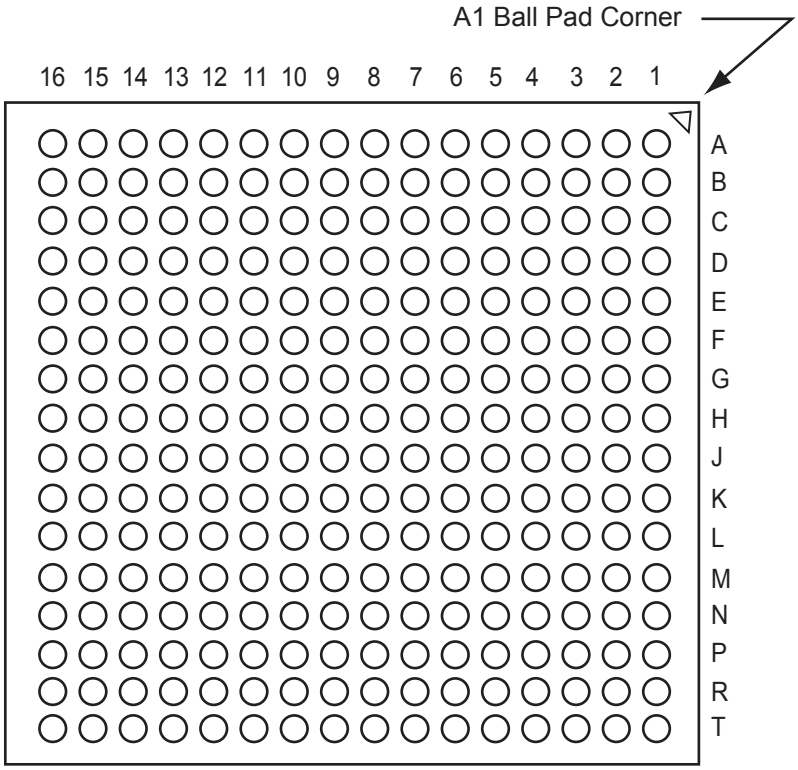
TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-1 and must satisfy the parallel resistance value requirement. The values in Table 3-1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Actel recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

FG256



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

FG256	
Pin Number	A3P250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117UDB3
B2	GAA2/IO118UDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117VDB3
C2	IO118VDB3
C3	NC
C4	NC

FG256	
Pin Number	A3P250 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114VDB3
D2	IO114UDB3
D3	GAC2/IO116UDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116VDB3
E4	IO115UDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO19RSB0

FG256	
Pin Number	A3P250 Function
E9	IO24RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115VDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

FG256	
Pin Number	A3P250 Function
G13	GCC1/IO48PPB1
G14	IO47NPB1
G15	IO54PDB1
G16	IO54NDB1
H1	GFB0/IO109NPB3
H2	GFA0/IO108NDB3
H3	GFB1/IO109PPB3
H4	VCOMPLF
H5	GFC0/IO110NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO48NPB1
H13	GCB1/IO49PPB1
H14	GCA0/IO50NPB1
H15	NC
H16	GCB0/IO49NPB1
J1	GFA2/IO107PPB3
J2	GFA1/IO108PDB3
J3	VCCPLF
J4	IO106NDB3
J5	GFB2/IO106PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO52PPB1
J13	GCA1/IO50PPB1
J14	GCC2/IO53PPB1
J15	NC
J16	GCA2/IO51PDB1

FG256	
Pin Number	A3P250 Function
K1	GFC2/IO105PDB3
K2	IO107NPB3
K3	IO104PPB3
K4	NC
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO52NPB1
K14	IO55RSB1
K15	IO53NPB1
K16	IO51NDB1
L1	IO105NDB3
L2	IO104NPB3
L3	NC
L4	IO102RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO59VPB1
L14	IO57VDB1
L15	IO57UDB1
L16	IO56PDB1
M1	IO103PDB3
M2	NC
M3	IO101NPB3
M4	GEC0/IO100NPB3

FG256	
Pin Number	A3P250 Function
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	NC
M9	IO74RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	NC
M14	GDB1/IO59UPB1
M15	GDC1/IO58UDB1
M16	IO56NDB1
N1	IO103NDB3
N2	IO101PPB3
N3	GEC1/IO100PPB3
N4	NC
N5	GNDQ
N6	GEA2/IO97RSB2
N7	IO86RSB2
N8	IO82RSB2
N9	IO75RSB2
N10	IO69RSB2
N11	IO64RSB2
N12	GNDQ
N13	NC
N14	VJTAG
N15	GDC0/IO58VDB1
N16	GDA1/IO60UDB1
P1	GEB1/IO99PDB3
P2	GEB0/IO99NDB3
P3	NC
P4	NC
P5	IO92RSB2
P6	IO89RSB2
P7	IO85RSB2
P8	IO81RSB2

FG256	
Pin Number	**A3P1000 Function**
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2

FG256	
Pin Number	**A3P1000 Function**
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND