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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	97
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p250-fg144t

Temperature Grade Offerings

Package	A3P060	A3P125	A3P250	A3P1000
VQ100	C, I, T	C, I, T	C, I, T	–
FG144	C, I, T	C, I, T	C, I, T	C, I, T
FG256	–	–	C, I, T	C, I, T
FG484	–	–	–	C, I, T
QNG132	–	C, I, T	C, I, T	–

Notes:
1. *C = Commercial temperature range: 0°C to 70°C*
2. *I = Industrial temperature range: –40°C to 85°C*
3. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
4. *Specifications for Commercial and Industrial grade devices can be found in the ProASIC3 Flash Family FPGAs datasheet.*

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
T (Grade 1 and Grade 2), Commercial, Industrial	3	3

Notes:
1. *T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100*
   Grade 2 = 105°C T_A and 115°C T_J
   Grade 1 = 125°C T_A and 135°C T_J
2. *Specifications for Commercial and Industrial grade devices can be found in the ProASIC3 Flash Family FPGAs datasheet.*

Contact your local Microsemi SoC Products Group representative for device availability:
http://www.microsemi.com/soc/contact/default.aspx.

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Calculating Power Dissipation

Quiescent Supply Current

Table 2-6 • Quiescent Supply Current Characteristics

	A3P060	A3P125	A3P250	A3P1000
Typical (25°C)	2 mA	2 mA	3 mA	8 mA
Maximum (Automotive Grade 1) – 135°C	53 mA	53 mA	106 mA	265 mA
Maximum (Automotive Grade 2) – 115°C	26 mA	26 mA	53 mA	131 mA

Note: IDD Includes VCC, VPUMP, VCCI, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-7 and Table 2-10 on page 2-8.

Power per I/O Pin

Table 2-7 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Advanced I/O Banks

	VMV (V)	Static Power PDC2 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.69
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-32 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-33 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	109	103	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-43 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		V_{OL}	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-44 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	VIL		VIH		V_{OL}	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

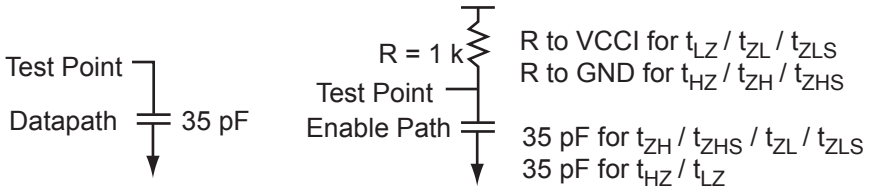


Figure 2-8 • AC Loading

Table 2-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	35

*Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.*

Table 2-52 • 2.5 V LVCMOS High Slew
Automotive-Case Conditions: TJ = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	8.95	0.05	1.40	0.45	8.01	8.95	1.20	1.09	10.43	11.37	ns
	-1	0.53	7.62	0.04	1.19	0.38	6.82	7.62	1.20	1.09	8.87	9.68	ns
6 mA	STD	0.63	5.25	0.05	1.40	0.45	5.03	5.25	1.38	1.42	7.44	7.67	ns
	-1	0.53	4.47	0.04	1.19	0.38	4.27	4.47	1.38	1.42	6.33	6.52	ns
12 mA	STD	0.63	3.47	0.05	1.40	0.45	3.53	3.40	1.51	1.63	5.95	5.82	ns
	-1	0.53	2.95	0.04	1.19	0.38	3.01	2.89	1.51	1.63	5.06	4.95	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-53 • 2.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	11.73	0.05	1.40	0.45	11.51	11.73	1.21	1.04	13.93	14.15	ns
	-1	0.53	9.98	0.04	1.19	0.38	9.79	9.98	1.21	1.04	11.85	12.03	ns
6 mA	STD	0.63	7.97	0.05	1.40	0.45	8.12	7.96	1.38	1.37	10.54	10.38	ns
	-1	0.53	6.78	0.04	1.19	0.38	6.91	6.77	1.39	1.37	8.96	8.83	ns
12 mA	STD	0.63	6.09	0.05	1.40	0.45	6.20	5.96	1.51	1.58	8.62	8.38	ns
	-1	0.53	5.18	0.04	1.19	0.38	5.28	5.07	1.51	1.58	7.33	7.12	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-66 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	0	0	10	10
4 mA	–0.3	0.30 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	0	0	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

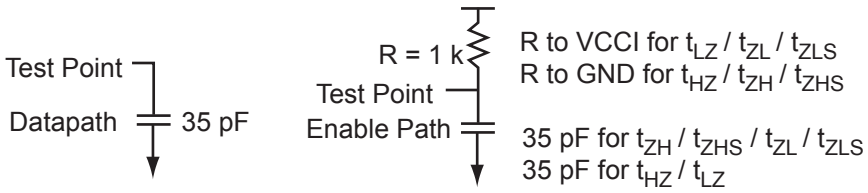


Figure 2-10 • AC Loading

Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	35

*Note: *Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.*

Table 2-97 • Output Enable Register Propagation Delays
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.53	0.62	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.37	0.44	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.52	0.61	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.79	0.93	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.79	0.93	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.31	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.31	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-103 • Output DDR Propagation Delays
Commercial-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.84	0.98	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.45	0.53	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.45	0.53	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.96	1.12	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.27	0.31	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.37	0.43	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

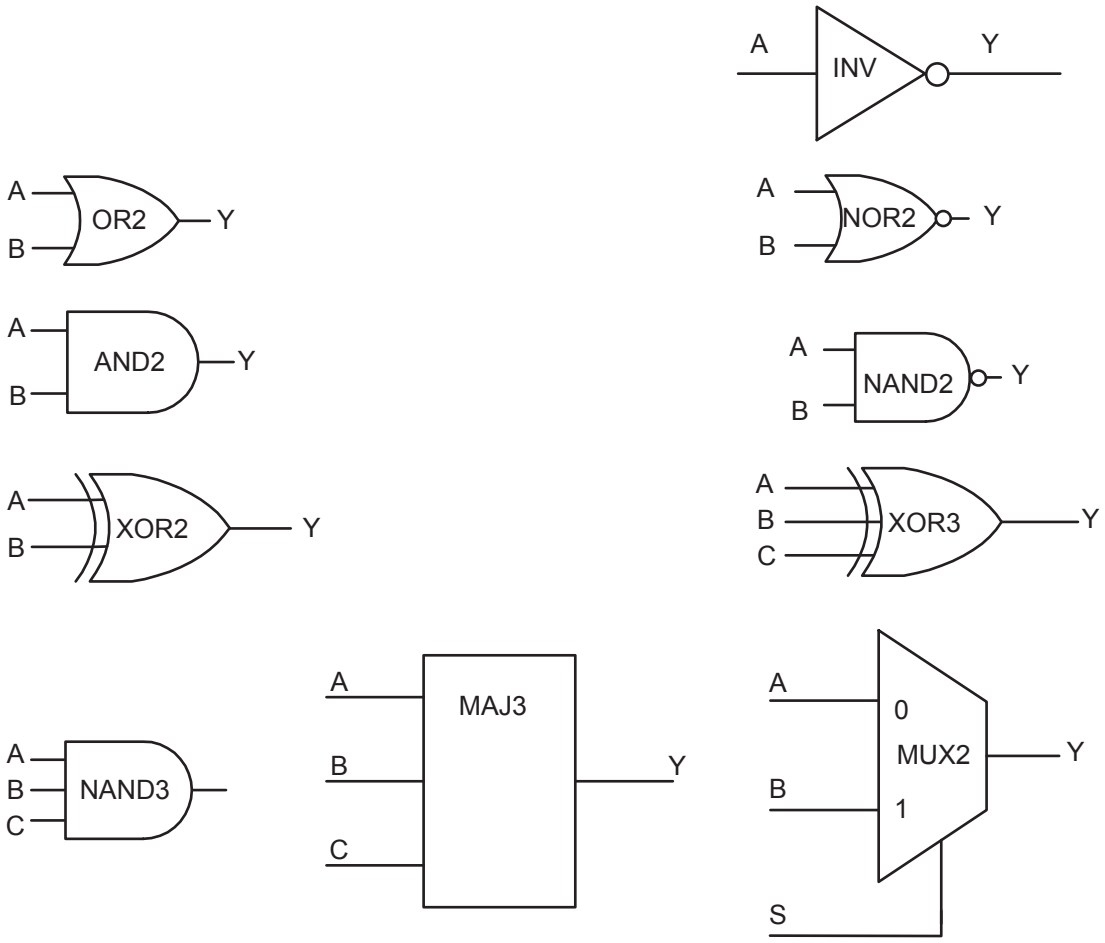


Figure 2-24 • **Sample of Combinatorial Cells**

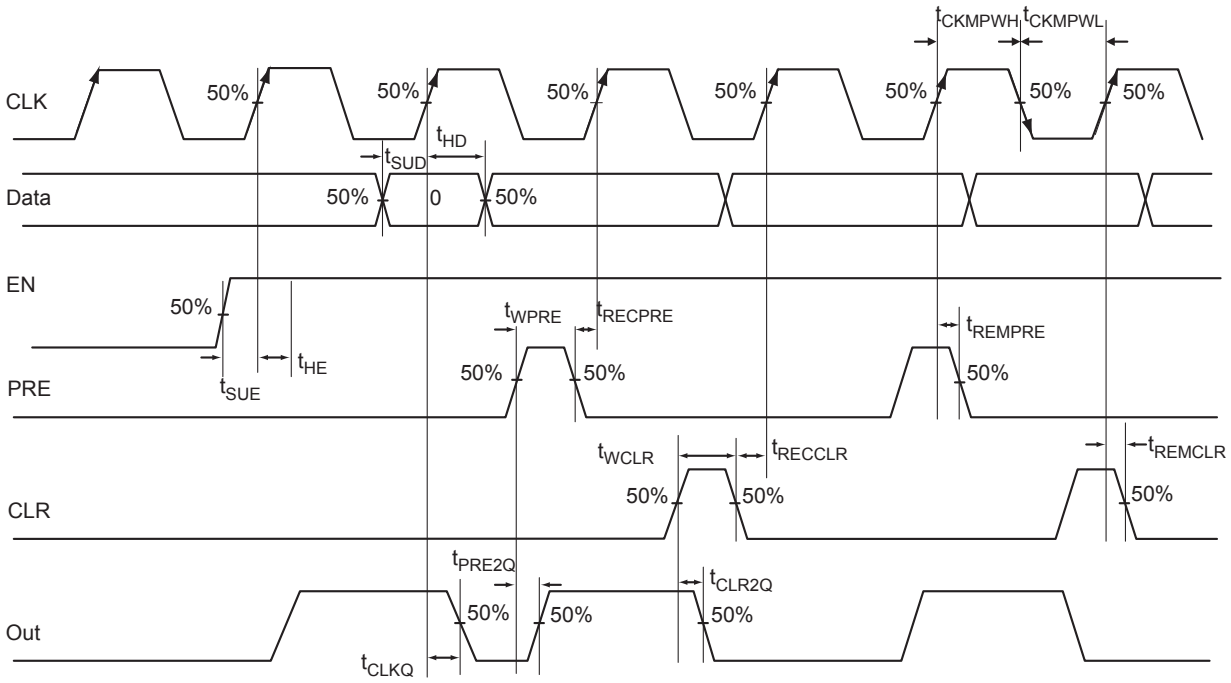


Figure 2-27 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-106 • **Register Delays**
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.67	0.79	ns
t_{SUD}	Data Setup Time for the Core Register	0.52	0.61	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.55	0.65	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.49	0.57	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.49	0.57	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.27	0.32	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.27	0.32	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.41	0.48	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

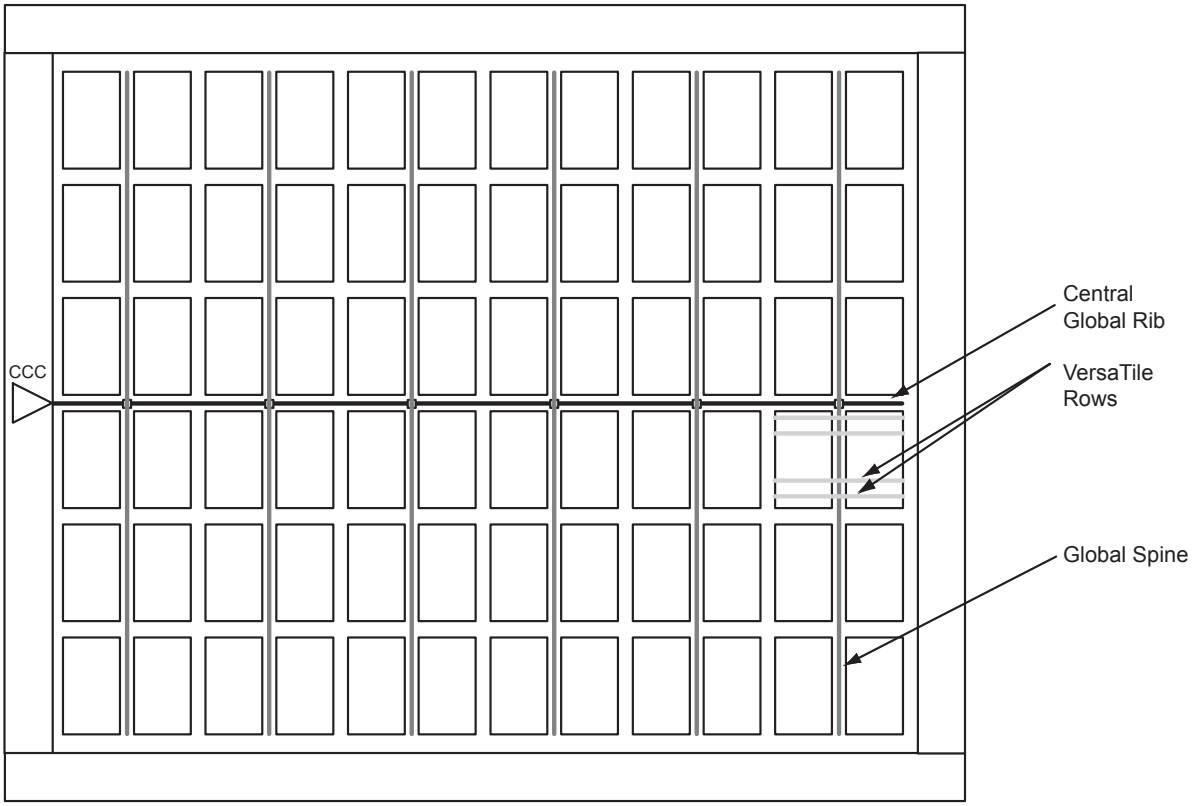


Figure 2-28 • **Example of Global Tree Use in an A3P250 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-80. Table 2-114 on page 2-79 to Table 2-125 on page 2-97 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 2-108 • A3P060 Global Resource
Commercial-Case Conditions: T_J = 135°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.87	1.16	1.02	1.37	ns
t_{RCKH}	Input High Delay for Global Clock	0.86	1.20	1.01	1.42	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35		0.41	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-109 • A3P060 Global Resource
Commercial-Case Conditions: T_J = 115°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.85	1.13	1.00	1.33	ns
t_{RCKH}	Input High Delay for Global Clock	0.84	1.18	0.99	1.38	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.34		0.40	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-112 • A3P250 Global Resource
Commercial-Case Conditions: T_J = 135°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.96	1.25	1.13	1.47	ns
t_{RCKH}	Input High Delay for Global Clock	0.94	1.28	1.10	1.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35		0.41	ns

Notes:

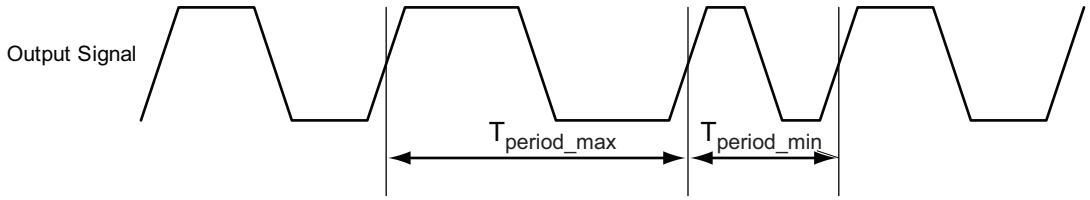
1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-113 • A3P250 Global Resource
Commercial-Case Conditions: T_J = 115°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.94	1.22	1.10	1.44	ns
t_{RCKH}	Input High Delay for Global Clock	0.92	1.25	1.08	1.47	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.80		0.94		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.98		1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.34		0.40	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-29 • **Peak-to-Peak Jitter Definition**

Timing Characteristics

Table 2-117 • RAM4K9
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.36	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN, WEN Setup Time	0.17	0.20	ns
t_{ENH}	REN, WEN Hold Time	0.12	0.14	ns
t_{BKS}	BLK Setup Time	0.28	0.33	ns
t_{BKH}	BLK Hold Time	0.02	0.03	ns
t_{DS}	Input Data (DIN) Setup Time	0.22	0.26	ns
t_{DH}	Input Data (DIN) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DOUT (output retained, WMODE = 0)	2.17	2.55	ns
	Clock High to New Data Valid on DOUT (flow-through, WMODE = 1)	2.86	3.37	ns
t_{CKQ2}	Clock High to New Data Valid on DOUT (pipelined)	1.09	1.28	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.28	0.33	ns
t_{C2CWWH} [1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.26	0.30	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.38	0.45	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.42	0.49	ns
t_{RSTBQ}	RESET Low to Data Out Low on DO (flow-through)	1.12	1.32	ns
	RESET Low to Data Out Low on DO (pipelined)	1.12	1.32	ns
$t_{REMRSTB}$	RESET Removal	0.35	0.41	ns
$t_{RECRSTB}$	RESET Recovery	1.82	2.14	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.26	0.30	ns
t_{CYC}	Clock Cycle Time	3.93	4.62	ns
F_{MAX}	Maximum Frequency	255	217	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

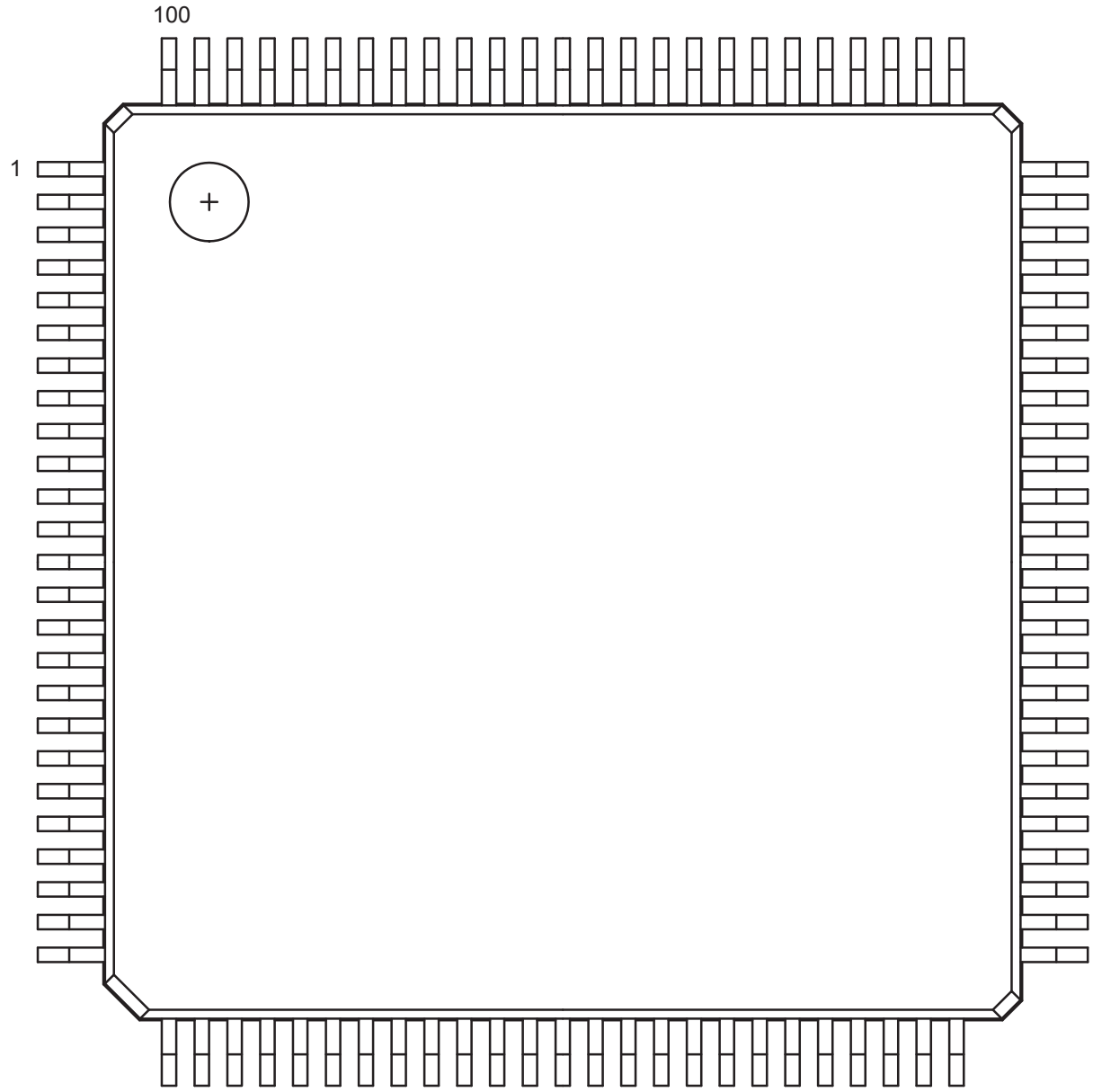
Table 2-122 • FIFO
Worst-Case Automotive Conditions: T_J = 115°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.93	1.64	ns
t_{ENH}	REN, WEN Hold Time	0.03	0.02	ns
t_{BKS}	BLK Setup Time	0.27	0.32	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.26	0.22	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	3.30	2.81	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.25	1.07	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.41	2.05	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.29	1.95	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	8.68	7.38	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.37	2.02	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	8.59	7.30	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.29	1.10	ns
	RESET Low to Data Out Low on RD (pipelined)	1.29	1.10	ns
$t_{REMRSTB}$	RESET Removal	0.40	0.34	ns
$t_{RECRSTB}$	RESET Recovery	2.10	1.79	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.30	0.25	ns
t_{CYC}	Clock Cycle Time	4.53	3.85	ns
F_{MAX}	Maximum Frequency for FIFO	221	260	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

4 – Package Pin Assignments

VQ100

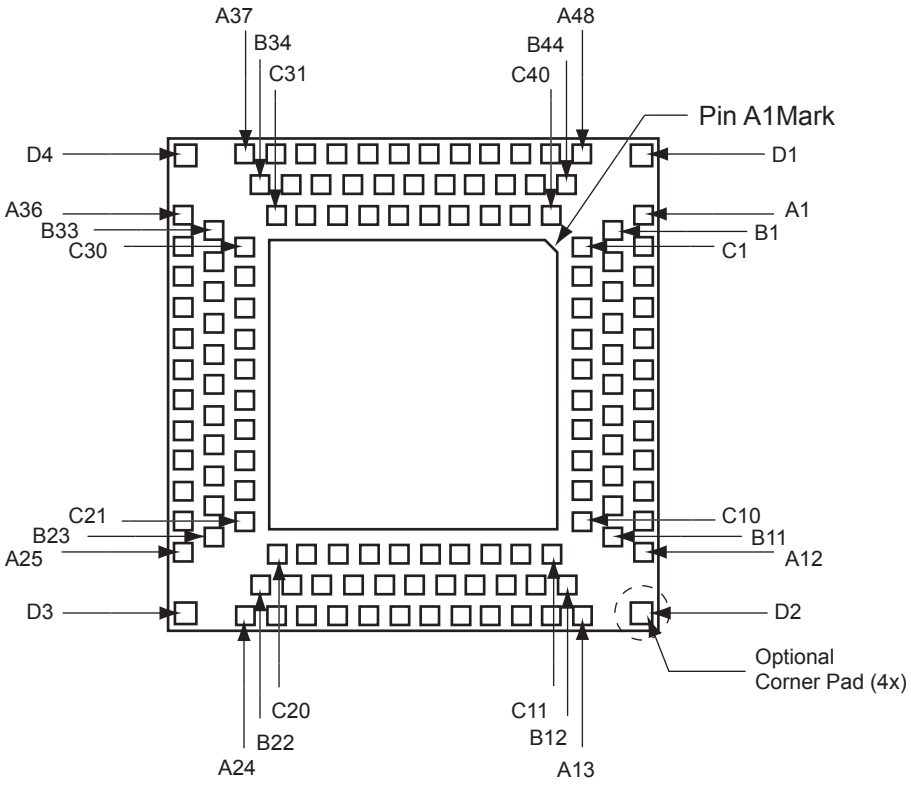


Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

QN132



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

FG144	
Pin Number	A3P060 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO04RSB0
A4	GAB1/IO05RSB0
A5	IO08RSB0
A6	GND
A7	IO11RSB0
A8	VCC
A9	IO16RSB0
A10	GBA0/IO23RSB0
A11	GBA1/IO24RSB0
A12	GNDQ
B1	GAB2/IO53RSB1
B2	GND
B3	GAA0/IO02RSB0
B4	GAA1/IO03RSB0
B5	IO00RSB0
B6	IO10RSB0
B7	IO12RSB0
B8	IO14RSB0
B9	GBB0/IO21RSB0
B10	GBB1/IO22RSB0
B11	GND
B12	VMV0
C1	IO95RSB1
C2	GFA2/IO83RSB1
C3	GAC2/IO94RSB1
C4	VCC
C5	IO01RSB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO17RSB0
C10	GBA2/IO25RSB0
C11	IO26RSB0
C12	GBC2/IO29RSB0

FG144	
Pin Number	A3P060 Function
D1	IO91RSB1
D2	IO92RSB1
D3	IO93RSB1
D4	GAA2/IO51RSB1
D5	GAC0/IO06RSB0
D6	GAC1/IO07RSB0
D7	GBC0/IO19RSB0
D8	GBC1/IO20RSB0
D9	GBB2/IO27RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	GCB1/IO37RSB0
E1	VCC
E2	GFC0/IO88RSB1
E3	GFC1/IO89RSB1
E4	VCCIB1
E5	IO52RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO35RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO40RSB0
E12	IO30RSB0
F1	GFB0/IO86RSB1
F2	VCOMPLF
F3	GFB1/IO87RSB1
F4	IO90RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO36RSB0
F9	GCB0/IO38RSB0
F10	GND
F11	GCA1/IO39RSB0
F12	GCA2/IO41RSB0

FG144	
Pin Number	A3P060 Function
G1	GFA1/IO84RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO85RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO45RSB0
G9	IO32RSB0
G10	GCC2/IO43RSB0
G11	IO31RSB0
G12	GCB2/IO42RSB0
H1	VCC
H2	GFB2/IO82RSB1
H3	GFC2/IO81RSB1
H4	GEC1/IO77RSB1
H5	VCC
H6	IO34RSB0
H7	IO44RSB0
H8	GDB2/IO55RSB1
H9	GDC0/IO46RSB0
H10	VCCIB0
H11	IO33RSB0
H12	VCC
J1	GEB1/IO75RSB1
J2	IO78RSB1
J3	VCCIB1
J4	GEC0/IO76RSB1
J5	IO79RSB1
J6	IO80RSB1
J7	VCC
J8	TCK
J9	GDA2/IO54RSB1
J10	TDO
J11	GDA1/IO49RSB0
J12	GDB1/IO47RSB0