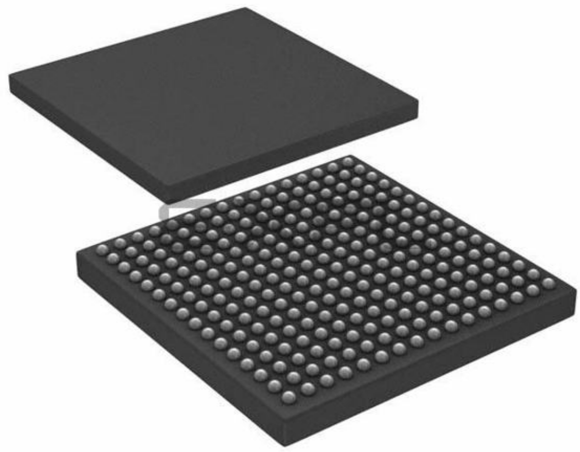

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	157
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p250-fg256t

Advanced Architecture

The proprietary Automotive ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The Automotive ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM memory
- Extensive CCCs and PLLs
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the Automotive ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

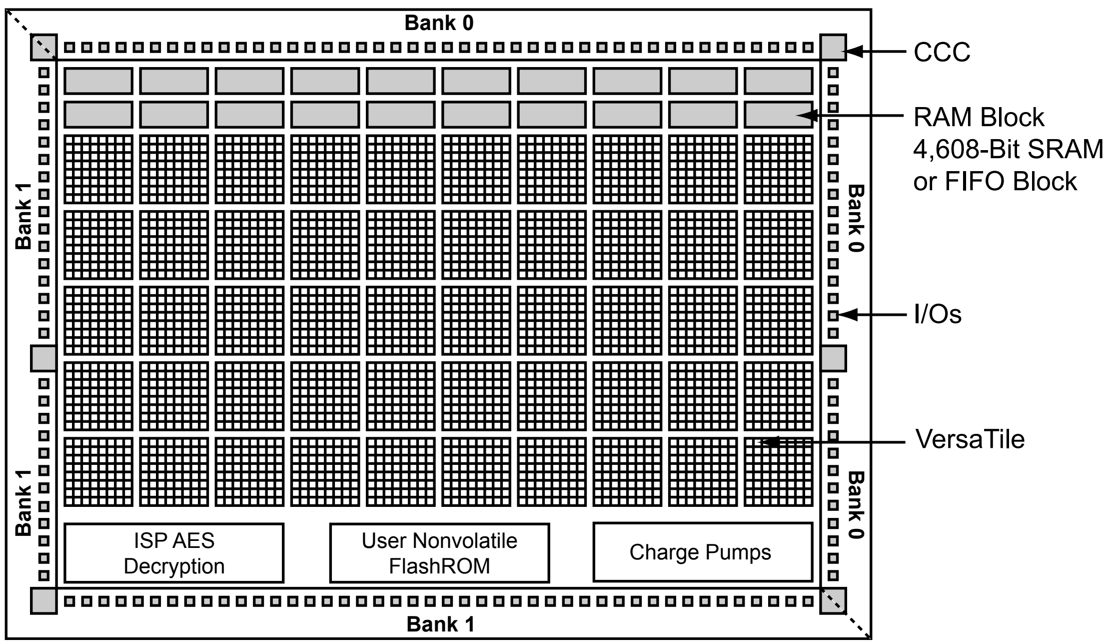


Figure 1-1 • **Automotive ProASIC3 Device Architecture Overview with Two I/O Banks (A3P060 and A3P125)**

Table 2-3 • Overshoot and Undershoot Limits (as measured on quiet I/Os)

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle	Maximum Overshoot/ Undershoot (115°C)	Maximum Overshoot/ Undershoot (135°C)
2.7 V or less	10%	0.81 V	0.72 V
	5%	0.90 V	0.82 V
3 V	10%	0.80 V	0.72 V
	5%	0.90 V	0.81 V
3.3 V	10%	0.79 V	0.69 V
	5%	0.88 V	0.79 V
3.6 V	10%	N/A	N/A
	5%	N/A	N/A

Notes:

1. *The duration is allowed at one out of six clock cycles (estimated SSO density over cycles). If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
2. *This table refers only to overshoot/undershoot limits for simultaneously switching I/Os and does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-2 on page 2-4.

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-2 on page 2-4).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI T**rip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC **Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

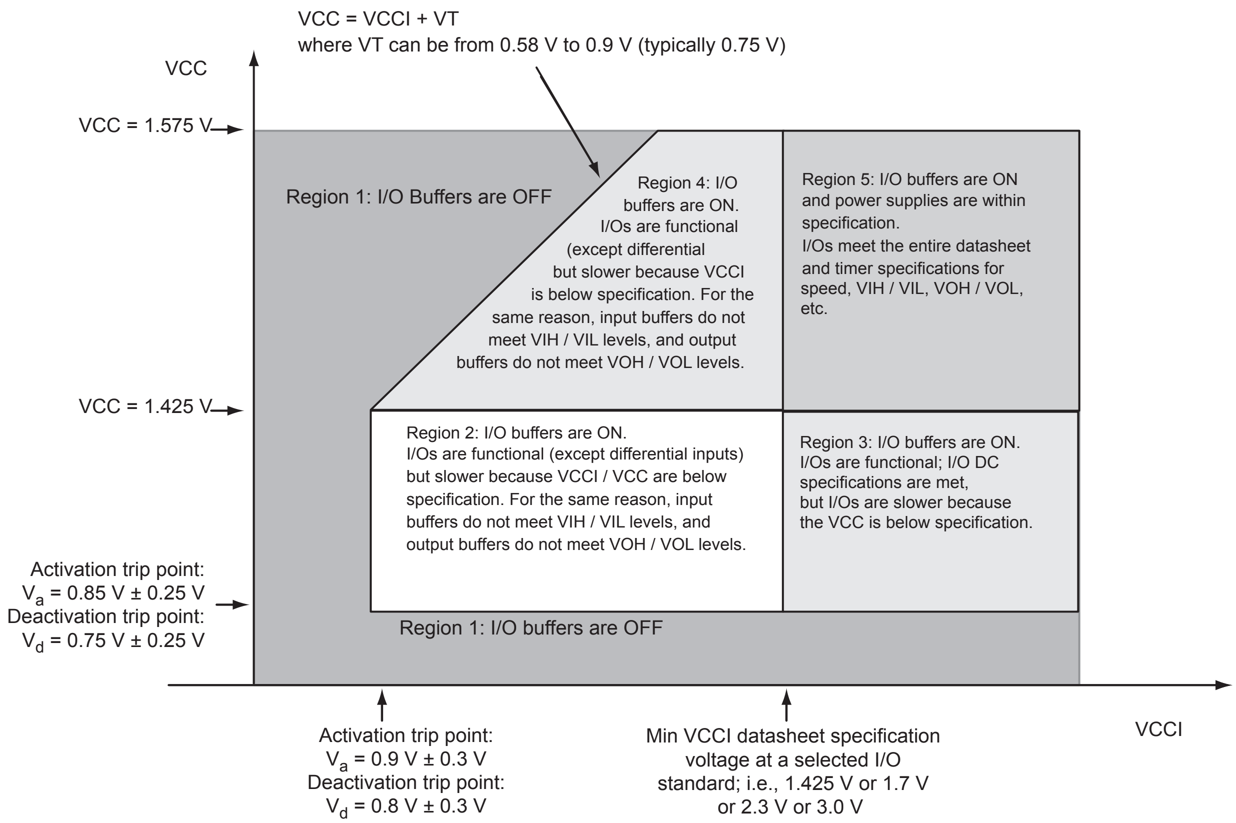


Figure 2-2 • **I/O State as a Function of VCCI and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

T_J = Junction Temperature = $\Delta T + T_A$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-4 on page 2-5.

P = Power dissipation

Total Static Power Consumption—P_{STAT}

$P_{STAT} = PDC1 + N_{INPUTS} * PDC2 + N_{OUTPUTS} * PDC3$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Automotive ProASIC3 FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the *Automotive ProASIC3 FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

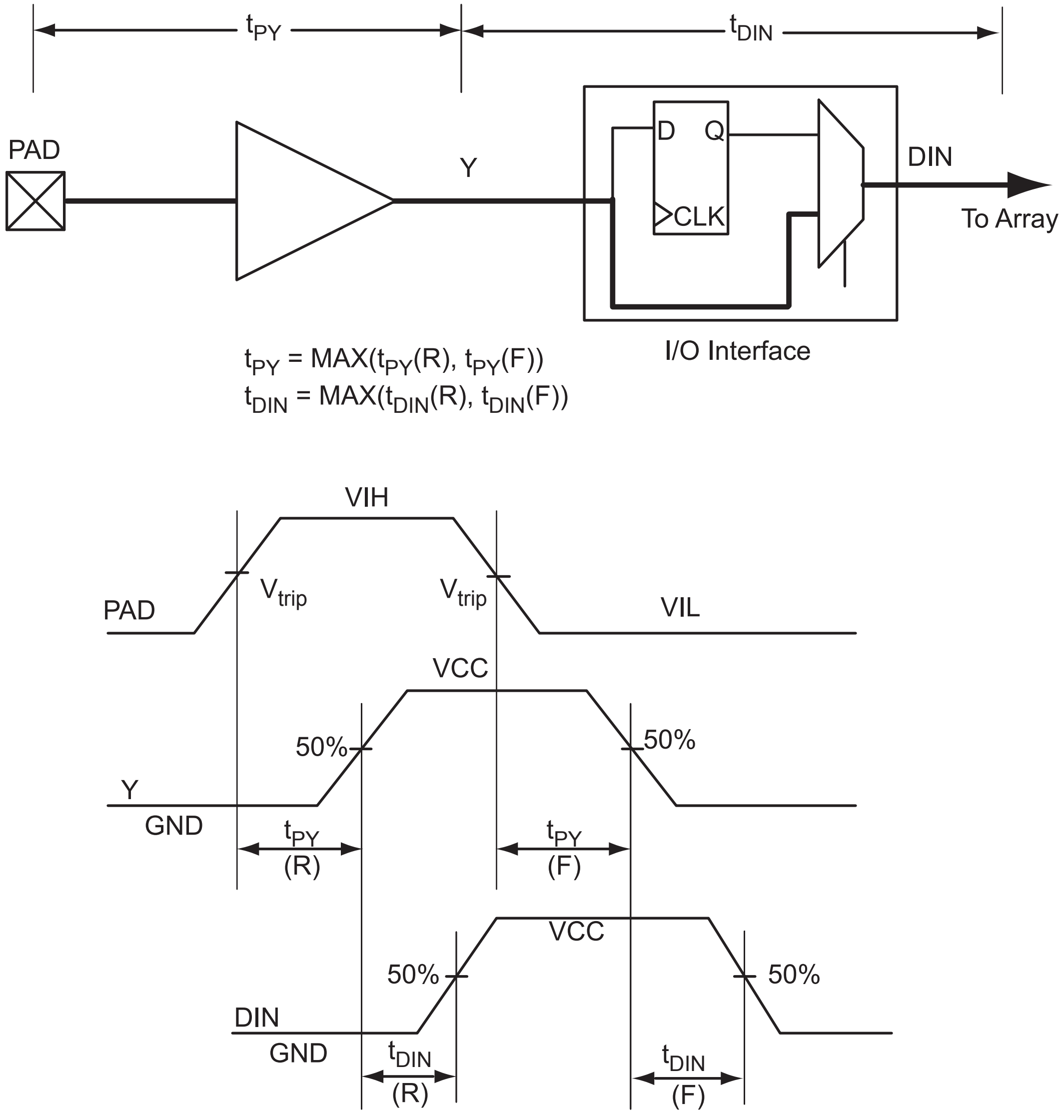


Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

Table 2-48 • 2.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.26	0.05	1.45	0.46	8.28	9.26	1.24	1.12	10.78	11.756	ns
	-1	0.55	7.87	0.04	1.23	0.39	7.05	7.87	1.24	1.13	9.17	10	ns
6 mA	STD	0.64	5.43	0.05	1.45	0.46	5.19	5.43	1.43	1.47	7.69	7.926	ns
	-1	0.55	4.62	0.04	1.23	0.39	4.42	4.62	1.43	1.47	6.55	6.743	ns
12 mA	STD	0.64	3.59	0.05	1.45	0.46	3.65	3.51	1.56	1.69	6.15	6.012	ns
	-1	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.114	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-49 • 2.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	12.12	0.05	1.45	0.46	11.89	12.12	1.25	1.08	14.39	14.622	ns
	-1	0.55	10.31	0.04	1.23	0.39	10.12	10.31	1.25	1.08	12.24	12.438	ns
6 mA	STD	0.64	8.24	0.05	1.45	0.46	8.39	8.23	1.43	1.42	10.89	10.73	ns
	-1	0.55	7.01	0.04	1.23	0.39	7.14	7.00	1.43	1.42	9.26	9.128	ns
12 mA	STD	0.64	6.30	0.05	1.45	0.46	6.41	6.16	1.56	1.63	8.91	8.656	ns
	-1	0.55	5.35	0.04	1.23	0.39	5.45	5.24	1.56	1.63	7.58	7.364	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-70 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	8.76	0.05	1.59	0.46	7.63	9.35	1.87	1.50	10.13	11.851	ns
	-1	0.55	7.45	0.04	1.35	0.39	6.49	7.95	1.87	1.50	8.62	10.081	ns
4 mA	STD	0.64	5.41	0.05	1.59	0.46	5.42	5.94	2.07	1.84	7.92	8.442	ns
	-1	0.55	4.60	0.04	1.35	0.39	4.61	5.05	2.07	1.85	6.74	7.181	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-71 • 1.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 135°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.51	0.05	1.45	0.46	14.32	14.29	1.88	1.43	16.82	16.794	ns
	-1	0.55	11.49	0.04	1.23	0.39	12.18	12.16	1.88	1.43	14.31	14.286	ns
4 mA	STD	0.64	10.38	0.05	1.45	0.46	11.40	10.67	2.07	1.77	13.90	13.175	ns
	-1	0.55	8.83	0.04	1.23	0.39	9.70	9.08	2.07	1.77	11.82	11.207	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-72 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	9.05	0.05	1.56	0.45	7.38	9.05	1.81	1.45	9.80	11.47	ns
	-1	0.53	7.70	0.04	1.32	0.38	6.28	7.70	1.81	1.45	8.34	9.75	ns
4 mA	STD	0.63	5.75	0.05	1.56	0.45	5.25	5.75	2.00	1.78	7.67	8.17	ns
	-1	0.53	4.89	0.04	1.32	0.38	4.46	4.89	2.00	1.78	6.52	6.95	ns
6 mA	STD	0.63	5.05	0.05	1.56	0.45	4.92	5.05	2.04	1.87	7.34	7.47	ns
	-1	0.53	4.29	0.04	1.32	0.38	4.19	4.29	2.04	1.87	6.24	6.35	ns
8 mA	STD	0.63	4.41	0.05	1.56	0.45	2.18	1.91	4.27	4.55	3.35	3.11	ns
	-1	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns
12 mA	STD	0.63	4.41	0.05	1.56	0.45	2.18	1.91	4.27	4.55	3.35	3.11	ns
	-1	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-73 • 1.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.83	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.76	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.83	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	9.21	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns
6 mA	STD	0.63	10.10	0.05	1.40	0.45	10.28	9.62	2.05	1.80	12.70	12.04	ns
	-1	0.53	8.59	0.04	1.19	0.38	8.75	8.18	2.05	1.80	10.81	10.24	ns
8 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns
12 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-74 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	8.47	0.05	1.54	0.45	7.38	9.05	1.81	1.45	9.80	11.47	ns
	-1	0.53	7.21	0.04	1.31	0.38	6.28	7.70	1.81	1.45	8.34	9.75	ns
4 mA	STD	0.63	5.24	0.05	1.54	0.45	5.25	5.75	2.00	1.78	7.67	8.17	ns
	-1	0.53	4.45	0.04	1.31	0.38	4.46	4.89	2.00	1.78	6.52	6.95	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.*

Table 2-75 • 1.5 V LVCMOS Low Slew
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.07	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.12	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.04	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	8.54	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-80 • 3.3 V PCI/PCI-X
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.628	2.50	0.05	0.92	0.45	1.23	0.91	3.02	3.48	2.40	2.11	ns
–1	0.53	2.12	0.04	0.78	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-81 • 3.3 V PCI/PCI-X
Automotive-Case Conditions: T_J = 115°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.628	2.90	0.05	0.90	0.45	1.23	0.91	3.02	3.48	2.40	2.11	ns
–1	0.53	2.47	0.04	0.77	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12 on page 2-50. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

DDR Module Specifications

Input DDR Module

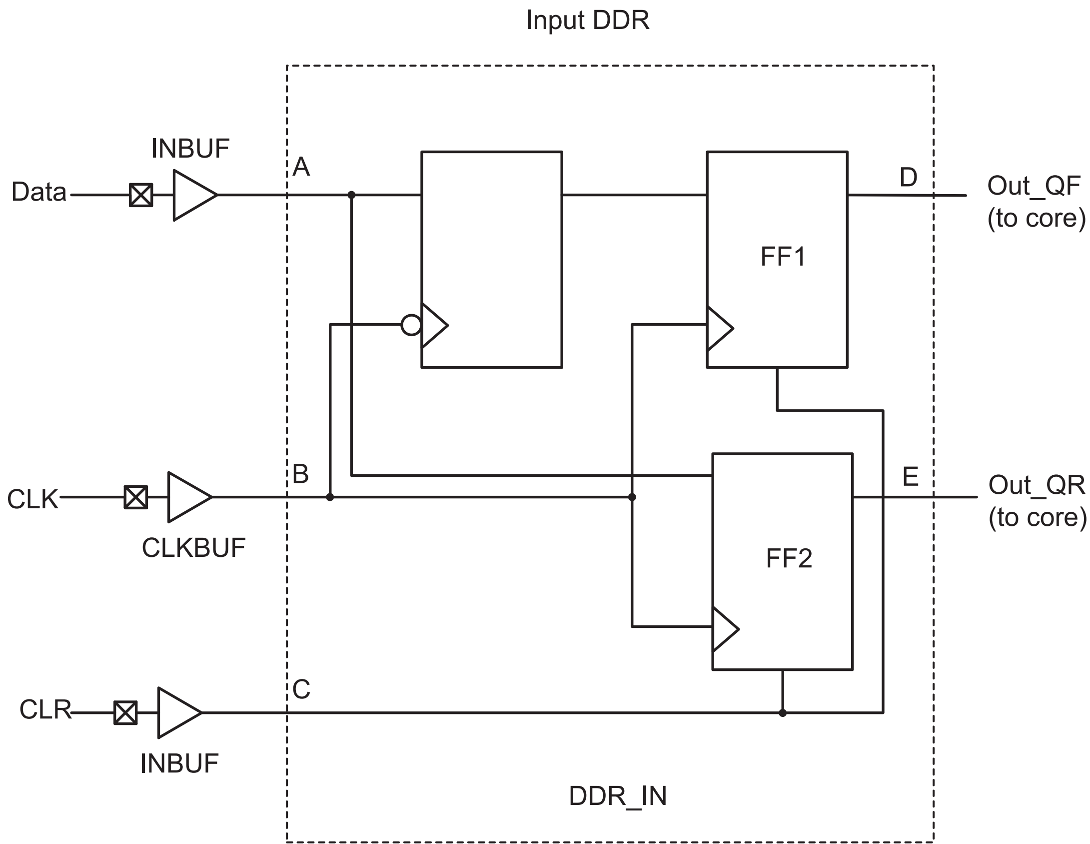


Figure 2-20 **• Input DDR Timing Model**

Table 2-98 **• Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR Input	A, B
t_{DDRIHD}	Data Hold Time of DDR Input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

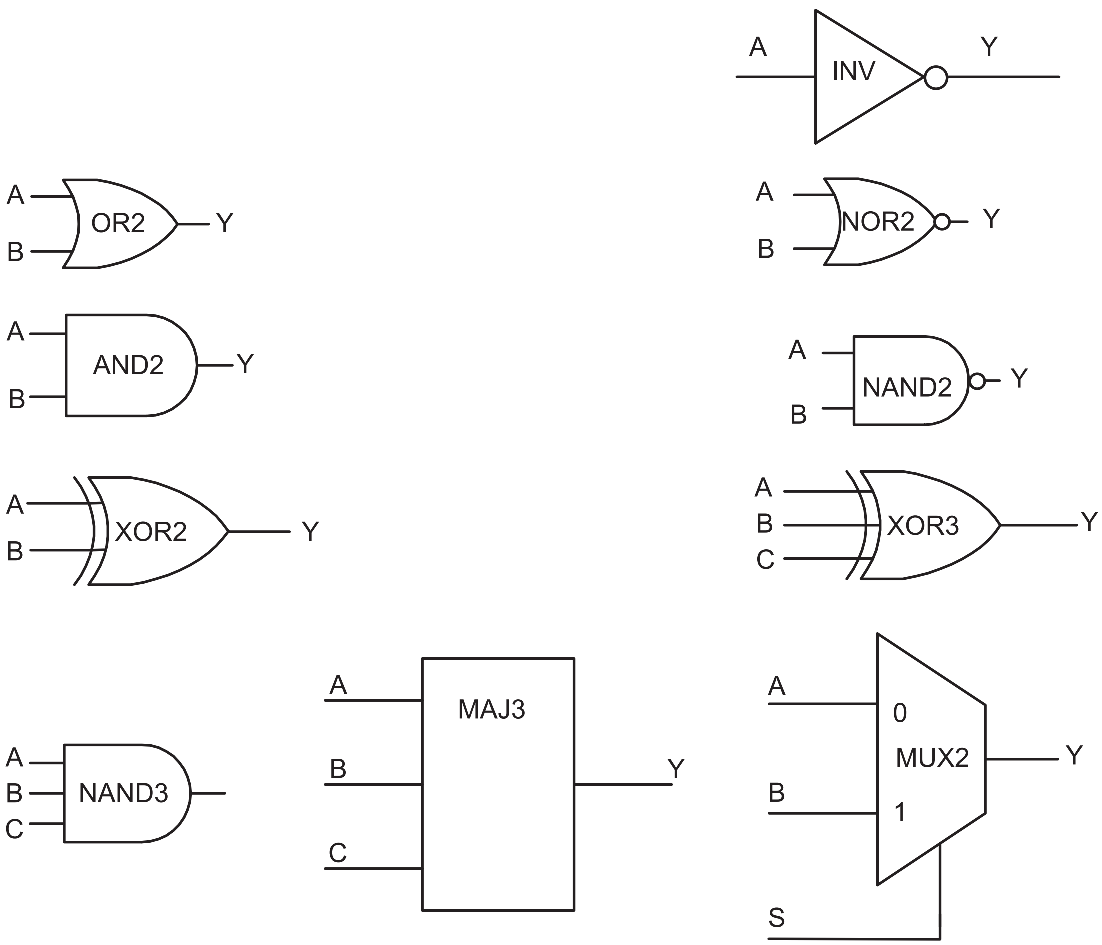


Figure 2-24 • **Sample of Combinatorial Cells**

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-116 • Automotive ProASIC3 CCC/PLL Specification

Parameter		Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		350	MHz
Delay Increments in Programmable Delay Blocks[1, 2]			160[3]		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Input Period Jitter				1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}		Max Peak-to-Peak Period Jitter			
		1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz		0.50%		0.70%	
24 MHz to 100 MHz		1.00%		1.20%	
100 MHz to 250 MHz		1.75%		2.00%	
250 MHz to 350 MHz		2.50%		5.60%	
Acquisition Time					
(A3P250 and A3P1000 only)	LockControl = 0			300	µs
	LockControl = 1			300	µs
(all other dies)	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter[4]					
(A3P250 and A3P1000 only)	LockControl = 0			1.6	ns
	LockControl = 1			1.6	ns
(all other dies)	LockControl = 0			1.6	ns
	LockControl = 1			0.8	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1[1, 2]		0.6		5.56	ns
Delay Range in Block: Programmable Delay 2[1, 2]		0.025		5.56	ns
Delay Range in Block: Fixed Delay[1, 2]			2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-5 on page 2-5 for deratings.*
2. *T_J = 25°C, VCC = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*

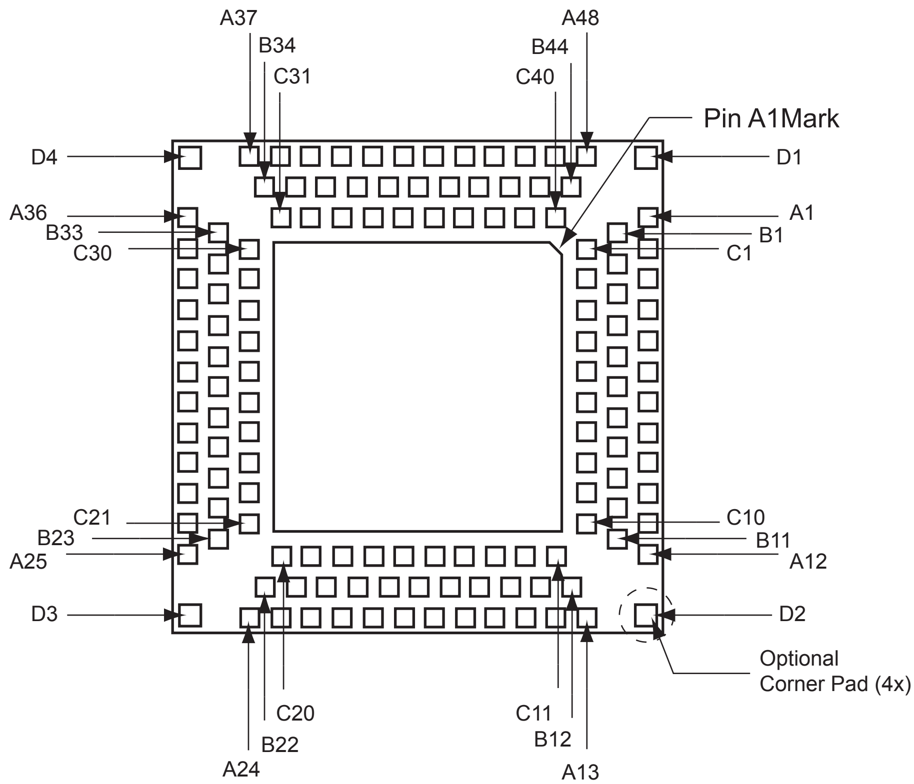
***Table 2-119* • RAM4K9**
Automotive-Case Conditions: T_J = 115°C, Worst Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.35	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN, WEN Setup Time	0.17	0.20	ns
t_{ENH}	REN, WEN Hold Time	0.12	0.14	ns
t_{BKS}	BLK Setup Time	0.28	0.33	ns
t_{BKH}	BLK Hold Time	0.02	0.03	ns
t_{DS}	Input data (DIN) Setup Time	0.22	0.26	ns
t_{DH}	Input data (DIN) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DOUT (output retained, WMODE = 0)	2.13	2.50	ns
	Clock High to New Data Valid on DOUT (flow-through, WMODE = 1)	2.81	3.30	ns
t_{CKQ2}	Clock High to New Data Valid on DOUT (pipelined)	1.07	1.25	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge	0.28	0.33	ns
t_{C2CWWH}[1]	Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge	0.26	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.38	0.45	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge	0.42	0.49	ns
t_{RSTBQ}	RESET Low to Data Out Low on DOUT (flow-through)	1.10	1.29	ns
	RESET Low to Data Out Low on DOUT (pipelined)	1.10	1.29	ns
$t_{REMRSTB}$	RESET Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET Recovery	1.79	2.10	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.25	0.30	ns
t_{CYC}	Clock Cycle Time	3.85	4.53	ns
F_{MAX}	Maximum Frequency	260	221	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to* *Table 2-5 on page 2-5* *for derating values.*

QN132



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

QN132	
Pin Number	A3P250 Function
A1	GAB2/IO117UPB3
A2	IO117VPB3
A3	VCCIB3
A4	GFC1/IO110PDB3
A5	GFB0/IO109NPB3
A6	VCCPLF
A7	GFA1/IO108PPB3
A8	GFC2/IO105PPB3
A9	IO103NDB3
A10	VCC
A11	GEA1/IO98PPB3
A12	GEA0/IO98NPB3
A13	GEC2/IO95RSB2
A14	IO91RSB2
A15	VCC
A16	IO90RSB2
A17	IO87RSB2
A18	IO85RSB2
A19	IO82RSB2
A20	IO76RSB2
A21	IO70RSB2
A22	VCC
A23	GDB2/IO62RSB2
A24	TDI
A25	TRST
A26	GDC1/IO58UDB1
A27	VCC
A28	IO54NDB1
A29	IO52NDB1
A30	GCA2/IO51PPB1
A31	GCA0/IO50NPB1
A32	GCB1/IO49PDB1
A33	IO47NSB1
A34	VCC
A35	IO41NPB1
A36	GBA2/IO41PPB1

QN132	
Pin Number	A3P250 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO118VDB3
B2	GAC2/IO116UDB3
B3	GND
B4	GFC0/IO110NDB3
B5	VCOMPLF
B6	GND
B7	GFB2/IO106PSB3
B8	IO103PDB3
B9	GND
B10	GEB0/IO99NDB3
B11	VMV3
B12	GEB2/IO96RSB2
B13	IO92RSB2
B14	GND
B15	IO89RSB2
B16	IO86RSB2
B17	GND
B18	IO78RSB2
B19	IO72RSB2
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO58VDB1

QN132	
Pin Number	A3P250 Function
B25	GND
B26	IO54PDB1
B27	GCB2/IO52PDB1
B28	GND
B29	GCB0/IO49NDB1
B30	GCC1/IO48PDB1
B31	GND
B32	GBB2/IO42PDB1
B33	VMV1
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO118UDB3
C2	IO116VDB3
C3	VCC
C4	GFB1/IO109PPB3
C5	GFA0/IO108NPB3
C6	GFA2/IO107PSB3
C7	IO105NPB3
C8	VCCIB3
C9	GEB1/IO99PDB3
C10	GNDQ
C11	GEA2/IO97RSB2
C12	IO94RSB2
C13	VCCIB2
C14	IO88RSB2
C15	IO84RSB2
C16	IO80RSB2

FG144	
Pin Number	A3P125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	A3P125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

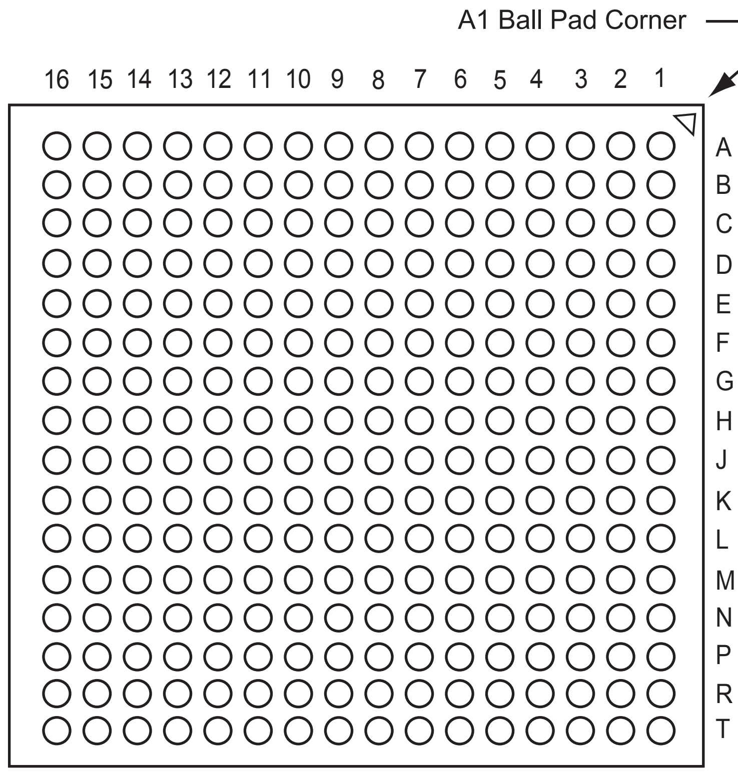
FG144	
Pin Number	A3P125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG144	
Pin Number	A3P250 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO29RSB0
A8	VCC
A9	IO33RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO117UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO22RSB0
B8	IO30RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV1
C1	IO117VDB3
C2	GFA2/IO107PPB3
C3	GAC2/IO116UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO24RSB0
C8	IO31RSB0
C9	IO34RSB0
C10	GBA2/IO41PDB1
C11	IO41NDB1
C12	GBC2/IO43PPB1

FG144	
Pin Number	A3P250 Function
D1	IO112NDB3
D2	IO112PDB3
D3	IO116VDB3
D4	GAA2/IO118UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO42PDB1
D10	IO42NDB1
D11	IO43NPB1
D12	GCB1/IO49PPB1
E1	VCC
E2	GFC0/IO110NDB3
E3	GFC1/IO110PDB3
E4	VCCIB3
E5	IO118VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO48PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO50NDB1
E12	IO51NDB1
F1	GFB0/IO109NPB3
F2	VCOMPLF
F3	GFB1/IO109PPB3
F4	IO107NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO48NDB1
F9	GCB0/IO49NPB1
F10	GND
F11	GCA1/IO50PDB1
F12	GCA2/IO51PDB1

FG144	
Pin Number	A3P250 Function
G1	GFA1/IO108PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO108NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO58UPB1
G9	IO53NDB1
G10	GCC2/IO53PDB1
G11	IO52NDB1
G12	GCB2/IO52PDB1
H1	VCC
H2	GFB2/IO106PDB3
H3	GFC2/IO105PSB3
H4	GEC1/IO100PDB3
H5	VCC
H6	IO79RSB2
H7	IO65RSB2
H8	GDB2/IO62RSB2
H9	GDC0/IO58VPB1
H10	VCCIB1
H11	IO54PSB1
H12	VCC
J1	GEB1/IO99PDB3
J2	IO106NDB3
J3	VCCIB3
J4	GEC0/IO100NDB3
J5	IO88RSB2
J6	IO81RSB2
J7	VCC
J8	TCK
J9	GDA2/IO61RSB2
J10	TDO
J11	GDA1/IO60UDB1
J12	GDB1/IO59UDB1

FG256



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

FG256	
Pin Number	A3P250 Function
G13	GCC1/IO48PPB1
G14	IO47NPB1
G15	IO54PDB1
G16	IO54NDB1
H1	GFB0/IO109NPB3
H2	GFA0/IO108NDB3
H3	GFB1/IO109PPB3
H4	VCOMPLF
H5	GFC0/IO110NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO48NPB1
H13	GCB1/IO49PPB1
H14	GCA0/IO50NPB1
H15	NC
H16	GCB0/IO49NPB1
J1	GFA2/IO107PPB3
J2	GFA1/IO108PDB3
J3	VCCPLF
J4	IO106NDB3
J5	GFB2/IO106PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO52PPB1
J13	GCA1/IO50PPB1
J14	GCC2/IO53PPB1
J15	NC
J16	GCA2/IO51PDB1

FG256	
Pin Number	A3P250 Function
K1	GFC2/IO105PDB3
K2	IO107NPB3
K3	IO104PPB3
K4	NC
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO52NPB1
K14	IO55RSB1
K15	IO53NPB1
K16	IO51NDB1
L1	IO105NDB3
L2	IO104NPB3
L3	NC
L4	IO102RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO59VPB1
L14	IO57VDB1
L15	IO57UDB1
L16	IO56PDB1
M1	IO103PDB3
M2	NC
M3	IO101NPB3
M4	GEC0/IO100NPB3

FG256	
Pin Number	A3P250 Function
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	NC
M9	IO74RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	NC
M14	GDB1/IO59UPB1
M15	GDC1/IO58UDB1
M16	IO56NDB1
N1	IO103NDB3
N2	IO101PPB3
N3	GEC1/IO100PPB3
N4	NC
N5	GNDQ
N6	GEA2/IO97RSB2
N7	IO86RSB2
N8	IO82RSB2
N9	IO75RSB2
N10	IO69RSB2
N11	IO64RSB2
N12	GNDQ
N13	NC
N14	VJTAG
N15	GDC0/IO58VDB1
N16	GDA1/IO60UDB1
P1	GEB1/IO99PDB3
P2	GEB0/IO99NDB3
P3	NC
P4	NC
P5	IO92RSB2
P6	IO89RSB2
P7	IO85RSB2
P8	IO81RSB2