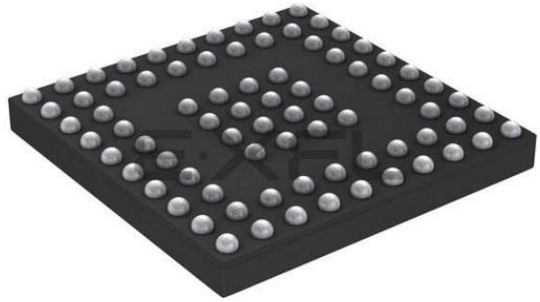
Lattice Semiconductor Corporation - LIF-MD6000-6JMG80I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1484
Number of Logic Elements/Cells	5936
Total RAM Bits	184320
Number of I/O	37
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	80-VFBGA
Supplier Device Package	80-CTFBGA (6.5x6.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lif-md6000-6jmg80i

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2.5. CMOS to MIPI DSI Display Interface Bridge

Figure 2.5 shows the block diagram for the CMOS to MIPI DSI display interface bridge. This solution bridges the CMOS parallel output from the application processor to a DSI display input.

Table 2.5 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

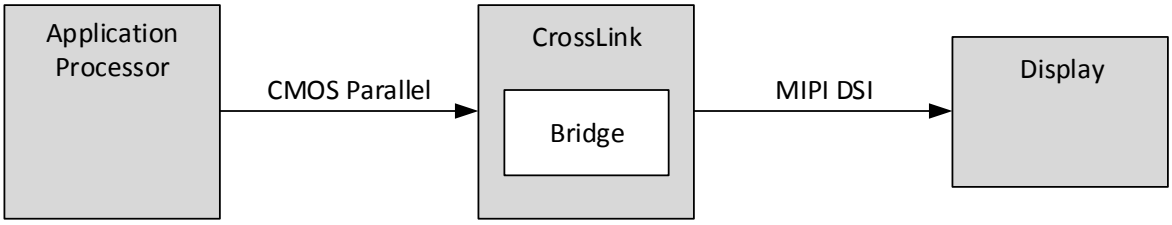


Figure 2.5. CMOS to MIPI DSI Display Interface Bridge

Table 2.5. CMOS to MIPI DSI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB CMOS Parallel @ 148.5 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~80 mW
Device I/O Used	28 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Figure 2.6 shows the block diagram for the CMOS to MIPI CSI-2 Image Sensor Interface Bridge. This solution bridges the CMOS parallel output from an image sensor to a CSI-2 input of an application processor.

Table 2.6 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

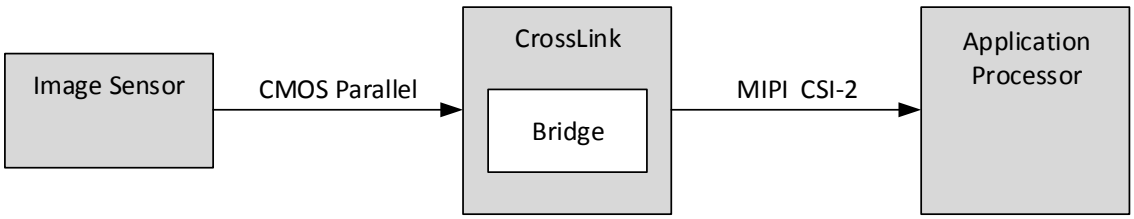


Figure 2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Table 2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 12-bit RAW CMOS Parallel @ 74.25 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 12-bit RAW 4-Lane MIPI D-PHY @ ~450 Mb/s per lane
Additional System Functions	I^2C for Camera Configuration GPIO for image sensor reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~75 mW
Device I/O Used	16 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge

Figure 2.8 shows the block diagram for the MIPI DSI to CMOS display interface bridge. This solution bridges the MIPI DSI output from the application processor to CMOS parallel display input.

Table 2.8 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting multiple pixel formats and data rates up to 1.5 Gb/s per lane input and up to 150 MHz CMOS parallel output. For details, refer to FPGA-IPUG-02004, MIPI D-PHY to CMOS Interface Bridge Soft IP User Guide.

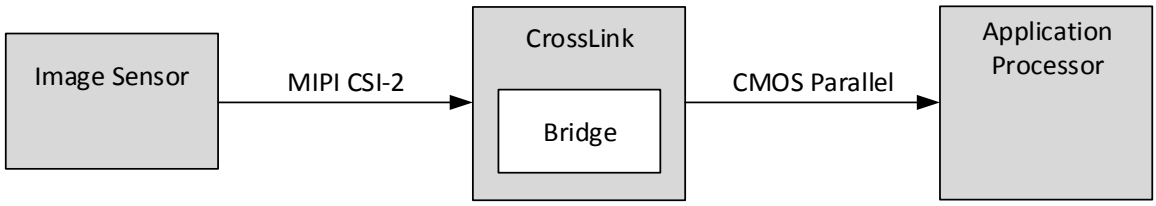


Figure 2.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge

Table 2.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	1080p60, RAW12 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, RAW12 CMOS Parallel @ 74.25 MHz
Additional System Functions	I^2C for Camera Configuration GPIO for image sensor reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	60 mW
Device I/O Used	16 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	15% of LUT4; ~15% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

3. Product Feature Summary

Table 3.1 lists CrossLink device information and packages.

Table 3.1. CrossLink Feature Summary

Device	**CrossLink**
LUTs	5936
sysMEM Blocks (9 kb)	20
Embedded Memory (kb)	180
Distributed RAM Bits (kb)	47
General Purpose PLL	1
NVCM	Yes
Embedded I^2C	2
Oscillator (10 KHz)	1
Oscillator (48 MHz)	1
Hardened MIPI D-PHY	2[1, 2]
Packages	**I/O**
36 WLCSP[2] (2.535 × 2.583 mm^2, 0.6 mm)	17
64 ucfBGA (3.5 × 3.5 mm^2, 1 mm)	29
80 ctfBGA (6.5 x 6.5 mm^2, 1 mm)	36
81 csfBGA (4.5 × 4.5 mm^2, 1 mm)	37

Notes:

1. Additional D-PHY Rx interfaces are available using programmable I/O.
2. Only one Hardened D-PHY is available in 36 WLCSP package.

4.1. MIPI D-PHY Blocks

The top side of the device includes two hard MIPI D-PHY quads. The D-PHY can be configured to support both camera interface (CSI-2) and display interface (DSI) applications. Below is a summary of the features supported by the hard D-PHY quads. Refer to FPGA-TN-02012, CrossLink High-Speed I/O Interface for more information on the Hard D-PHY quads.

- Transmit and Receive compliant to D-PHY Revision 1.1
- High-Speed (HS) and Low-Power (LP) mode support (including built-in contention detect)
- Up to 6 Gb/s per quad (1500 Mb/s data rate per lane)
- Dedicated PLL for Transmit Frequency Synthesis
- Dedicated Serializer and De-Serializer blocks for fabric interfacing
- Supports continuous clock mode or low power clock mode

Lattice Semiconductor provides a set of pre-engineered IP modules which include the full implementation and control of the hard D-PHY blocks for the examples in Application Examples section on page 7, enabling designers to focus on unique aspects of their design.

4.2. Programmable I/O Banks

CrossLink devices provide programmable I/O which can be used to interface to a variety of external standards. The I/O features are summarized below, and described in detail in FPGA-TN-02012, CrossLink High-Speed I/O Interface and FPGA-TN-02016, CrossLink sysI/O Usage Guide. The programmable LVDS/CMOS I/O (Banks 1 and 2) are described below, while the CMOS GPIO (bank 0) and hard D-PHY quads are described separately.

Programmable LVDS/CMOS I/O (Bank 1 and 2) features:

- Built-in support for the following differential standards
  - LVDS – Tx and Rx
  - SLVS – Rx
  - SubLVDS – Rx
  - MIPI – Rx (both LP and HS receive on a single differential pair)
- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs)
  - LVTTL33
- Independent voltage levels per bank based on VCCIO supply
- Input/output gearboxes per LVDS pair supporting several ratios for video interface applications
  - DDRX1, DDRX2, DDRX4, DDRX8 and DDRX71, DDRX141
  - Programmable delay cells to support edge-aligned and center-aligned interfaces
- Programmable differential termination (~ 100 Ω) with dynamic enable control
- Tri-state control for output
- Input/output register blocks
- Single-ended standards support open-drain and programmable input hysteresis
- Optional weak pull-up resistors

To ensure the MIPI Rx interface implemented in FPGA fabric using Programmable I/Os runs in an optimal environment, follow this guideline of assigning I/Os to the bank for the MIPI Rx inputs:

- When an SLVS/MIPI Rx interface is placed in Bank 1 or 2, do not place both Banks 1 and 2 with LVCMOS outputs in these 2 banks.

4.3. Programmable FPGA Fabric

4.3.1. FPGA Fabric Overview

CrossLink is built around a programmable logic fabric consisting of 5936 four input lookup tables (LUT4) arranged alongside dedicated registers in Programmable Functional Units (PFU). These PFU blocks are the building blocks for logic, arithmetic, RAM and ROM functions. The PFU blocks are connected via a programmable routing network. The Lattice Diamond design software configures the PFU blocks and the programmable routing for each unique design. Interspersed between rows of PFU are rows of sysMEM™ Embedded Block RAM (EBR), with programmable I/O banks, embedded I^2C and embedded MIPI D-PHY arranged on the top and bottom of the device as shown in Figure 4.2.

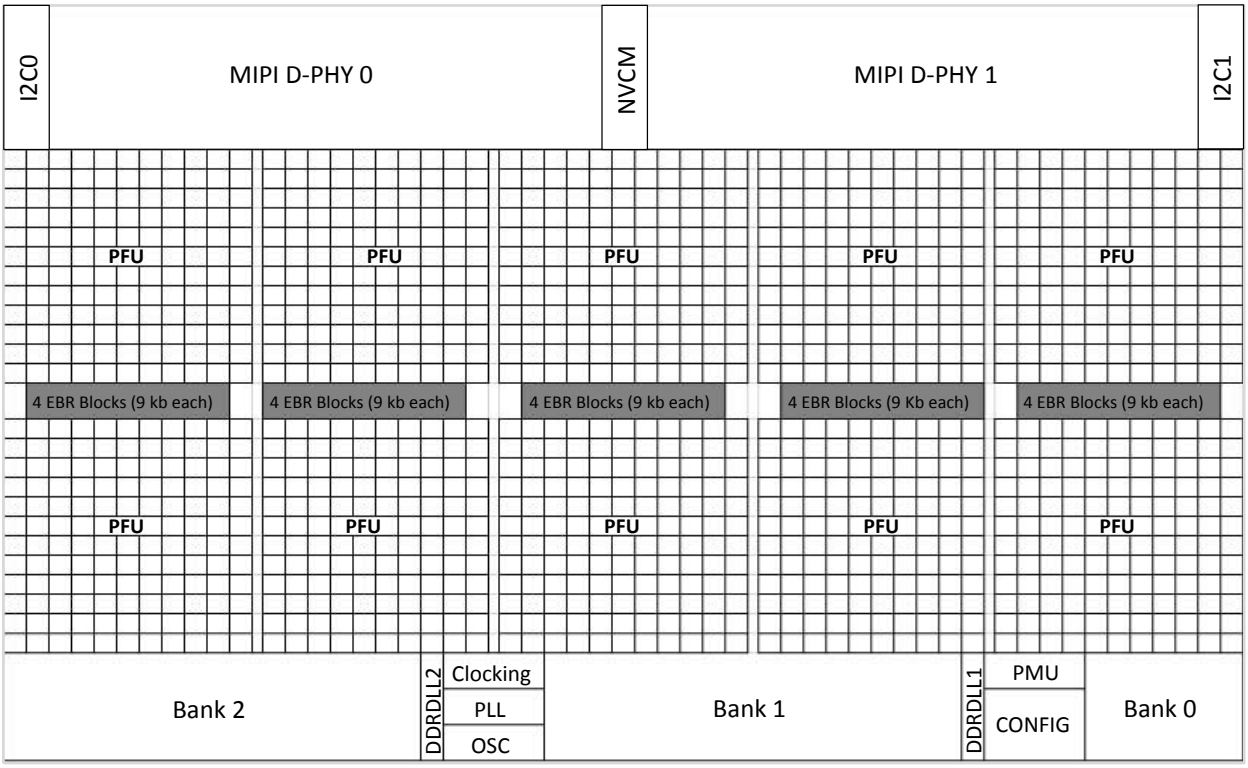


Figure 4.2. CrossLink Device Simplified Block Diagram (Top Level)

4.3.2. Clocking Overview

The CrossLink device family provides resources to support a wide range of clocking requirements for programmable video bridging. These resources are listed below. For details, refer to FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide.

- sysCLOCK PLL
  - Flexible Frequency Synthesis (See Table 5.14 for input frequency range and output frequency range.)
  - Dynamically selectable Clock Input
  - Four Clock Outputs
    - Independent, dynamic enable control
    - Programmable phase adjustment
  - Standby Input
  - Lock Output
- Clock Distribution Network
  - Eight Primary Clocks
    - Dedicated Clock input pins (PCLK)
    - Source from PLL, Clock Divider, Hard D-PHY blocks or On-chip Oscillator

- Four Edge Clocks for high-speed DDR interfaces
  - 2 per Programmable I/O bank
  - Source from PCLK pins, PLL or DLL blocks
  - Programmable Clock divider per Edge Clock
  - Delay primitives for 90 degree phase shifting of clock/data (DDRDLL, DLLDEL)
- Dynamic Clock Control
  - Fabric control to disable clock nets for power savings
- Dynamic Clock Select
  - Smart clock multiplexer with two independent inputs and glitchless output support
- Two On-Chip Oscillators
  - Always-on Low Frequency (LFCLKOUT) with nominal frequency of 10 kHz
  - High-Frequency (HFCLKOUT) with nominal frequency of 48 MHz, programmable output dividers, and dynamic enable control

4.3.3. Embedded Block RAM Overview

CrossLink devices also contain sysMEM Embedded Block RAM (EBR). The EBR consists of a 9 kB RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Supported modes and other general information on the EBR are listed below. For details, refer to FPGA-TN-02017, CrossLink Memory Usage Guide.

- Support for different memory configurations
  - Single Port
  - True Dual Port
  - Pseudo Dual Port
  - ROM
  - FIFO (logic wrapper added automatically by design tools)
- Flexible customization features
  - Initialization of RAM/ROM
  - Memory cascading (handled automatically by design tools)
  - Optional parity bit support
  - Byte-enable
  - Multiple block size options
  - RAM modes support optional Write Through or Read-Before-Write modes

4.4. System Resources

4.4.1. CMOS GPIO (Bank 0)

CrossLink provides dedicated CMOS GPIO on Bank 0 of the device. These GPIO do not include differential signaling support. A summary of the features associated with these GPIOs is listed below:

- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs)
  - LVTTL33
- Tri-state control for output
- Input/output register blocks
- Open-drain option and programmable input hysteresis
- Internal pull-up resistors with configurable values of 3.3 kΩ, 6.8 kΩ, 10 kΩ

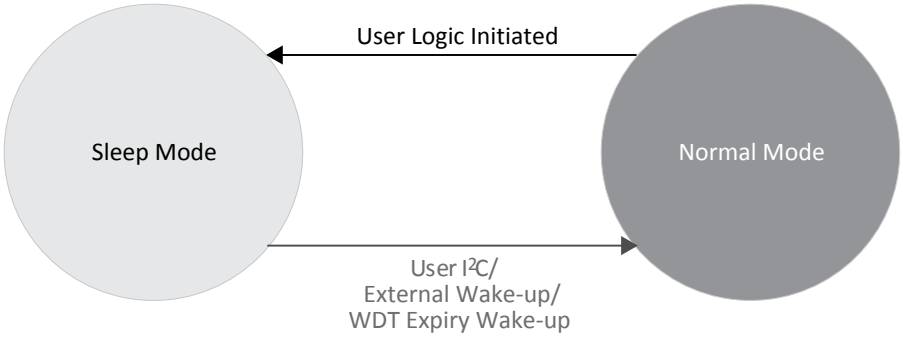


Figure 4.4. CrossLink PMU State Machine

For more details, refer to FPGA-TN-02018, Power Management and Calculation for CrossLink Devices.

4.4.3. Device Configuration

The CrossLink SRAM can be configured as follows:

- Internal Non Volatile Configuration Memory (NVCM)
  - NVCM can be programmed using either the SPI or I²C port
- Standard Serial Peripheral Interface (Master SPI Mode) Interface to external SPI Flash
- System microprocessor to drive a serial Slave SPI port (SSPI mode)
- System microprocessor to drive a serial Slave I²C port

For more information, refer to FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide. In addition to the flexible configuration modes, the CrossLink configuration engine supports the following special features:

- TransFR (Transparent Field Reconfiguration) allowing users to update logic in field without interrupting system operation by freezing I/O states during configuration
- Dual-Boot Support for primary and golden bitstreams provides automatic recovery from configuration failures
- Security and One-Time Programmable (OTP) modes protect bitstream integrity and prevent readback
- 64-bit unique TraceID per device

4.4.4. User I²C IP

CrossLink devices have two I²C IP cores that can be configured either as an I²C master or as an I²C slave. The I2C0 core has pre-assigned pins, and supports PMU wakeup over I²C. The pins for the I2C1 interface are not pre-assigned – user can use any General Purpose I/O pins.

The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I²C, refer to FPGA-TN-02019, CrossLink I2C Hardened IP Usage Guide.

5.11.2. Preliminary Hardened MIPI D-PHY I/Os

Table 5.11. Preliminary MIPI D-PHY

	Description	Min	Typ	Max	Unit
Receiver					
High Speed					
V_{CMRX}	Common-Mode Voltage HS Receive Mode	70	—	330	mV
V_{IDTH}	Differential Input High Threshold	—	—	70	mV
V_{IDTL}	Differential Input Low Threshold	−70	—	—	mV
V_{IHHS}	Single-ended Input High Voltage	—	—	460	mV
V_{ILHS}	Single-ended Input Low Voltage	−40	—	—	mV
$V_{TERM-EN}$	Single-ended Threshold for HS Termination Enable	—	—	450	mV
Z_{ID}	Differential Input Impedance	80	100	125	Ω
Low Power					
V_{IH}	Logic 1 Input Voltage	880	—	—	mV
V_{IL}	Logic 0 Input Voltage, not in ULP State	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 Input Voltage, in ULP State	—	—	300	mV
V_{HYST}	Input Hysteresis	25	—	—	mV
Transmitter					
High Speed					
V_{CMTX}	HS Transmit Static Common Mode Voltage	150	200	250	mV
V_{OD}	HS Transmit Differential Voltage	140	200	270	mV
V_{OHHS}	HS Output High Voltage	—	—	360	mV
Z_{OS}	Single-ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single-ended Output Impedance Mismatch	—	—	10	%
Low Power					
V_{OH}	Output High Level	1.1	1.2	1.3	V
V_{OL}	Output Low Level	−50	—	50	mV
Z_{OLP}	Output Impedance of LP Transmitter	110	—	—	Ω

Table 5.13. Preliminary CrossLink External Switching Characteristics (*Continued*)

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Generic DDRX8 or DDRX4 I/O with Clock and Data Aligned at General Purpose Pins (GDDRX8_RX/TX.ECLK.Aligned or GDDRX4_RX/TX.ECLK.Aligned)					
$t_{DVA\_GDDRX4\_8}$	Input Data Valid After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s	—	0.188	ns
		Other Data Rates	—	–0.229	ns+1/2UI
$t_{DVE\_GDDRX4\_8}$	Input Data Hold After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s	0.646	—	ns
		Other Data Rates	0.229	—	ns+1/2UI
$t_{DIA\_GDDRX4\_8}$	Output Data Invalid After CLK Rising and Falling edges Output	—	—	0.120	ns
$t_{DIB\_GDDRX4\_8}$	Output Data Invalid Before CLK Output Rising and Falling edges	—	—	0.120	ns
$f_{MAX\_GDDRX4\_8}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz
General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing					
$t_{SU\_GDDRX\_MP}$	Input Data Set-Up Before CLK	—	0.167	—	ns
$t_{HO\_GDDRX\_MP}$	Input Data Hold After CLK	—	0.167	—	ns
$f_{MAX\_GDDRX\_MP}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz
Generic DDRX71 or DDRX141 Inputs (GDDRX71_RX.ECLK or GDDRX141_RX.ECLK)					
t_{RPBi_DVA}	Input Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.3	UI
		—	—	–0.222	ns+ (i+ 1/2)*UI
t_{RPBi_DVE}	Input Hold Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.7	—	UI
		—	0.222	—	ns+ (i+ 1/2)*UI
f_{MAX_RX71}	DDR71/DDR141 ECLK Frequency[3]	—	—	450	MHz
Generic DDRX71 Outputs with Clock and Data Aligned at Pin (GDDRX71_TX.ECLK)					
T_{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.143	ns+i*UI
T_{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	–0.143	—	ns+ (i+ 1)*UI
$T_{TPBi\_skew\_UI}$	Tx skew in UI	—	—	0.15	UI
f_{MAX_TX71}	DDR71 ECLK Frequency[3]	csfBGA81	—	525	MHz
		WLCSP36	—	500	MHz

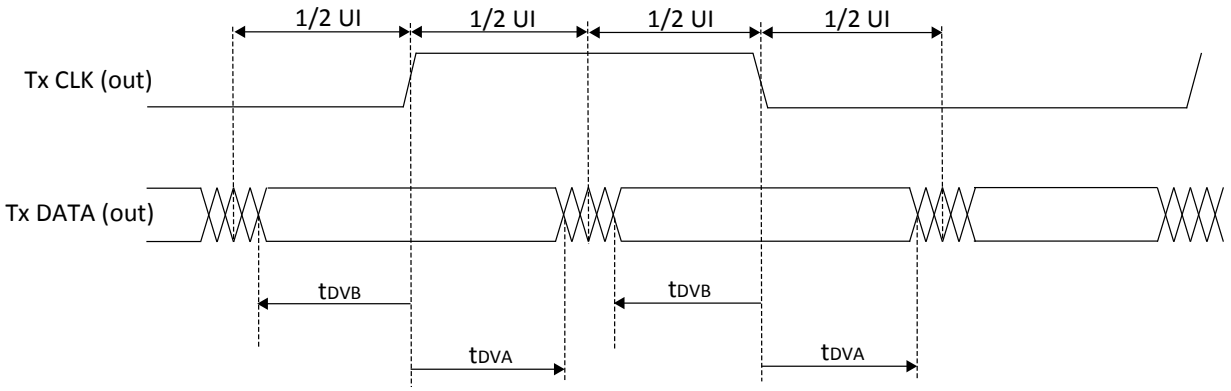


Figure 5.3. Transmit TX.CLK.Centered Output Waveforms

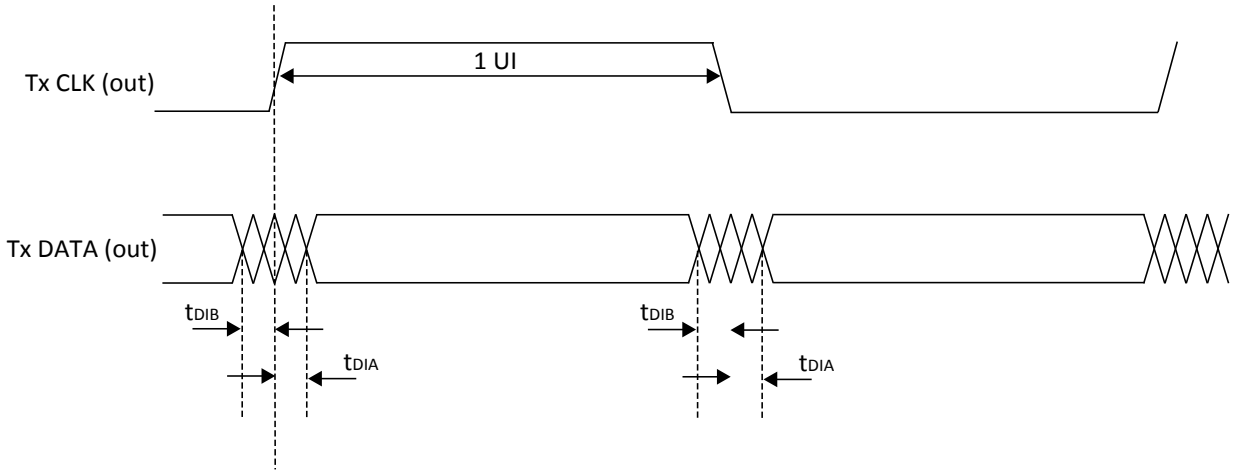


Figure 5.4. Transmit TX.CLK.Aligned Waveforms

5.14. Preliminary sysCLOCK PLL Timing

Over recommended operating conditions.

Table 5.14. Preliminary sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Unit
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	10	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	4.6875	600	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH4}	Output Phase Accuracy	—	–5	5	%
t_{OPJIT}[1]	Output Clock Period Jitter[3]	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter[3]	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.05	UIPP
	Output Clock Phase Jitter	$f_{PFD} > 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.05	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
t_{LOCK}[2]	PLL Lock-in Time	—	—	1	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	500	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns

Notes:

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} \geq 10$ MHz. For $f_{PFD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

5.18. CrossLink sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 5.20. CrossLink sysCONFIG Port Timing Specifications

Symbol	Parameter	Min	Max	Unit
All Configuration Mode				
t_{PRGM}	CRESETB LOW Pulse Accepted	145	—	ns
Slave SPI				
f_{CCLK}	SPI_SCK Input Clock Frequency	—	110	MHz
t_{STSU}	MOSI Setup Time	0.5	—	ns
t_{STH}	MOSI Hold Time	2.0	—	ns
t_{STCO}	SPI_SCK Falling Edge to Valid MISO Output	—	13.3	ns
t_{SCS}	Chip Select HIGH Time	42	—	ns
t_{SCSS}	Chip Select Setup Time	0.5	—	ns
t_{SCSH}	Chip Select Hold Time	0.5	—	ns
Master SPI				
f_{CCLK}	MCK Output Clock Frequency	—	52.8	MHz
I^2C*				
f_{MAX}	Maximum SCL Clock Frequency (Fast-Mode Plus	—	1	MHz

***Note**: Refer to the I^2C specification for timing requirements when configuring with I^2C port.

5.19. Preliminary SRAM Configuration Time from NVCM

Over recommended operating conditions.

Table 5.21. Preliminary SRAM Configuration Time from NVCM

Symbol	Parameter	Typ	Unit
$t_{CONFIGURATION}$	POR to Device I/O Active[1]	83	ms

Note:

1. Before and during configuration, the I/Os are held in tristate with weak internal pullups enabled. I/Os are released to user functionality when the device has finished configuration.

6.4. csfBGA81 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
A2	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A3	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
A4	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
A5	VCCA_DPHY1	DPHY1	—	—
A6	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A7	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
A8	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
A9	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
B1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
B3	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
B4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
B5	GNDPLL_DPHYX	GND	—	—
B6	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B7	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
B8	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
B9	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
C1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
C2	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
C3	GNDA_DPHY1	DPHY1	—	—
C4	VCCPLL_DPHY1	DPHY1	—	—
C5	GND	GND	—	—
C6	VCCPLL_DPHY0	DPHY0	—	—
C7	GNDA_DPHY0	DPHY0	—	—
C8	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
C9	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
D1	PB34A	1	GR_PCLK1_0	True_OF_PB34B
D2	PB34B	1	—	Comp_OF_PB34A
D3	VCCA_DPHY1	DPHY1	—	—
D4	GND	GND	—	—
D5	VCCAUX	VCCAUX	—	—
D6	GND	GND	—	—
D7	VCCA_DPHY0	DPHY0	—	—
D8	PB16B	2	PCLKC2_0	Comp_OF_PB16A
D9	PB16A	2	PCLKT2_0	True_OF_PB16B
E1	PB38A	1	—	True_OF_PB38B
E2	PB38B	1	—	Comp_OF_PB38A
E3	VCC	VCC	—	—
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCCIO2	2	—	—

6.5. Dual Function Pin Descriptions

The following table describes the dual functions available to certain pins on the CrossLink device. These pins may alternatively be used as general purpose I/O when the described dual function is not enabled.

Signal Name	I/O	Description
General Purpose		
USER_SCL	I/O	User Slave I2C0 clock input and Master I²C0 clock output. Enables PMU wake-up via I2C0.
USER_SDA	I/O	User Slave I2C0 data input and Master I²C0 data output. Enables PMU wakeup via I2C0.
PMU_WKUPN	—	This pin wakes the PMU from sleep mode when toggled low.
Clock Functions		
GPLL2_0[T, C]_IN	I	General Purpose PLL (GPLL) input pads: T = true and C = complement. These pins can be used to input a reference clock directly to the General Purpose PLL. These pins do not provide direct access to the primary clock network.
GR_PCLK[Bank]0	I	These pins provide a short General Routing path to the primary clock network. Refer to FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide for details.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins provide direct access to the primary and edge clock networks.
MIPI_CLK[T/C][Bank]_0	I/O	MIPI D-PHY Reference CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins can be used to input a reference clock directly to the D-PHY PLLs. These pins do not provide direct access to the primary clock network.
Configuration		
CDONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. Holding CDONE delays configuration.
SPI_SCK	I	Input Configuration Clock for configuring CrossLink in Slave SPI mode (SSPI).
MCK	O	Output Configuration Clock for configuring CrossLink in Master SPI mode (MSPI).
SPI_SS	I	Input Chip Select for configuring CrossLink in Slave SPI mode (SSPI).
CSN	O	Output Chip Select for configuring CrossLink in Master SPI mode (MSPI).
MOSI	I/O	Data Output when configuring CrossLink in Master SPI mode (MSPI), data input when configuring CrossLink in Slave SPI mode (SSPI).
MISO	I/O	Data Input when configuring CrossLink in Master SPI mode (MSPI), data output when configuring CrossLink in Slave SPI mode (SSPI).
SCL	I/O	Slave I²C clock I/O when configuring CrossLink in I²C mode.
SDA	I/O	Slave I²C data I/O when configuring CrossLink in I²C mode.

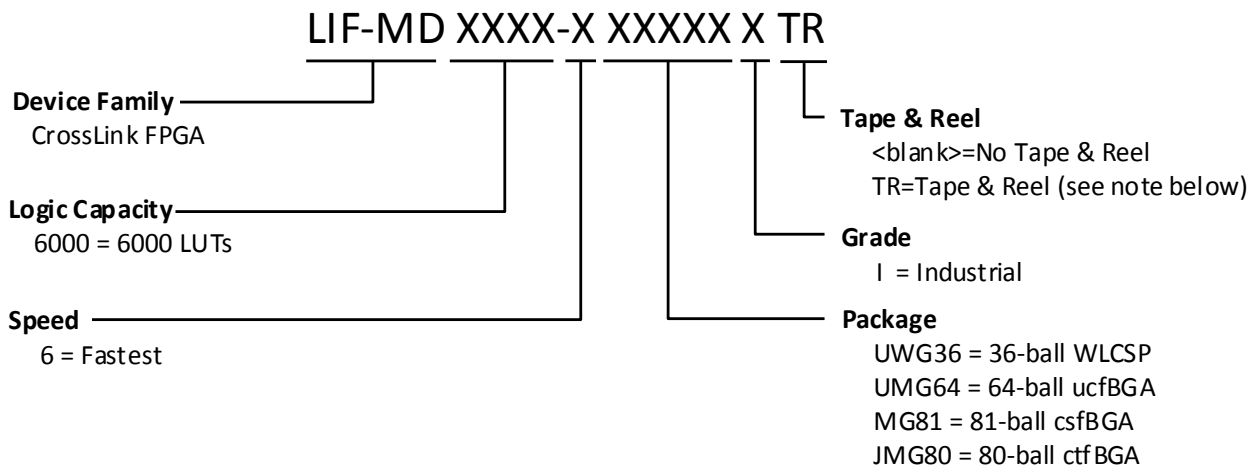
6.6. Dedicated Function Pin Descriptions

Signal Name	I/O	Description
Configuration		
CRESET_B	I	Configuration Reset, active LOW.
MIPI D-PHY		
DPHY[num]_CK[P/N]	I/O	MIPI D-PHY Clock [num] = D-PHY 0 or 1, P = Positive, N = Negative.
DPHY[num]_D[P/N][lane]	I/O	MIPI D-PHY Data [num] = D-PHY 0 or 1, P = Positive, N = Negative, Lane = data lane in the D-PHY block 0, 1, 2 or 3.

6.7. Pin Information Summary

Pin Type	CrossLink			
	WLCSP36	ucfBGA64	ctfBGA80	csfBGA81
General Purpose I/O per Bank				
Bank 0	7	6	7	7
Bank 1	0	10	14	14
Bank 2	10	12	16	16
Total General Purpose Single Ended IO	**17**	**28**	**37**	**37**
Differential I/O pairs per Bank				
Bank 0	0	0	0	0
Bank 1	0	5	7	7
Bank 2	5	6	8	8
Total General Purpose Differential I/O pairs	5	11	15	15
D-PHY	1	2	2	2
D-PHY Clock/Data	10	20	20	20
D-PHY VCC	1	2	4	4
D-PHY GND	1	1	3	3
VCC/VCCIOx/VCCAUX/VCCGPLL	4	8	9	10
GND	3	4	9	9
CRESETB	1	1	1	1
Total Balls	**36**	**64**	**80**	**81**

7. CrossLink Part Number Description



7.1. Ordering Part Numbers

Industrial

Part Number	Grade	Package	Pins	Temp.	LUTs (K)
LIF-MD6000-6UWG36ITR	–6	Lead free WLCSP	36	Industrial	5.9
LIF-MD6000-6UMG64I	–6	Lead free ucfBGA	64	Industrial	5.9
LIF-MD6000-6MG81I	–6	Lead free csfBGA	81	Industrial	5.9
LIF-MD6000-6JMG80I	–6	Lead free ctfBGA	80	Industrial	5.9

Note: UWG36 package is available in shipments of 5000 pieces/reel (TR), 1000 pieces/reel (TR1K), and 50 pieces/reel (TR50 – for samples only).