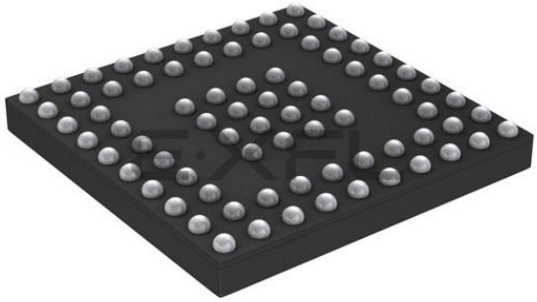

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1484
Number of Logic Elements/Cells	5936
Total RAM Bits	184320
Number of I/O	37
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	80-TFBGA
Supplier Device Package	80-ckfBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lif-md6000-6kmg80i

Contents

Figures

2.2. 1:2 MIPI DSI Display Interface Bridge

Figure 2.2 shows the block diagram for the 1:2 MIPI DSI display interface bridge. This solution duplicates the display output from single application processor DSI output to two different DSI displays.

Table 2.2 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting any input encoding, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. The solution can be customized to split the input image, or perform additional bridging operations. For details, refer to FPGA-IPUG-02001, 1:2 and 1:1 MIPI DSI Display Interface Bridge Soft IP User Guide.

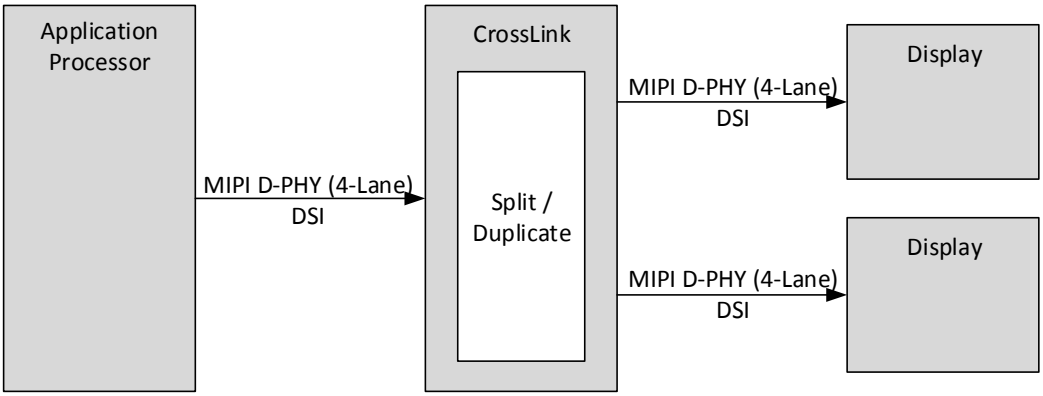


Figure 2.2. 1:2 MIPI DSI Display Interface Bridge

Table 2.2. 1:2 MIPI DSI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Split/Duplicate Image
Output Type	2 x 1080p60, 24-bit RGB 2 x 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~140 mW
Device I/O Used	10 Programmable I/O; 2 x Hard D-PHY Quads
Fabric Resources Used	80% of LUT4; ~80% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.3. FPD-Link/OpenLDI LVDS to MIPI DSI Display Interface Bridge

Figure 2.3 shows the block diagram for the FPD-Link/OpenLDI LVDS to MIPI DSI display interface bridge. This solution bridges the single or dual-channel FPD-Link/OpenLDI LVDS display output from the application processor to a MIPI DSI input display.

Table 2.3 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting both RGB666 and RGB888, variable number of LVDS data lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02005, OpenLDI/FPD-Link/LVDS to MIPI DSI Interface Bridge Soft IP User Guide.

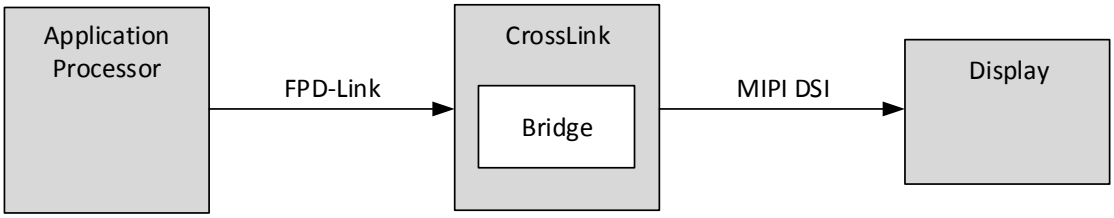


Figure 2.3. FPD-Link/OpenLDI LVDS to MIPI DSI Display Interface Bridge

Table 2.3. FPD-Link/OpenLDI LVDS to MIPI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 2 Channels (2 x 4 Data Lanes and 2 x 1 Clock Lane) @ 74.25 MHz FPD-Link Clock
Programmable Fabric Operation(s)	Bridge
Output Type	1 x 1080p60, 24-bit RGB 1 x 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	TBD mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~50% of LUT4; ~60% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Figure 2.4 shows the block diagram for the MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge. This solution bridges the MIPI DSI output from the application processor to a single or dual channel FPD-Link/OpenLDI LVDS display input.

Table 2.4 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting both RGB666 and RGB888, variable number of LVDS data lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02003, MIPI DSI to OpenLDI/FPD-Link/LVDS Interface Bridge Soft IP User Guide.

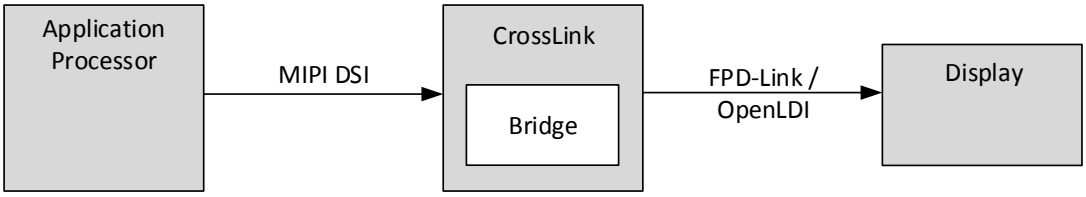


Figure 2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Table 2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Bridge
Output Type	1080p60, 24-bit RGB 2 Channels (2 x 4 Data Lanes and 2 x 1 Clock Lane) @ 74.25MHz FPD-Link Clock
Additional System Functions	Display Configuration Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	TBD mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~30% of LUT4; ~30% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

3. Product Feature Summary

Table 3.1 lists CrossLink device information and packages.

Table 3.1. CrossLink Feature Summary

Device	**CrossLink**
LUTs	5936
sysMEM Blocks (9 kb)	20
Embedded Memory (kb)	180
Distributed RAM Bits (kb)	47
General Purpose PLL	1
NVCM	Yes
Embedded I^2C	2
Oscillator (10 KHz)	1
Oscillator (48 MHz)	1
Hardened MIPI D-PHY	2[1, 2]
Packages	**I/O**
36 WLCSP[2] (2.535 × 2.583 mm^2, 0.6 mm)	17
64 ucfBGA (3.5 × 3.5 mm^2, 1 mm)	29
80 ctfBGA (6.5 x 6.5 mm^2, 1 mm)	36
81 csfBGA (4.5 × 4.5 mm^2, 1 mm)	37

Notes:

1. Additional D-PHY Rx interfaces are available using programmable I/O.
2. Only one Hardened D-PHY is available in 36 WLCSP package.

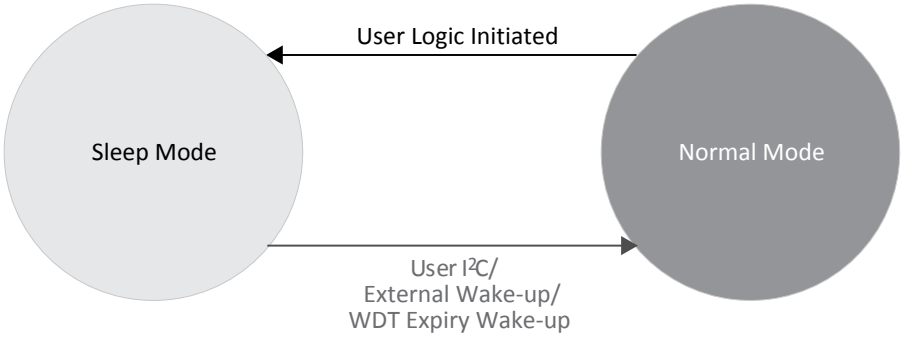


Figure 4.4. CrossLink PMU State Machine

For more details, refer to FPGA-TN-02018, Power Management and Calculation for CrossLink Devices.

4.4.3. Device Configuration

The CrossLink SRAM can be configured as follows:

- Internal Non Volatile Configuration Memory (NVCM)
  - NVCM can be programmed using either the SPI or I²C port
- Standard Serial Peripheral Interface (Master SPI Mode) Interface to external SPI Flash
- System microprocessor to drive a serial Slave SPI port (SSPI mode)
- System microprocessor to drive a serial Slave I²C port

For more information, refer to FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide. In addition to the flexible configuration modes, the CrossLink configuration engine supports the following special features:

- TransFR (Transparent Field Reconfiguration) allowing users to update logic in field without interrupting system operation by freezing I/O states during configuration
- Dual-Boot Support for primary and golden bitstreams provides automatic recovery from configuration failures
- Security and One-Time Programmable (OTP) modes protect bitstream integrity and prevent readback
- 64-bit unique TraceID per device

4.4.4. User I²C IP

CrossLink devices have two I²C IP cores that can be configured either as an I²C master or as an I²C slave. The I2C0 core has pre-assigned pins, and supports PMU wakeup over I²C. The pins for the I2C1 interface are not pre-assigned – user can use any General Purpose I/O pins.

The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I²C, refer to FPGA-TN-02019, CrossLink I2C Hardened IP Usage Guide.

5. DC and Switching Characteristics

5.1. Absolute Maximum Ratings

Table 5.1. Absolute Maximum Ratings[1, 2, 3]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Core Supply Voltage	–0.5	1.32	V
V_{CCPLL}	PLL Supply Voltage	–0.5	1.32	V
V_{CCAUX}	Auxiliary Supply Voltage for Bank 1, 2 and NVCM	–0.5	2.75	V
V_{CCIO}	I/O Driver Supply Voltage for Banks 0, 1, 2	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CC_DPHY} V_{CCA_DPHY} V_{CCPLL_DPHY} V_{CCMU_DPHY}	MIPI D-PHY Supply Voltages	–0.5	1.32	V
—	Voltage Applied on MIPI D-PHY Pins	–0.5	1.32	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature (TJ)	—	+125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

5.2. Recommended Operating Conditions

Table 5.2. Recommended Operating Conditions[1, 2]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V
V_{CCAUX}	Auxiliary Supply Voltage for Bank 1, 2 and NVCM	2.375	2.625	V
V_{CCIO}	I/O Driver Supply Voltage for Bank 0, 1, 2	1.14	3.465	V
T_{JIND}	Junction Temperature, Industrial Operation	–40	100	°C
D-PHY External Power Supply				
V_{CC_DPHYx}	Supply Voltage for D-PHY	1.14	1.26	V
V_{CCA_DPHYx}	Analog Supply Voltage for D-PHY	1.14	1.26	V
V_{CCPLL_DPHYx}	PLL Supply voltage for D-PHY	1.14	1.26	V
V_{CCMU_DPHY}	Supply for V_{CC_DPHY1}, V_{CCA_DPHY1} and V_{CCPLL_DPHY1} on the WLCSP36	1.14	1.26	V

Notes:

1. For Correct Operation, all supplies must be held in their valid operation range.
2. Like power supplies, must be tied together if they are at the same supply voltage. Follow the noise filtering recommendations in FPGA-TN-02013, CrossLink Hardware Checklist.

5.3. Preliminary Power Supply Ramp Rates

Table 5.3. Preliminary Power Supply Ramp Rates[1]

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies except V_{CCAUX}	0.6	10	V/ms

Note:

1. Assume monotonic ramp rates.

5.4. Preliminary Power-On-Reset Voltage Levels

Table 5.4. Preliminary Power-On-Reset Voltage Levels[1, 3, 4]

Symbol	Parameter		Min	Typ	Max	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	0.62	0.68	0.93	V
		V_{CCIO0}[2]	0.87	1.08	1.50	V
		V_{CCAUX}	0.90	—	1.53	V
V_{PORDN}	Power-On-Reset ramp down trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	—	—	0.79	V
		V_{CCIO0}[2]	—	—	1.50	V
		V_{CCAUX}	—	—	1.53	V

Notes:

1. These POR ramp up trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. Only V_{CCIO0} (Config Bank) has a Power-On-Reset ramp up trip point. All other VCCIOs do not have Power-On-Reset ramp up detection.
3. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.
4. Configuration starts after V_{CC}, V_{CCIO0} and V_{CCAUX} reach V_{PORUP}. For details, see $t_{REFRESH}$ time in Table 5.21 on page 38.

5.5. ESD Performance

Refer to the LIFMD Product Family Qualification Summary for complete qualification data, including ESD performance.

5.7. Preliminary CrossLink Supply Current

Over recommended operating conditions.

Table 5.6. Preliminary CrossLink Supply Current

Symbol	Parameter	Typ	Unit
Normal Operation[1]			
I_{CC}	Core Power Supply Current	7.17	mA
I_{CCPLL}	PLL Power Supply Current	0.05	mA
$I_{CCAUX25VPP}$	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	2.65	mA
I_{CCIOx}	Bank x Power Supply Current (per Bank)	0.06	mA
I_{CCA_DPHYx}	V_{CCA_DPHYx} Power Supply Current	8.33	mA
I_{CCPLL_DPHYx}	V_{CCPLL_DPHYx} Power Supply Current	1.31	mA
Standby Current[2]			
$I_{CCSTDBY}$	Core Power Supply Standby Current	2.73	mA
$I_{CCPLLSTDBY}$	PLL Power Supply Standby Current	—	mA
$I_{CCAUX25VPPSTDBY}$	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Standby Current	0.46	mA
$I_{CCIOSTDBY}$	Bank Power Supply Standby Current (per Bank)	0	mA
$I_{CCA\_DPHYxSTDBY}$	V_{CCA_DPHYx} Power Supply Standby Current	0.01	mA
$I_{CCPLL\_DPHYxSTDBY}$	V_{CCPLL_DPHYx} Power Supply Standby Current	0.01	mA
Sleep/Power Down Mode Current[3]			
I_{CC_SLEEP}	Core Power Supply Sleep Current	0.48	mA
I_{CCGPLL_SLEEP}	PLL Power Supply Current	0.05	mA
I_{CCAUX_SLEEP}	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	0.03	mA
I_{CCIOx_SLEEP}	Bank Power Supply Current (per Bank)	0.06	mA
$I_{CCPLL\_DPHY\_SLEEP}$	V_{CCPLL_DPHY} Power Supply Sleep Current	0.01	mA
$I_{CCA\_DPHY\_SLEEP}$	V_{CCA_DPHY} Power Supply Sleep Current	0.05	mA

Notes:

1. **Normal Operation**
   Typical design as defined in 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge section, under the following conditions:
   a. T_J = 25 °C, all power supplies at nominal voltages.
   b. Typical processed device in csfBGA81 package.
   c. To determine power for all other applications and operating conditions, use Power Calculator in Lattice Diamond design software
2. **Standby Operation**
   A typically processed device in csfBGA81 package with blank pattern programmed, under the following conditions:
   a. All outputs are tri-stated, all inputs are held at either V_{CCIO}, or GND.
   b. All clock inputs are at 0 MHz.
   c. T_J = 25 °C, all power supplies at nominal voltages.
   d. No pull-ups on I/O.
3. **Sleep/Power Down Mode**
   Typical design as defined in 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge section, under following conditions:
   a. Design is put into Sleep/Power Down Mode with user logic powers down D-PHY, and enters into Sleep Mode in PMU.
   b. T_J = 25 °C, all power supplies at nominal voltages.
   c. Typical processed device in csfBGA81 package.
4. **For ucfBGA64 package**
   a. V_{CCA_DPHY0} and V_{CCA_DPHY1} are tied together as V_{CC_DPHYX}.
   b. V_{CCPLL_DPHY0} and V_{CCPLL_DPHY1} are tied together as V_{CC_DPHYX}.
5. **For WLCS36 package**
   a. V_{CCGPLL} and V_{CCIO1} (Bank 1) are tied together to V_{CC}.
   b. V_{CCPLL_DPHY} and V_{CCA_DPHY} are tied together as V_{CCMU_DPHY}.
6. To determine the CrossLink start-up peak current, use the Power Calculator tool in the Lattice Diamond design software.

5.8. Preliminary Power Management Unit (PMU) Timing

Table 5.7. Preliminary PMU Timing[1]

Symbol	Parameter	Device	Max	Unit
$t_{PMUWAKE}$	Time for PMU to wake from Sleep mode	All Devices	1	ms

Note:

1. For details on PMU usage, refer to FPGA-TN-02018, Power Management and Calculation for CrossLink Devices.

5.9. sysI/O Recommended Operating Conditions

Table 5.8. sysI/O Recommended Operating Conditions[1]

Standard	V_{CCIO}		
	Min	Typ	Max
LVCMOS33/LVTTL33	3.135	3.30	3.465
LVCMOS25	2.375	2.50	2.625
LVCMOS18	1.710	1.80	1.890
LVCMOS12 (Output only)	1.140	1.20	1.260
subLDVS (Input only)	2.375	2.50	2.625
SLVS (Input only)[2]	2.375	2.50	2.625
LVDS	2.375	2.50	2.625
MIPI (Input only)	1.140	1.20	1.260

Note:

1. For input voltage compatibility, refer to FPGA-TN-02016, CrossLink sysI/O Usage Guide.
2. For SLVS/MIPI interface I/O placement, see the Programmable I/O Banks section.

5.10. Preliminary sysI/O Single-Ended DC Electrical Characteristics

Table 5.9. Preliminary sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL} (mA)	I_{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS33/ LVTTL33	–0.3	0.8	2.0	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	8	–8
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS25	–0.3	0.7	1.7	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	6	–6
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	4	–4
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS12 (Output only)	—	—	—	—	0.40	V_{CCIO} – 0.4	2	–2
					0.20	V_{CCIO} – 0.2	0.1	–0.1

5.11.2. Preliminary Hardened MIPI D-PHY I/Os

Table 5.11. Preliminary MIPI D-PHY

	Description	Min	Typ	Max	Unit
Receiver					
High Speed					
V_{CMRX}	Common-Mode Voltage HS Receive Mode	70	—	330	mV
V_{IDTH}	Differential Input High Threshold	—	—	70	mV
V_{IDTL}	Differential Input Low Threshold	−70	—	—	mV
V_{IHHS}	Single-ended Input High Voltage	—	—	460	mV
V_{ILHS}	Single-ended Input Low Voltage	−40	—	—	mV
$V_{TERM-EN}$	Single-ended Threshold for HS Termination Enable	—	—	450	mV
Z_{ID}	Differential Input Impedance	80	100	125	Ω
Low Power					
V_{IH}	Logic 1 Input Voltage	880	—	—	mV
V_{IL}	Logic 0 Input Voltage, not in ULP State	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 Input Voltage, in ULP State	—	—	300	mV
V_{HYST}	Input Hysteresis	25	—	—	mV
Transmitter					
High Speed					
V_{CMTX}	HS Transmit Static Common Mode Voltage	150	200	250	mV
V_{OD}	HS Transmit Differential Voltage	140	200	270	mV
V_{OHHS}	HS Output High Voltage	—	—	360	mV
Z_{OS}	Single-ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single-ended Output Impedance Mismatch	—	—	10	%
Low Power					
V_{OH}	Output High Level	1.1	1.2	1.3	V
V_{OL}	Output Low Level	−50	—	50	mV
Z_{OLP}	Output Impedance of LP Transmitter	110	—	—	Ω

5.13. Preliminary CrossLink External Switching Characteristics

Over recommended commercial operating conditions.

Table 5.13. Preliminary CrossLink External Switching Characteristics[4, 5]

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Clocks					
Primary Clock					
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	150	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	ns
t_{ISKEW_PRI}	Primary Clock Skew Within a Clock	—	—	450	ps
Edge Clock					
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	600	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	0.783	—	ns
t_{ISKEW_EDGE}	Edge Clock Skew Within a Bank	—	—	120	ps
Generic SDR Interface[1]					
General Purpose I/O Pin Parameters Using Clock Tree Without PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	6.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	—	–0.90	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.82	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	—	1.02	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	—	0	—	ns
General Purpose I/O Pin Parameters Using Clock Tree With PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	5.2	ns
t_{SU}	Clock to Data Setup – PIO Input Register	—	0.17	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.01	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	—	1.70	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	—	0	—	ns
Generic DDR Interfaces[2]					
Generic DDRX8 or DDRX4 I/O with Clock and Data Centered at General Purpose Pins (GDDRX8_RX/TX.ECLK.Centered or GDDRX4_RX/TX.ECLK.Centered)					
$t_{SU\_GDDRX4\_8}$	Input Data Set-Up Before CLK Rising and Falling edges	—	0.167	—	ns
$t_{HO\_GDDRX4\_8}$	Input Data Hold After CLK Rising and Falling edges	—	0.167	—	ns
$t_{DVB\_GDDRX4\_8}$	Output Data Valid Before CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	–0.120	—	ns+1/2UI
$t_{DVA\_GDDRX4\_8}$	Output Data Valid After CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	–0.120	—	ns+1/2UI
$f_{MAX\_GDDRX4\_8}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz

Table 5.13. Preliminary CrossLink External Switching Characteristics (*Continued*)

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Generic DDRX8 or DDRX4 I/O with Clock and Data Aligned at General Purpose Pins (GDDRX8_RX/TX.ECLK.Aligned or GDDRX4_RX/TX.ECLK.Aligned)					
$t_{DVA\_GDDRX4\_8}$	Input Data Valid After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s	—	0.188	ns
		Other Data Rates	—	–0.229	ns+1/2UI
$t_{DVE\_GDDRX4\_8}$	Input Data Hold After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s	0.646	—	ns
		Other Data Rates	0.229	—	ns+1/2UI
$t_{DIA\_GDDRX4\_8}$	Output Data Invalid After CLK Rising and Falling edges Output	—	—	0.120	ns
$t_{DIB\_GDDRX4\_8}$	Output Data Invalid Before CLK Output Rising and Falling edges	—	—	0.120	ns
$f_{MAX\_GDDRX4\_8}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz
General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing					
$t_{SU\_GDDRX\_MP}$	Input Data Set-Up Before CLK	—	0.167	—	ns
$t_{HO\_GDDRX\_MP}$	Input Data Hold After CLK	—	0.167	—	ns
$f_{MAX\_GDDRX\_MP}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz
Generic DDRX71 or DDRX141 Inputs (GDDRX71_RX.ECLK or GDDRX141_RX.ECLK)					
t_{RPBi_DVA}	Input Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.3	UI
		—	—	–0.222	ns+ (i+ 1/2)*UI
t_{RPBi_DVE}	Input Hold Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.7	—	UI
		—	0.222	—	ns+ (i+ 1/2)*UI
f_{MAX_RX71}	DDR71/DDR141 ECLK Frequency[3]	—	—	450	MHz
Generic DDRX71 Outputs with Clock and Data Aligned at Pin (GDDRX71_TX.ECLK)					
T_{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.143	ns+i*UI
T_{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	–0.143	—	ns+ (i+ 1)*UI
$T_{TPBi\_skew\_UI}$	Tx skew in UI	—	—	0.15	UI
f_{MAX_TX71}	DDR71 ECLK Frequency[3]	csfBGA81	—	525	MHz
		WLCSP36	—	500	MHz

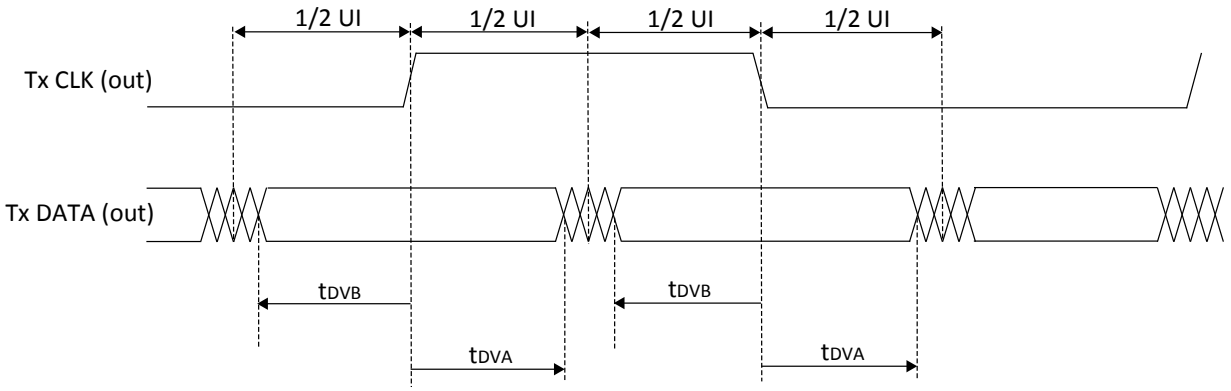


Figure 5.3. Transmit TX.CLK.Centered Output Waveforms

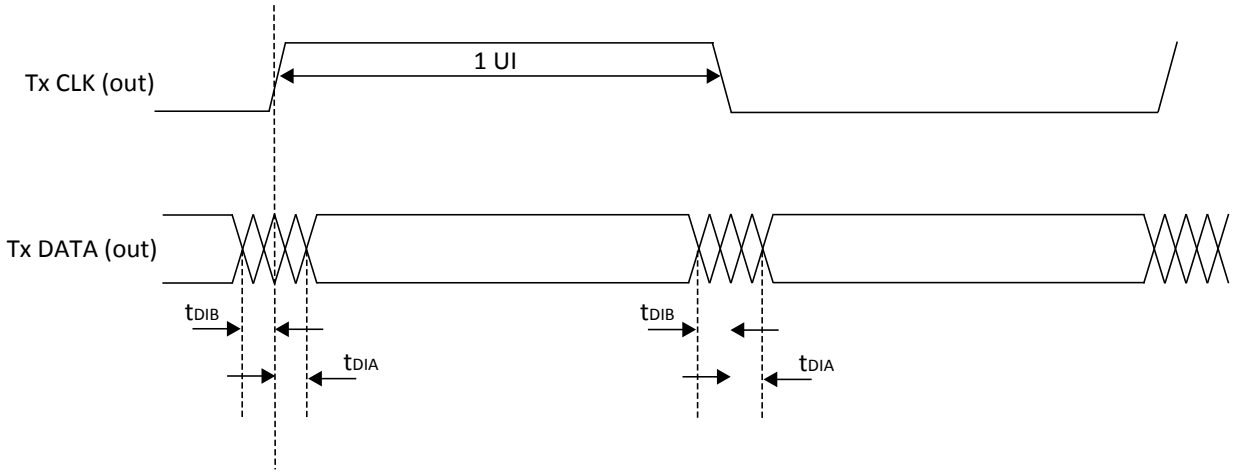


Figure 5.4. Transmit TX.CLK.Aligned Waveforms

5.18. CrossLink sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 5.20. CrossLink sysCONFIG Port Timing Specifications

Symbol	Parameter	Min	Max	Unit
All Configuration Mode				
t_{PRGM}	CRESETB LOW Pulse Accepted	145	—	ns
Slave SPI				
f_{CCLK}	SPI_SCK Input Clock Frequency	—	110	MHz
t_{STSU}	MOSI Setup Time	0.5	—	ns
t_{STH}	MOSI Hold Time	2.0	—	ns
t_{STCO}	SPI_SCK Falling Edge to Valid MISO Output	—	13.3	ns
t_{SCS}	Chip Select HIGH Time	42	—	ns
t_{SCSS}	Chip Select Setup Time	0.5	—	ns
t_{SCSH}	Chip Select Hold Time	0.5	—	ns
Master SPI				
f_{CCLK}	MCK Output Clock Frequency	—	52.8	MHz
I^2C*				
f_{MAX}	Maximum SCL Clock Frequency (Fast-Mode Plus	—	1	MHz

***Note**: Refer to the I^2C specification for timing requirements when configuring with I^2C port.

5.19. Preliminary SRAM Configuration Time from NVCM

Over recommended operating conditions.

Table 5.21. Preliminary SRAM Configuration Time from NVCM

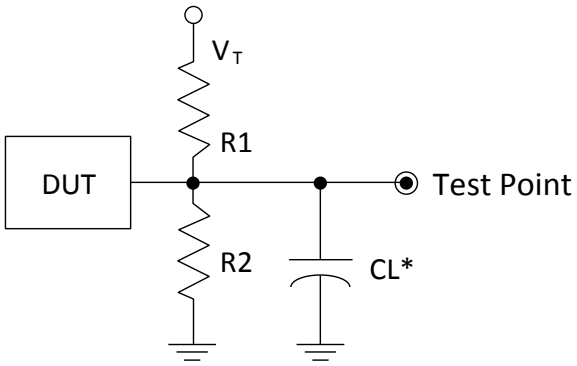
Symbol	Parameter	Typ	Unit
$t_{CONFIGURATION}$	POR to Device I/O Active[1]	83	ms

Note:

1. Before and during configuration, the I/Os are held in tristate with weak internal pullups enabled. I/Os are released to user functionality when the device has finished configuration.

5.20. Switching Test Conditions

Figure 5.6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 5.22.



*CL Includes Test Fixture and Probe Capacitance

Figure 5.6. Output Test Load, LVTTL and LVCMOS Standards

Table 5.22. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	$V_{OH} - 0.10$	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	$V_{OL} + 0.10$	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

ctfBGA80 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
F4	VCCIO0	0	—	—
F5	VCCIO1	1	—	—
F6	VCCIO2	2	—	—
F7	VCCIO2	2	—	—
F9	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F10	PB6B	2	—	Comp_OF_PB6A
G1	PB50	0	MOSI	—
G2	VSS	GND	—	—
G4	VCCIO1	1	—	—
G5	VSS	GND	—	—
G6	VCCGPLL	VCCGPLL	—	—
G7	VSSGPLL	GND	—	—
G9	PB2A	2	—	True_OF_PB2B
G10	PB2B	2	—	Comp_OF_PB2A
H1	PB52	0	SPI_SS/CSN/SCL	—
H2	CRESET_B	0	—	—
H9	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
H10	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
J1	PB53	0	SPI_SCK/MCK/SDA	—
J2	PB49	0	PMU_WKUPN/CDONE	—
J3	PB43D	1	—	Comp_OF_PB43C
J4	PB38D	1	—	Comp_OF_PB38C
J5	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
J6	PB29D	1	PCLKC1_1	Comp_OF_PB29C
J7	PB29A	1	PCLKT1_0	True_OF_PB29B
J8	PB16D	2	PCLKC2_1	Comp_OF_PB16C
J9	PB6D	2	—	Comp_OF_PB6C
J10	PB6C	2	—	True_OF_PB6D
K1	PB51	0	MISO	—
K2	PB47	0	PCLKT0_0/USER_SDA	—
K3	PB43C	1	—	True_OF_PB43D
K4	PB38C	1	—	True_OF_PB38D
K5	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
K6	PB29C	1	PCLKT1_1	True_OF_PB29D
K7	PB29B	1	PCLKC1_0	Comp_OF_PB29A
K8	PB16C	2	PCLKT2_1	True_OF_PB16D
K9	PB12D	2	—	Comp_OF_PB12C
K10	PB12C	2	—	True_OF_PB12D

6.4. csfBGA81 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
A2	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A3	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
A4	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
A5	VCCA_DPHY1	DPHY1	—	—
A6	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A7	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
A8	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
A9	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
B1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
B3	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
B4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
B5	GNDPLL_DPHYX	GND	—	—
B6	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B7	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
B8	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
B9	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
C1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
C2	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
C3	GNDA_DPHY1	DPHY1	—	—
C4	VCCPLL_DPHY1	DPHY1	—	—
C5	GND	GND	—	—
C6	VCCPLL_DPHY0	DPHY0	—	—
C7	GNDA_DPHY0	DPHY0	—	—
C8	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
C9	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
D1	PB34A	1	GR_PCLK1_0	True_OF_PB34B
D2	PB34B	1	—	Comp_OF_PB34A
D3	VCCA_DPHY1	DPHY1	—	—
D4	GND	GND	—	—
D5	VCCAUX	VCCAUX	—	—
D6	GND	GND	—	—
D7	VCCA_DPHY0	DPHY0	—	—
D8	PB16B	2	PCLKC2_0	Comp_OF_PB16A
D9	PB16A	2	PCLKT2_0	True_OF_PB16B
E1	PB38A	1	—	True_OF_PB38B
E2	PB38B	1	—	Comp_OF_PB38A
E3	VCC	VCC	—	—
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCCIO2	2	—	—

References

For more information, refer to the following technical notes:

- FPGA-TN-02012, CrossLink High-Speed I/O Interface
- FPGA-TN-02013, CrossLink Hardware Checklist
- FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide
- FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide
- FPGA-TN-02016, CrossLink sysI/O Usage Guide
- FPGA-TN-02017, CrossLink Memory Usage Guide
- FPGA-TN-02018, Power Management and Calculation for CrossLink Devices
- FPGA-TN-02019, CrossLink I2C Hardened IP Usage Guide
- FPGA-TN-02020, Advanced CrossLink I2C Hardened IP Reference Guide

For package information, refer to the following technical notes:

- TN1074, PCB Layout Recommendations for BGA Packages
- TN1076, Solder Reflow Guide for Surface Mount Devices
- TN1242, Wafer-Level Chip-Scale Package Guide
- Thermal Management
- Package Diagrams

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- MIPI Standards (D-PHY): www.mipi.org

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
March 2017	1.1	Updated I/O placements on banks containing MIPI interface in Programmable I/O Banks section. Updated DC and Switching Characteristics section: • Updated Table 5.4. Preliminary Power-On-Reset Voltage Levels1, [3, 4], added row of V_{PORDN} • Added Note 5 to Table 5.5. Preliminary DC Electrical Characteristics • Updated Table 5.6. Preliminary CrossLink Supply Current, added notes • Updated max values of V_{THD} and $V_{THD(subLVDS)}$ in Table 5.10. LVDS/subLVDS1/SLVS1, [2] • Maximum input frequency values of subLVDS and SLVS are TBD in Table 5.12. Preliminary CrossLink Maximum I/O Buffer Speed • Updated Table 5.13. Preliminary CrossLink External Switching Characteristics4, [5] • Updated min values of t_{SU_MIPIX4} and t_{HO_MIPIX4} in Table 5.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s) and Table 5.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s) • Updated Table 5.20. CrossLink sysCONFIG Port Timing Specifications • Updated Table 5.21. Preliminary SRAM Configuration Time from NVCM Updated Pinout Information section Updated CrossLink Part Number Description
July 2016	1.0	Updated document numbers.
May 2016	1.0	First preliminary release.