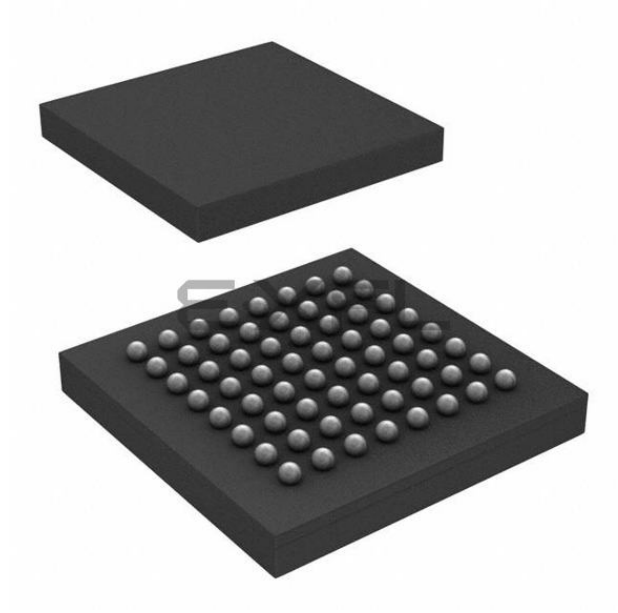
Lattice Semiconductor Corporation - LIF-MD6000-6UMG64I Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1484
Number of Logic Elements/Cells	5936
Total RAM Bits	184320
Number of I/O	29
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	64-VFBGA
Supplier Device Package	64-ucfBGA (3.5x3.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lif-md6000-6umg64i

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2.2. 1:2 MIPI DSI Display Interface Bridge

Figure 2.2 shows the block diagram for the 1:2 MIPI DSI display interface bridge. This solution duplicates the display output from single application processor DSI output to two different DSI displays.

Table 2.2 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting any input encoding, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. The solution can be customized to split the input image, or perform additional bridging operations. For details, refer to FPGA-IPUG-02001, 1:2 and 1:1 MIPI DSI Display Interface Bridge Soft IP User Guide.

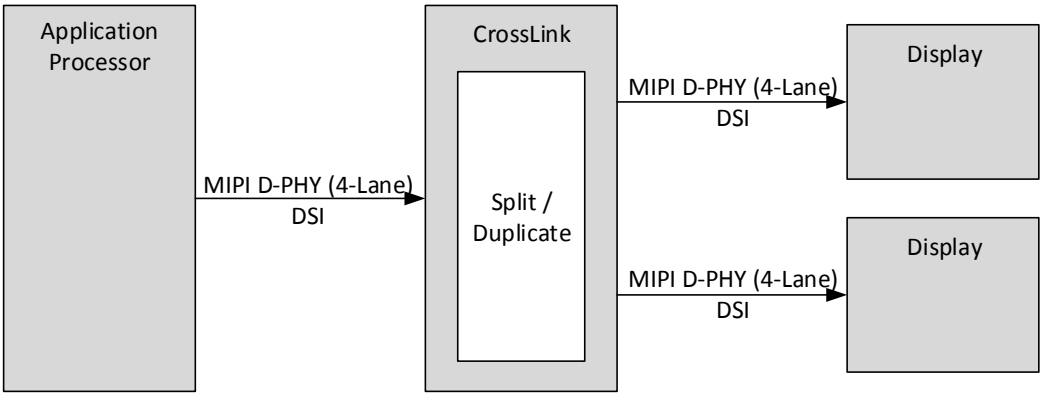


Figure 2.2. 1:2 MIPI DSI Display Interface Bridge

Table 2.2. 1:2 MIPI DSI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Split/Duplicate Image
Output Type	2 x 1080p60, 24-bit RGB 2 x 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~140 mW
Device I/O Used	10 Programmable I/O; 2 x Hard D-PHY Quads
Fabric Resources Used	80% of LUT4; ~80% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.5. CMOS to MIPI DSI Display Interface Bridge

Figure 2.5 shows the block diagram for the CMOS to MIPI DSI display interface bridge. This solution bridges the CMOS parallel output from the application processor to a DSI display input.

Table 2.5 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

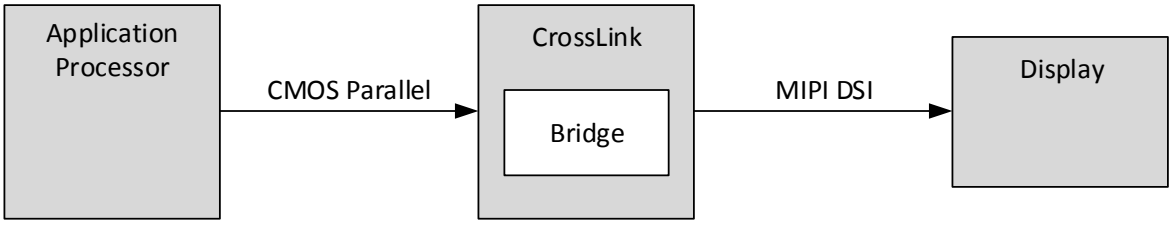


Figure 2.5. CMOS to MIPI DSI Display Interface Bridge

Table 2.5. CMOS to MIPI DSI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB CMOS Parallel @ 148.5 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~80 mW
Device I/O Used	28 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Figure 2.6 shows the block diagram for the CMOS to MIPI CSI-2 Image Sensor Interface Bridge. This solution bridges the CMOS parallel output from an image sensor to a CSI-2 input of an application processor.

Table 2.6 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

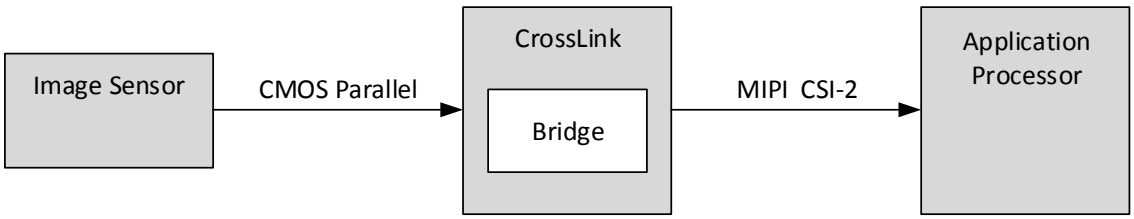


Figure 2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Table 2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 12-bit RAW CMOS Parallel @ 74.25 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 12-bit RAW 4-Lane MIPI D-PHY @ ~450 Mb/s per lane
Additional System Functions	I^2C for Camera Configuration GPIO for image sensor reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~75 mW
Device I/O Used	16 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.7. MIPI DSI to CMOS Display Interface Bridge

Figure 2.7 shows the block diagram for the MIPI DSI to CMOS display interface bridge. This solution bridges the MIPI DSI output from the application processor to CMOS parallel display input.

Table 2.7 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting multiple pixel formats and data rates up to 1.5 Gb/s per lane input and up to 150 MHz CMOS parallel output. For details, refer to FPGA-IPUG-02004, MIPI D-PHY to CMOS Interface Bridge Soft IP User Guide.

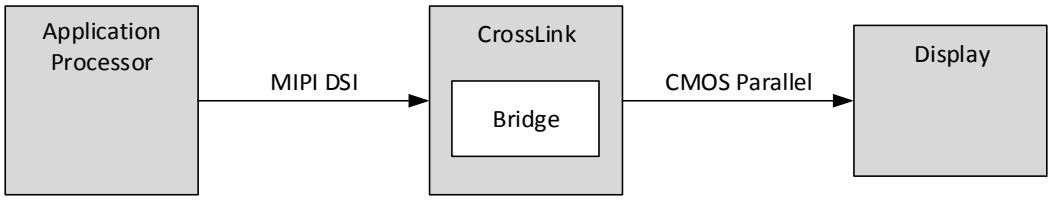


Figure 2.7. MIPI DSI to CMOS Display Interface Bridge

Table 2.7. MIPI DSI to CMOS Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 24-bit RGB CMOS Parallel @ 148.5 MHz
Additional System Functions	Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~80 mW
Device I/O Used	28 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	15% of LUT4; ~15% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

4.4.2. Power Management Unit

The embedded Power Management Unit (PMU) allows low-power Sleep State of the device. Figure 4.3 shows the block diagram of the PMU IP.

When instantiated in the design, PMU is always on, and uses the low-speed clock from oscillator of the device to perform its operations.

The typical use case for the PMU is through a user implemented state machine that controls the sleep and wake up of the device. The state machine implemented in the FPGA fabric identifies when the device needs to go into sleep mode, issues the command through PMU's FPGA fabric interface, assigns the parameters for sleep (time to wake up and so on) and issues Sleep command.

The device can be woken up externally using the PMU Wake-Up (USRWKUP) pin, or from the PMU Watch Dog Timer expiry or from I2C0 (address decoding detection or FIFO full in one of hardened I^2C).

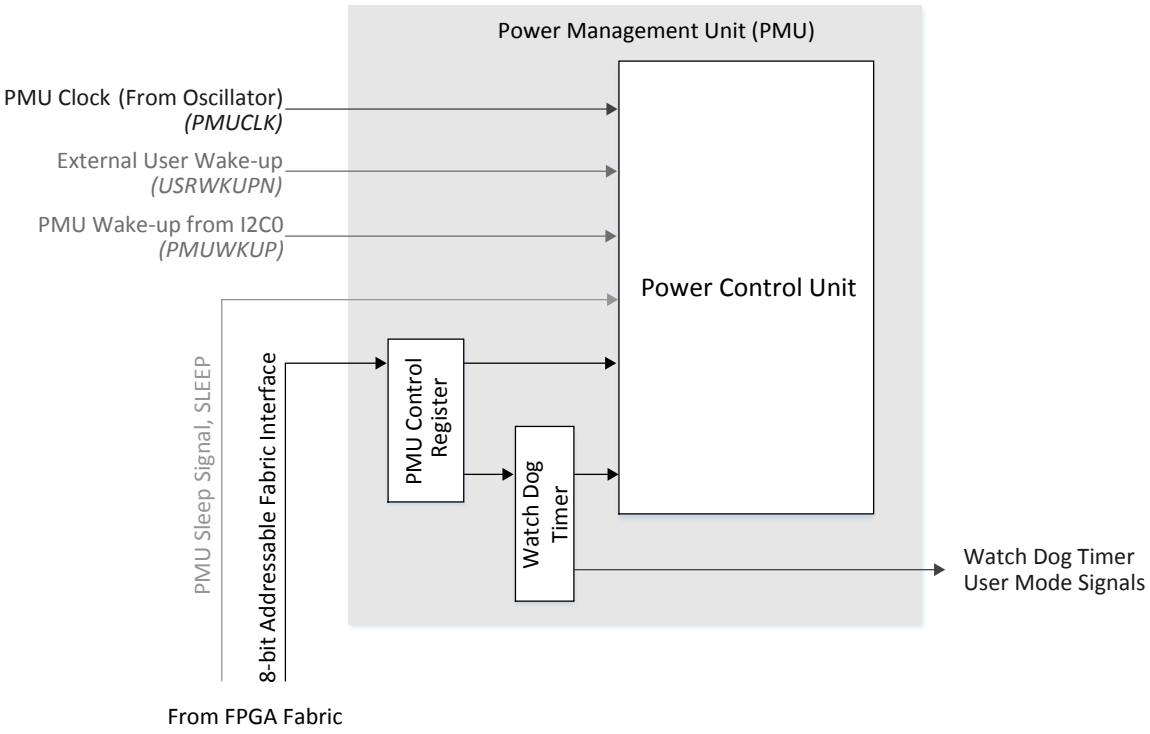


Figure 4.3. CrossLink MIPI D-PHY Block

4.4.2.1. PMU State Machine

PMU can place the device in two mutually exclusive states – Normal State and Sleep State. Figure 4.4 on the next page shows the PMU State Machine triggers for transition from one state to the other.

- Normal state – All elements of the device are active to the extent required by the design. In this state, the device is at fully active and performing as required by the application.
  Note that the power consumption of the device is highest in this state.
- Sleep state – The device is power gated such that the device is not operational. The configuration of the device and the EBR contents are retained; thus in Sleep mode, the device does not lose configuration SRAM and EBR contents. When it transitions to Normal state, device operates with these contents preserved.
  The PMU is active along with the associated GPIOs.
  The power consumption of the device is lowest in this state. This helps reduce the overall power consumption for the device.

5.3. Preliminary Power Supply Ramp Rates

Table 5.3. Preliminary Power Supply Ramp Rates[1]

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies except V_{CCAUX}	0.6	10	V/ms

Note:

1. Assume monotonic ramp rates.

5.4. Preliminary Power-On-Reset Voltage Levels

Table 5.4. Preliminary Power-On-Reset Voltage Levels[1, 3, 4]

Symbol	Parameter		Min	Typ	Max	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	0.62	0.68	0.93	V
		V_{CCIO0}[2]	0.87	1.08	1.50	V
		V_{CCAUX}	0.90	—	1.53	V
V_{PORDN}	Power-On-Reset ramp down trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	—	—	0.79	V
		V_{CCIO0}[2]	—	—	1.50	V
		V_{CCAUX}	—	—	1.53	V

Notes:

1. These POR ramp up trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. Only V_{CCIO0} (Config Bank) has a Power-On-Reset ramp up trip point. All other VCCIOs do not have Power-On-Reset ramp up detection.
3. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.
4. Configuration starts after V_{CC}, V_{CCIO0} and V_{CCAUX} reach V_{PORUP}. For details, see $t_{REFRESH}$ time in Table 5.21 on page 38.

5.5. ESD Performance

Refer to the LIFMD Product Family Qualification Summary for complete qualification data, including ESD performance.

5.6. Preliminary DC Electrical Characteristics

Over recommended operating conditions.

Table 5.5. Preliminary DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4, 5]	Input or I/O Leakage	$0 \le V_{IN} \le V_{CCIO}$	−10	—	+10	µA
I_{PU}[4]	Internal Pull-Up Current	V_{CCIO} = 1.2 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−2.7	—	−8	µA
		V_{CCIO} = 1.8 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−3	—	−31	µA
		V_{CCIO} = 2.5 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−8	—	−72	µA
		V_{CCIO} = 3.3 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−11	—	−128	µA
C_1[2]	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf
C_2[2]	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf
V_{HYST}[3]	Hysteresis for Single-Ended Inputs	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	200	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A = 25 °C, f = 1.0 MHz.
3. Hysteresis is not available for V_{CCIO} = 1.2 V.
4. Weak pull-up setting. Programmable pull-up resistors on Bank 0 will see higher current. Refer to FPGA-TN-02016, CrossLink sysI/O Usage Guide for details on programmable pull-up resistors.
5. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO}, or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

Table 5.13. Preliminary CrossLink External Switching Characteristics (*Continued*)

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Generic DDRX141 Outputs with Clock and Data Aligned at Pin (GDDRX141_TX.ECLK)					
T_{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	All Devices	—	0.125	ns+i*UI
T_{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	All Devices	–0.125	—	ns+(i+ 1)*UI
$T_{TPBi\_skew\_UI}$	TX skew in UI	All Devices	—	0.15	UI
f_{MAX_TX141}	DDR141 ECLK Frequency[3]	csfBGA81	—	600	MHz
		WLCSP36	—	500	MHz

Notes:
1. General I/O timing numbers based on LVCMOS 2.5, 0 pf load.
2. Generic DDRX8, DDRX71 and DDRX141 timing numbers based on LVDS I/O.
3. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
4. These numbers are generated using best case PLL located.
5. All numbers are generated with the Lattice Diamond design software.

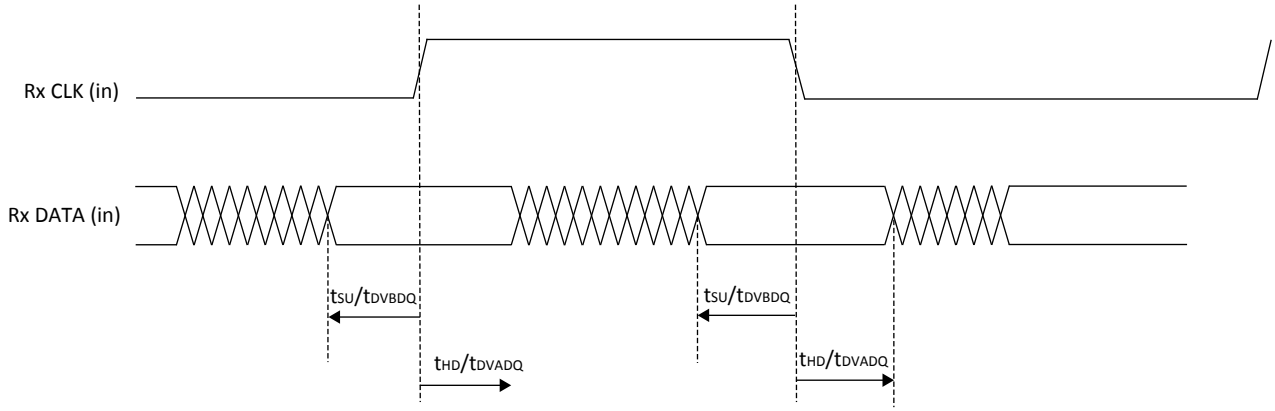


Figure 5.1. Receiver RX.CLK.Centered Waveforms

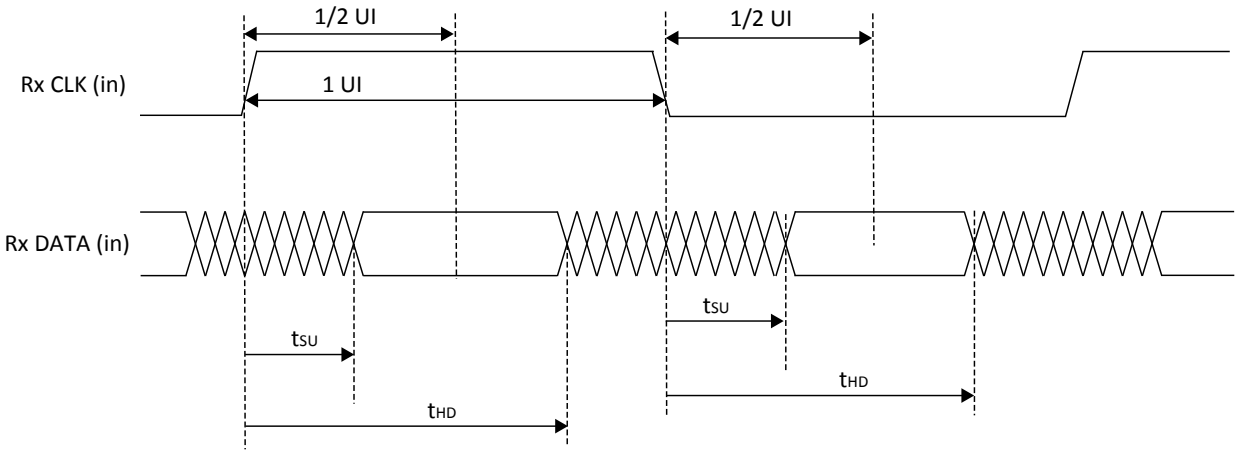


Figure 5.2. Receiver RX.CLK.Aligned Input Waveforms

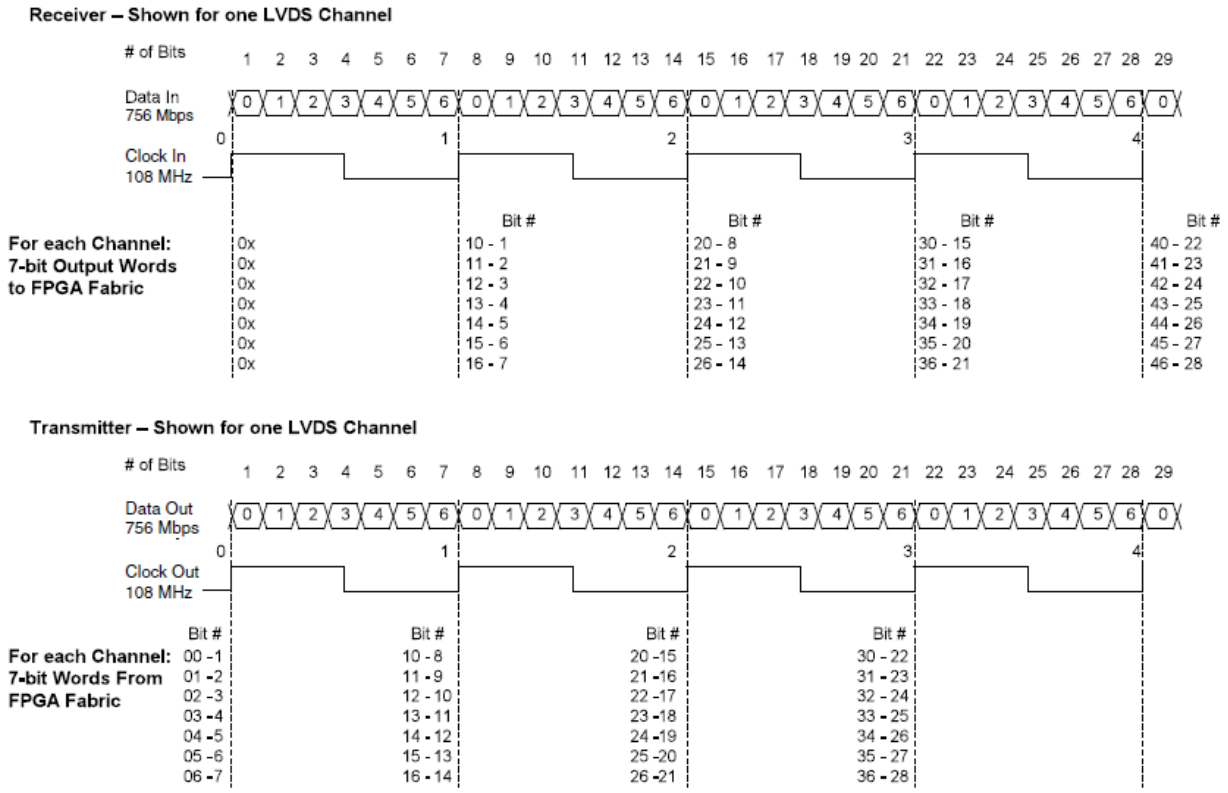


Figure 5.5. DDRX71, DDRX141 Video Timing Waveforms

5.14. Preliminary sysCLOCK PLL Timing

Over recommended operating conditions.

Table 5.14. Preliminary sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Unit
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	10	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	4.6875	600	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH4}	Output Phase Accuracy	—	–5	5	%
t_{OPJIT}[1]	Output Clock Period Jitter[3]	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter[3]	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.05	UIPP
	Output Clock Phase Jitter	$f_{PFD} > 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.05	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
t_{LOCK}[2]	PLL Lock-in Time	—	—	1	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	500	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns

Notes:

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} \geq 10$ MHz. For $f_{PFD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

5.15. Hardened MIPI D-PHY Performance

Table 5.15. 1500 Mb/s MIPI_DPHY_X8_RX/TX Timing Table (1500 Mb/s > MIPI D-PHY Data Rate > 1200 Mb/s)[1]

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX8}	Input Data Setup before CLK	0.133	—	ns
t_{HO_MIPIX8}	Input Data Hold after CLK	0.133	—	ns
t_{DVB_MIPIX8}	Output Data Valid before CLK Output	0.200	—	ns
t_{DVA_MIPIX8}	Output Data Valid after CLK Output	0.200	—	ns

Note:

1. For WLCSP36 package, the MIPI D-PHY f_{max} is 1200 Mb/s, for other packages, f_{max} is 1500 Mb/s.

Table 5.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s)

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX4}	Input Data Setup before CLK	0.150	—	ns
t_{HO_MIPIX4}	Input Data Hold after CLK	0.150	—	ns
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.250	—	ns
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.250	—	ns

Table 5.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s)

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX4}	Input Data Setup before CLK	0.167	—	ns
t_{HO_MIPIX4}	Input Data Hold after CLK	0.167	—	ns
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.350	—	ns
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.350	—	ns

5.16. Preliminary Internal Oscillators (HFOSC, LFOSC)

Table 5.18. Preliminary Internal Oscillators

Parameter	Parameter Description	Min	Typ	Max	Unit
f_{CLKHF}	HFOSC CLKK Clock Frequency	43.2	48	52.8	MHz
f_{CLKLF}	LFOSC CLKK Clock Frequency	9	10	11	kHz
DCH_{CLKHF}	HFOSC Duty Cycle (Clock High Period)	45	—	55	%
DCH_{CLKLF}	LFOSC Duty Cycle (Clock High Period)	45	—	55	%

5.17. Preliminary User I²C[1]

Table 5.19. Preliminary User I²C[1]

Symbol	Parameter	STD Mode		FAST Mode		FAST Mode Plus[2]		Units
		Min	Max	Min	Max	Min	Max	
f_{scl}	SCL Clock Frequency	—	100	—	400	—	1000[2]	kHz

Notes:

1. Refer to the I²C Specification for timing requirements.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I²C bus. Internal pull up may not be sufficient to support the maximum speed.

5.18. CrossLink sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 5.20. CrossLink sysCONFIG Port Timing Specifications

Symbol	Parameter	Min	Max	Unit
All Configuration Mode				
t_{PRGM}	CRESETB LOW Pulse Accepted	145	—	ns
Slave SPI				
f_{CCLK}	SPI_SCK Input Clock Frequency	—	110	MHz
t_{STSU}	MOSI Setup Time	0.5	—	ns
t_{STH}	MOSI Hold Time	2.0	—	ns
t_{STCO}	SPI_SCK Falling Edge to Valid MISO Output	—	13.3	ns
t_{SCS}	Chip Select HIGH Time	42	—	ns
t_{SCSS}	Chip Select Setup Time	0.5	—	ns
t_{SCSH}	Chip Select Hold Time	0.5	—	ns
Master SPI				
f_{CCLK}	MCK Output Clock Frequency	—	52.8	MHz
I^2C*				
f_{MAX}	Maximum SCL Clock Frequency (Fast-Mode Plus	—	1	MHz

***Note**: Refer to the I^2C specification for timing requirements when configuring with I^2C port.

5.19. Preliminary SRAM Configuration Time from NVCM

Over recommended operating conditions.

Table 5.21. Preliminary SRAM Configuration Time from NVCM

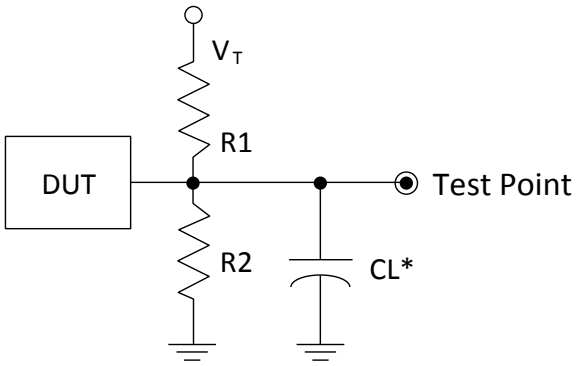
Symbol	Parameter	Typ	Unit
$t_{CONFIGURATION}$	POR to Device I/O Active[1]	83	ms

Note:

1. Before and during configuration, the I/Os are held in tristate with weak internal pullups enabled. I/Os are released to user functionality when the device has finished configuration.

5.20. Switching Test Conditions

Figure 5.6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 5.22.



*CL Includes Test Fixture and Probe Capacitance

Figure 5.6. Output Test Load, LVTTL and LVCMOS Standards

Table 5.22. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	$V_{OH} - 0.10$	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	$V_{OL} + 0.10$	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

ctfBGA80 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
F4	VCCIO0	0	—	—
F5	VCCIO1	1	—	—
F6	VCCIO2	2	—	—
F7	VCCIO2	2	—	—
F9	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F10	PB6B	2	—	Comp_OF_PB6A
G1	PB50	0	MOSI	—
G2	VSS	GND	—	—
G4	VCCIO1	1	—	—
G5	VSS	GND	—	—
G6	VCCGPLL	VCCGPLL	—	—
G7	VSSGPLL	GND	—	—
G9	PB2A	2	—	True_OF_PB2B
G10	PB2B	2	—	Comp_OF_PB2A
H1	PB52	0	SPI_SS/CSN/SCL	—
H2	CRESET_B	0	—	—
H9	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
H10	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
J1	PB53	0	SPI_SCK/MCK/SDA	—
J2	PB49	0	PMU_WKUPN/CDONE	—
J3	PB43D	1	—	Comp_OF_PB43C
J4	PB38D	1	—	Comp_OF_PB38C
J5	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
J6	PB29D	1	PCLKC1_1	Comp_OF_PB29C
J7	PB29A	1	PCLKT1_0	True_OF_PB29B
J8	PB16D	2	PCLKC2_1	Comp_OF_PB16C
J9	PB6D	2	—	Comp_OF_PB6C
J10	PB6C	2	—	True_OF_PB6D
K1	PB51	0	MISO	—
K2	PB47	0	PCLKT0_0/USER_SDA	—
K3	PB43C	1	—	True_OF_PB43D
K4	PB38C	1	—	True_OF_PB38D
K5	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
K6	PB29C	1	PCLKT1_1	True_OF_PB29D
K7	PB29B	1	PCLKC1_0	Comp_OF_PB29A
K8	PB16C	2	PCLKT2_1	True_OF_PB16D
K9	PB12D	2	—	Comp_OF_PB12C
K10	PB12C	2	—	True_OF_PB12D

csfBGA81 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
E7	PB12B	2	GPLLC2_0	Comp_OF_PB12A
E8	PB6B	2	—	Comp_OF_PB6A
E9	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F1	PB50	0	MOSI	—
F2	PB48	0	PCLKT0_1/USER_SCL	—
F3	VCCIO1	1	—	—
F4	GND	GND	—	—
F5	GNDGPLL	GND	—	—
F6	VCCIO2	2	—	—
F7	PB12A	2	GPLLT2_0	True_OF_PB12B
F8	PB2B	2	—	Comp_OF_PB2A
F9	PB2A	2	—	True_OF_PB2B
G1	PB52	0	SPI_SS/CSN/SCL	—
G2	CRESET_B	0	—	—
G3	VCCIO0	0	—	—
G4	VCCIO1	1	—	—
G5	VCCGPLL	VCCGPLL	—	—
G6	PB29B	1	PCLKC1_0	Comp_OF_PB29A
G7	PB29A	1	PCLKT1_0	True_OF_PB29B
G8	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
G9	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
H1	PB53	0	SPI_SCK/MCK/SDA	—
H2	PB49	0	PMU_WKUPN/CDONE	—
H3	PB43D	1	—	Comp_OF_PB43C
H4	PB38D	1	—	Comp_OF_PB38C
H5	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
H6	PB29D	1	PCLKC1_1	Comp_OF_PB29C
H7	PB16D	2	PCLKC2_1	Comp_OF_PB16C
H8	PB6D	2	—	Comp_OF_PB6C
H9	PB6C	2	—	True_OF_PB6D
J1	PB51	0	MISO	—
J2	PB47	0	PCLKT0_0/USER_SDA	—
J3	PB43C	1	—	True_OF_PB43D
J4	PB38C	1	—	True_OF_PB38D
J5	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
J6	PB29C	1	PCLKT1_1	True_OF_PB29D
J7	PB16C	2	PCLKT2_1	True_OF_PB16D
J8	PB12D	2	—	Comp_OF_PB12C
J9	PB12C	2	—	True_OF_PB12D