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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1484
Number of Logic Elements/Cells	5936
Total RAM Bits	184320
Number of I/O	17
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP (2.54x2.59)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lif-md6000-6uwg36itr

Contents

2. Application Examples

2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge

Figure 2.1 shows the block diagram for the 2:1 MIPI CSI-2 image sensor aggregator bridge. This solution merges image outputs from multiple sensors into a single CSI-2 output to an application processor.

Table 2.1 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting any input encoding, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. Up to 8 image sensor inputs can be aggregated, depending on data rate and number of lanes. For details, refer to FPGA-IPUG-02002, 2:1 MIPI CSI-2 Bridge Soft IP User Guide.

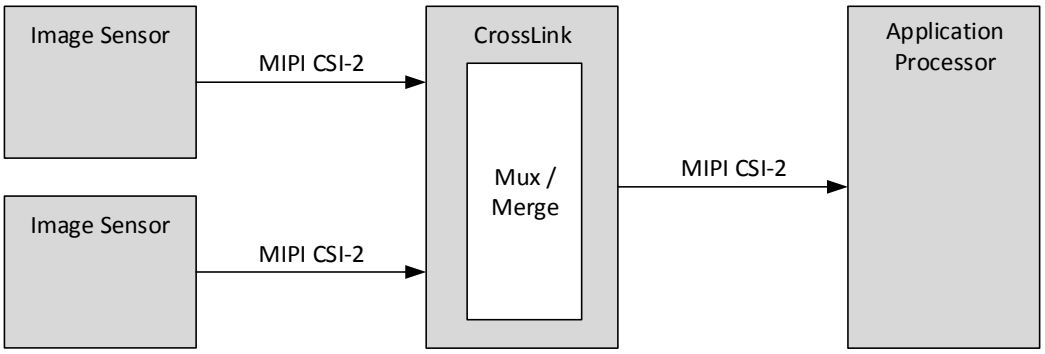


Figure 2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge

Table 2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge Overview

Application Example Details	
Input Type	2 x 1080p60, 12-bit RAW 2 x 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Programmable Fabric Operation(s)	Merge Image Sensor Outputs with no Frame drop Mux/Merge in flexible combinations
Output Type	1 x 1080p60, 12-bit RAW 1 x 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Additional System Functions	Support for I²C Bridge/Mux for Camera Configuration GPIO for image sensor sync and reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~55 mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~85% of LUT4; ~100% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.3. FPD-Link/OpenLDI LVDS to MIPI DSI Display Interface Bridge

Figure 2.3 shows the block diagram for the FPD-Link/OpenLDI LVDS to MIPI DSI display interface bridge. This solution bridges the single or dual-channel FPD-Link/OpenLDI LVDS display output from the application processor to a MIPI DSI input display.

Table 2.3 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting both RGB666 and RGB888, variable number of LVDS data lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02005, OpenLDI/FPD-Link/LVDS to MIPI DSI Interface Bridge Soft IP User Guide.

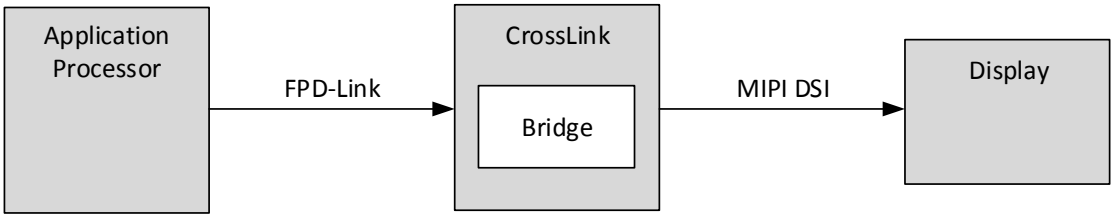


Figure 2.3. FPD-Link/OpenLDI LVDS to MIPI DSI Display Interface Bridge

Table 2.3. FPD-Link/OpenLDI LVDS to MIPI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 2 Channels (2 x 4 Data Lanes and 2 x 1 Clock Lane) @ 74.25 MHz FPD-Link Clock
Programmable Fabric Operation(s)	Bridge
Output Type	1 x 1080p60, 24-bit RGB 1 x 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	TBD mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~50% of LUT4; ~60% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.5. CMOS to MIPI DSI Display Interface Bridge

Figure 2.5 shows the block diagram for the CMOS to MIPI DSI display interface bridge. This solution bridges the CMOS parallel output from the application processor to a DSI display input.

Table 2.5 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

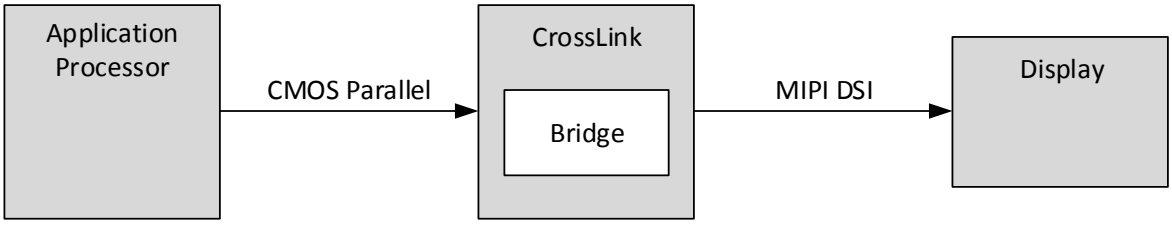


Figure 2.5. CMOS to MIPI DSI Display Interface Bridge

Table 2.5. CMOS to MIPI DSI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB CMOS Parallel @ 148.5 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~80 mW
Device I/O Used	28 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge

Figure 2.8 shows the block diagram for the MIPI DSI to CMOS display interface bridge. This solution bridges the MIPI DSI output from the application processor to CMOS parallel display input.

Table 2.8 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting multiple pixel formats and data rates up to 1.5 Gb/s per lane input and up to 150 MHz CMOS parallel output. For details, refer to FPGA-IPUG-02004, MIPI D-PHY to CMOS Interface Bridge Soft IP User Guide.

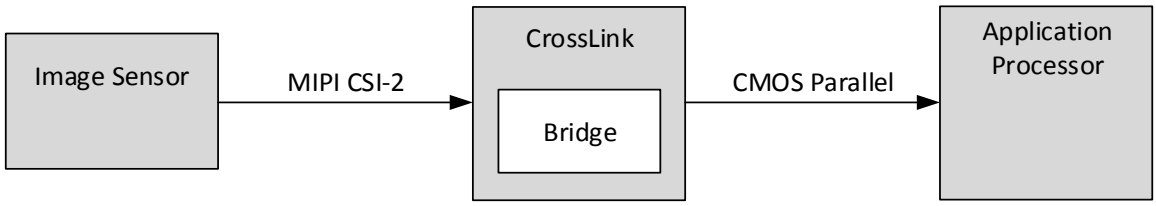


Figure 2.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge

Table 2.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	1080p60, RAW12 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, RAW12 CMOS Parallel @ 74.25 MHz
Additional System Functions	I^2C for Camera Configuration GPIO for image sensor reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	60 mW
Device I/O Used	16 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	15% of LUT4; ~15% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

Figure 2.9 shows the block diagram for a SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge. This solution bridges from an image sensor SubLVDS output to CSI-2 output to an application processor.

Table 2.9 provides additional details for a specific application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting RAW10 or RAW12 pixel width, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02006, SubLVDS to MIPI CSI-2 IP Image Sensor Interface Bridge Soft IP User Guide.

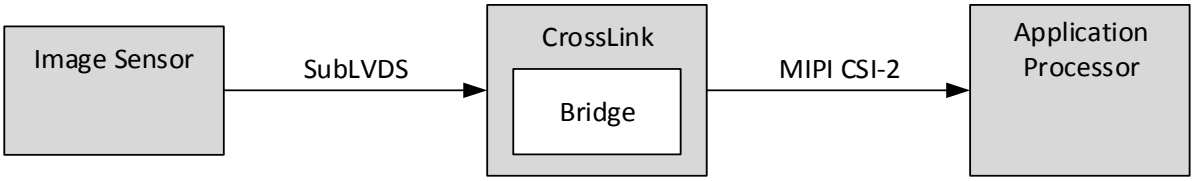


Figure 2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

Table 2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	4k2k@64.7fps, RAW10 SubLVDS 10 data lane @ 600 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	4k2k@64.7fps, RAW10 CSI-2 over 4-Lane MIPI D-PHY @ 1.5 Gb/s per lane
Additional System Functions	Image Frame Control GPIO for reset and power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~130 mW
Device I/O Used	22 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	80% of LUT4; ~60% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

3. Product Feature Summary

Table 3.1 lists CrossLink device information and packages.

Table 3.1. CrossLink Feature Summary

Device	**CrossLink**
LUTs	5936
sysMEM Blocks (9 kb)	20
Embedded Memory (kb)	180
Distributed RAM Bits (kb)	47
General Purpose PLL	1
NVCM	Yes
Embedded I^2C	2
Oscillator (10 KHz)	1
Oscillator (48 MHz)	1
Hardened MIPI D-PHY	2[1, 2]
Packages	**I/O**
36 WLCSP[2] (2.535 × 2.583 mm^2, 0.6 mm)	17
64 ucfBGA (3.5 × 3.5 mm^2, 1 mm)	29
80 ctfBGA (6.5 x 6.5 mm^2, 1 mm)	36
81 csfBGA (4.5 × 4.5 mm^2, 1 mm)	37

Notes:

1. Additional D-PHY Rx interfaces are available using programmable I/O.
2. Only one Hardened D-PHY is available in 36 WLCSP package.

4.1. MIPI D-PHY Blocks

The top side of the device includes two hard MIPI D-PHY quads. The D-PHY can be configured to support both camera interface (CSI-2) and display interface (DSI) applications. Below is a summary of the features supported by the hard D-PHY quads. Refer to FPGA-TN-02012, CrossLink High-Speed I/O Interface for more information on the Hard D-PHY quads.

- Transmit and Receive compliant to D-PHY Revision 1.1
- High-Speed (HS) and Low-Power (LP) mode support (including built-in contention detect)
- Up to 6 Gb/s per quad (1500 Mb/s data rate per lane)
- Dedicated PLL for Transmit Frequency Synthesis
- Dedicated Serializer and De-Serializer blocks for fabric interfacing
- Supports continuous clock mode or low power clock mode

Lattice Semiconductor provides a set of pre-engineered IP modules which include the full implementation and control of the hard D-PHY blocks for the examples in Application Examples section on page 7, enabling designers to focus on unique aspects of their design.

4.2. Programmable I/O Banks

CrossLink devices provide programmable I/O which can be used to interface to a variety of external standards. The I/O features are summarized below, and described in detail in FPGA-TN-02012, CrossLink High-Speed I/O Interface and FPGA-TN-02016, CrossLink sysI/O Usage Guide. The programmable LVDS/CMOS I/O (Banks 1 and 2) are described below, while the CMOS GPIO (bank 0) and hard D-PHY quads are described separately.

Programmable LVDS/CMOS I/O (Bank 1 and 2) features:

- Built-in support for the following differential standards
  - LVDS – Tx and Rx
  - SLVS – Rx
  - SubLVDS – Rx
  - MIPI – Rx (both LP and HS receive on a single differential pair)
- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs)
  - LVTTL33
- Independent voltage levels per bank based on VCCIO supply
- Input/output gearboxes per LVDS pair supporting several ratios for video interface applications
  - DDRX1, DDRX2, DDRX4, DDRX8 and DDRX71, DDRX141
  - Programmable delay cells to support edge-aligned and center-aligned interfaces
- Programmable differential termination (~ 100 Ω) with dynamic enable control
- Tri-state control for output
- Input/output register blocks
- Single-ended standards support open-drain and programmable input hysteresis
- Optional weak pull-up resistors

To ensure the MIPI Rx interface implemented in FPGA fabric using Programmable I/Os runs in an optimal environment, follow this guideline of assigning I/Os to the bank for the MIPI Rx inputs:

- When an SLVS/MIPI Rx interface is placed in Bank 1 or 2, do not place both Banks 1 and 2 with LVCMOS outputs in these 2 banks.

- Four Edge Clocks for high-speed DDR interfaces
  - 2 per Programmable I/O bank
  - Source from PCLK pins, PLL or DLL blocks
  - Programmable Clock divider per Edge Clock
  - Delay primitives for 90 degree phase shifting of clock/data (DDRDLL, DLLDEL)
- Dynamic Clock Control
  - Fabric control to disable clock nets for power savings
- Dynamic Clock Select
  - Smart clock multiplexer with two independent inputs and glitchless output support
- Two On-Chip Oscillators
  - Always-on Low Frequency (LFCLKOUT) with nominal frequency of 10 kHz
  - High-Frequency (HFCLKOUT) with nominal frequency of 48 MHz, programmable output dividers, and dynamic enable control

4.3.3. Embedded Block RAM Overview

CrossLink devices also contain sysMEM Embedded Block RAM (EBR). The EBR consists of a 9 kB RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Supported modes and other general information on the EBR are listed below. For details, refer to FPGA-TN-02017, CrossLink Memory Usage Guide.

- Support for different memory configurations
  - Single Port
  - True Dual Port
  - Pseudo Dual Port
  - ROM
  - FIFO (logic wrapper added automatically by design tools)
- Flexible customization features
  - Initialization of RAM/ROM
  - Memory cascading (handled automatically by design tools)
  - Optional parity bit support
  - Byte-enable
  - Multiple block size options
  - RAM modes support optional Write Through or Read-Before-Write modes

4.4. System Resources

4.4.1. CMOS GPIO (Bank 0)

CrossLink provides dedicated CMOS GPIO on Bank 0 of the device. These GPIO do not include differential signaling support. A summary of the features associated with these GPIOs is listed below:

- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs)
  - LVTTL33
- Tri-state control for output
- Input/output register blocks
- Open-drain option and programmable input hysteresis
- Internal pull-up resistors with configurable values of 3.3 kΩ, 6.8 kΩ, 10 kΩ

4.4.2. Power Management Unit

The embedded Power Management Unit (PMU) allows low-power Sleep State of the device. Figure 4.3 shows the block diagram of the PMU IP.

When instantiated in the design, PMU is always on, and uses the low-speed clock from oscillator of the device to perform its operations.

The typical use case for the PMU is through a user implemented state machine that controls the sleep and wake up of the device. The state machine implemented in the FPGA fabric identifies when the device needs to go into sleep mode, issues the command through PMU's FPGA fabric interface, assigns the parameters for sleep (time to wake up and so on) and issues Sleep command.

The device can be woken up externally using the PMU Wake-Up (USRWKUP) pin, or from the PMU Watch Dog Timer expiry or from I2C0 (address decoding detection or FIFO full in one of hardened I^2C).

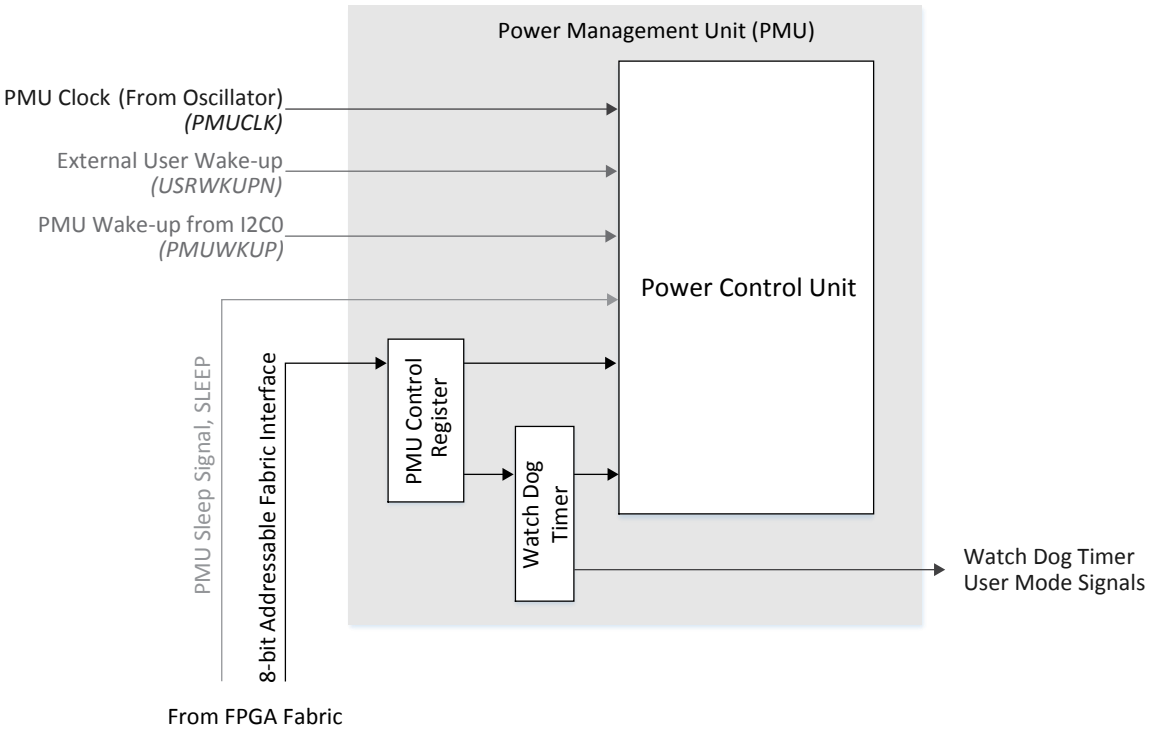


Figure 4.3. CrossLink MIPI D-PHY Block

4.4.2.1. PMU State Machine

PMU can place the device in two mutually exclusive states – Normal State and Sleep State. Figure 4.4 on the next page shows the PMU State Machine triggers for transition from one state to the other.

- Normal state – All elements of the device are active to the extent required by the design. In this state, the device is at fully active and performing as required by the application.
  Note that the power consumption of the device is highest in this state.
- Sleep state – The device is power gated such that the device is not operational. The configuration of the device and the EBR contents are retained; thus in Sleep mode, the device does not lose configuration SRAM and EBR contents. When it transitions to Normal state, device operates with these contents preserved.
  The PMU is active along with the associated GPIOs.
  The power consumption of the device is lowest in this state. This helps reduce the overall power consumption for the device.

5.6. Preliminary DC Electrical Characteristics

Over recommended operating conditions.

Table 5.5. Preliminary DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4, 5]	Input or I/O Leakage	$0 \le V_{IN} \le V_{CCIO}$	−10	—	+10	µA
I_{PU}[4]	Internal Pull-Up Current	V_{CCIO} = 1.2 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−2.7	—	−8	µA
		V_{CCIO} = 1.8 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−3	—	−31	µA
		V_{CCIO} = 2.5 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−8	—	−72	µA
		V_{CCIO} = 3.3 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−11	—	−128	µA
C_1[2]	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf
C_2[2]	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf
V_{HYST}[3]	Hysteresis for Single-Ended Inputs	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	200	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A = 25 °C, f = 1.0 MHz.
3. Hysteresis is not available for V_{CCIO} = 1.2 V.
4. Weak pull-up setting. Programmable pull-up resistors on Bank 0 will see higher current. Refer to FPGA-TN-02016, CrossLink sysI/O Usage Guide for details on programmable pull-up resistors.
5. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO}, or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

5.7. Preliminary CrossLink Supply Current

Over recommended operating conditions.

Table 5.6. Preliminary CrossLink Supply Current

Symbol	Parameter	Typ	Unit
Normal Operation[1]			
I_{CC}	Core Power Supply Current	7.17	mA
I_{CCPLL}	PLL Power Supply Current	0.05	mA
$I_{CCAUX25VPP}$	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	2.65	mA
I_{CCIOx}	Bank x Power Supply Current (per Bank)	0.06	mA
I_{CCA_DPHYx}	V_{CCA_DPHYx} Power Supply Current	8.33	mA
I_{CCPLL_DPHYx}	V_{CCPLL_DPHYx} Power Supply Current	1.31	mA
Standby Current[2]			
$I_{CCSTDBY}$	Core Power Supply Standby Current	2.73	mA
$I_{CCPLLSTDBY}$	PLL Power Supply Standby Current	—	mA
$I_{CCAUX25VPPSTDBY}$	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Standby Current	0.46	mA
$I_{CCIOSTDBY}$	Bank Power Supply Standby Current (per Bank)	0	mA
$I_{CCA\_DPHYxSTDBY}$	V_{CCA_DPHYx} Power Supply Standby Current	0.01	mA
$I_{CCPLL\_DPHYxSTDBY}$	V_{CCPLL_DPHYx} Power Supply Standby Current	0.01	mA
Sleep/Power Down Mode Current[3]			
I_{CC_SLEEP}	Core Power Supply Sleep Current	0.48	mA
I_{CCGPLL_SLEEP}	PLL Power Supply Current	0.05	mA
I_{CCAUX_SLEEP}	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	0.03	mA
I_{CCIOx_SLEEP}	Bank Power Supply Current (per Bank)	0.06	mA
$I_{CCPLL\_DPHY\_SLEEP}$	V_{CCPLL_DPHY} Power Supply Sleep Current	0.01	mA
$I_{CCA\_DPHY\_SLEEP}$	V_{CCA_DPHY} Power Supply Sleep Current	0.05	mA

Notes:

1. **Normal Operation**
   Typical design as defined in 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge section, under the following conditions:
   a. T_J = 25 °C, all power supplies at nominal voltages.
   b. Typical processed device in csfBGA81 package.
   c. To determine power for all other applications and operating conditions, use Power Calculator in Lattice Diamond design software
2. **Standby Operation**
   A typically processed device in csfBGA81 package with blank pattern programmed, under the following conditions:
   a. All outputs are tri-stated, all inputs are held at either V_{CCIO}, or GND.
   b. All clock inputs are at 0 MHz.
   c. T_J = 25 °C, all power supplies at nominal voltages.
   d. No pull-ups on I/O.
3. **Sleep/Power Down Mode**
   Typical design as defined in 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge section, under following conditions:
   a. Design is put into Sleep/Power Down Mode with user logic powers down D-PHY, and enters into Sleep Mode in PMU.
   b. T_J = 25 °C, all power supplies at nominal voltages.
   c. Typical processed device in csfBGA81 package.
4. **For ucfBGA64 package**
   a. V_{CCA_DPHY0} and V_{CCA_DPHY1} are tied together as V_{CC_DPHYX}.
   b. V_{CCPLL_DPHY0} and V_{CCPLL_DPHY1} are tied together as V_{CC_DPHYX}.
5. **For WLCS36 package**
   a. V_{CCGPLL} and V_{CCIO1} (Bank 1) are tied together to V_{CC}.
   b. V_{CCPLL_DPHY} and V_{CCA_DPHY} are tied together as V_{CCMU_DPHY}.
6. To determine the CrossLink start-up peak current, use the Power Calculator tool in the Lattice Diamond design software.

5.11. Preliminary sysI/O Differential Electrical Characteristics

5.11.1. Preliminary LVDS/subLVDS/SLVS

Over recommended operating conditions.

Table 5.10. LVDS/subLVDS[1]/SLVS[1, 2]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INPM}	Input Voltage	—	0.00	—	2.40	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two inputs	–100	—	100	mV
$V_{THD(subLVDS)}$	Differential Input Threshold	Difference between the two inputs	–90	—	90	mV
$V_{THD(SLVS)}$	Differential Input Threshold	Difference between the two inputs	TBD	—	TBD	mV
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ω	—	1.43	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ω	0.90	1.08	—	V
V_{OD}	Output Voltage Differential	$\lvert V_{OP} - V_{OM} \rvert$, RT = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OH} + V_{OL})/2$, RT = 100 Ω	1.13	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V driver outputs shorted to each other	—	—	12	mA

Notes:

1. Inputs only for subLVDS and SLVS.
2. For SLVS/MIPI interface I/O placement, see the Programmable I/O Banks section.

5.11.2. Preliminary Hardened MIPI D-PHY I/Os

Table 5.11. Preliminary MIPI D-PHY

	Description	Min	Typ	Max	Unit
Receiver					
High Speed					
V_{CMRX}	Common-Mode Voltage HS Receive Mode	70	—	330	mV
V_{IDTH}	Differential Input High Threshold	—	—	70	mV
V_{IDTL}	Differential Input Low Threshold	−70	—	—	mV
V_{IHHS}	Single-ended Input High Voltage	—	—	460	mV
V_{ILHS}	Single-ended Input Low Voltage	−40	—	—	mV
$V_{TERM-EN}$	Single-ended Threshold for HS Termination Enable	—	—	450	mV
Z_{ID}	Differential Input Impedance	80	100	125	Ω
Low Power					
V_{IH}	Logic 1 Input Voltage	880	—	—	mV
V_{IL}	Logic 0 Input Voltage, not in ULP State	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 Input Voltage, in ULP State	—	—	300	mV
V_{HYST}	Input Hysteresis	25	—	—	mV
Transmitter					
High Speed					
V_{CMTX}	HS Transmit Static Common Mode Voltage	150	200	250	mV
V_{OD}	HS Transmit Differential Voltage	140	200	270	mV
V_{OHHS}	HS Output High Voltage	—	—	360	mV
Z_{OS}	Single-ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single-ended Output Impedance Mismatch	—	—	10	%
Low Power					
V_{OH}	Output High Level	1.1	1.2	1.3	V
V_{OL}	Output Low Level	−50	—	50	mV
Z_{OLP}	Output Impedance of LP Transmitter	110	—	—	Ω

Table 5.13. Preliminary CrossLink External Switching Characteristics (*Continued*)

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Generic DDRX141 Outputs with Clock and Data Aligned at Pin (GDDRX141_TX.ECLK)					
T_{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	All Devices	—	0.125	ns+i*UI
T_{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	All Devices	–0.125	—	ns+(i+ 1)*UI
$T_{TPBi\_skew\_UI}$	TX skew in UI	All Devices	—	0.15	UI
f_{MAX_TX141}	DDR141 ECLK Frequency[3]	csfBGA81	—	600	MHz
		WLCSP36	—	500	MHz

Notes:
1. General I/O timing numbers based on LVCMOS 2.5, 0 pf load.
2. Generic DDRX8, DDRX71 and DDRX141 timing numbers based on LVDS I/O.
3. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
4. These numbers are generated using best case PLL located.
5. All numbers are generated with the Lattice Diamond design software.

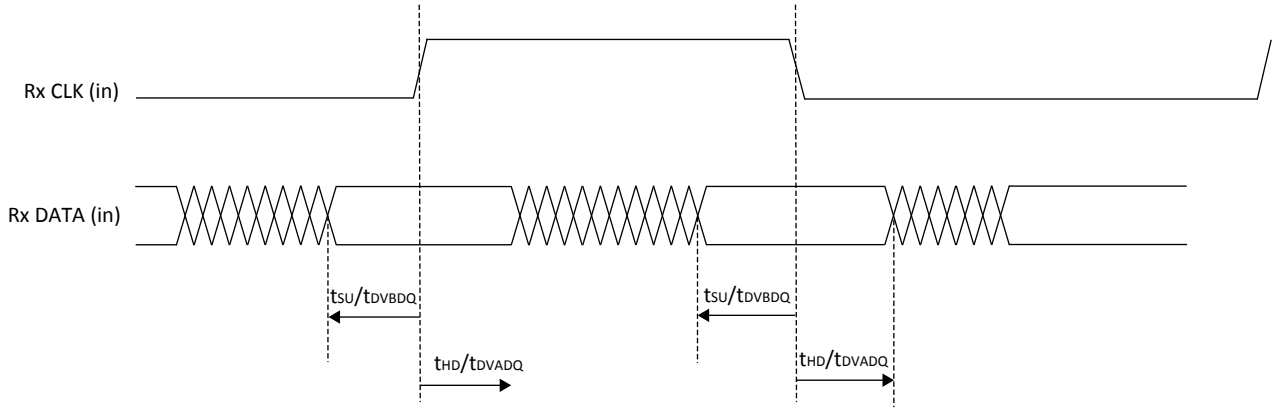


Figure 5.1. Receiver RX.CLK.Centered Waveforms

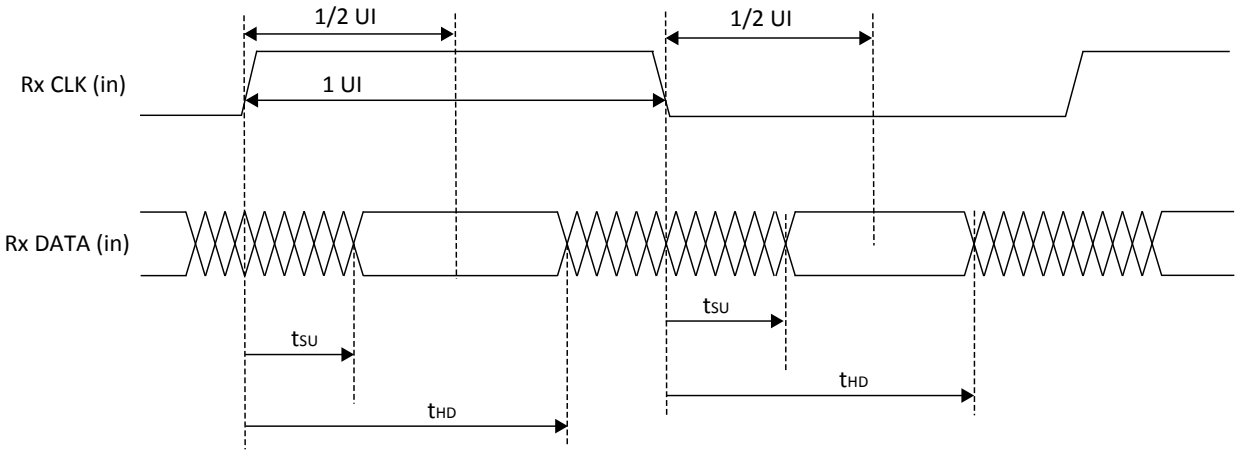


Figure 5.2. Receiver RX.CLK.Aligned Input Waveforms

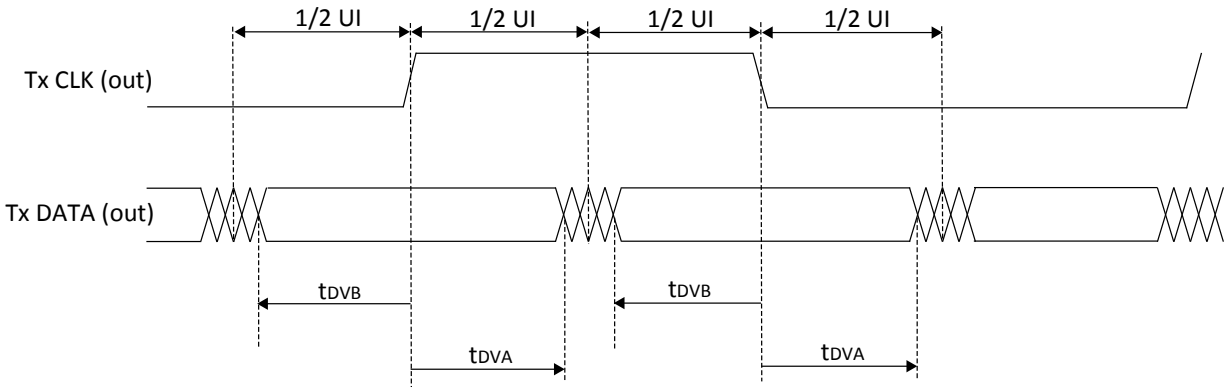


Figure 5.3. Transmit TX.CLK.Centered Output Waveforms

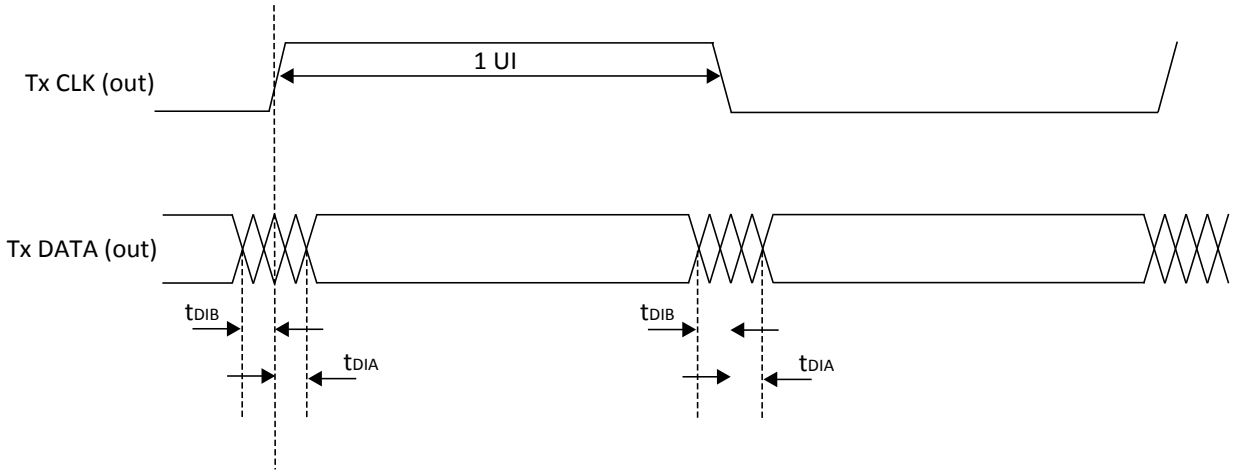


Figure 5.4. Transmit TX.CLK.Aligned Waveforms

5.18. CrossLink sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 5.20. CrossLink sysCONFIG Port Timing Specifications

Symbol	Parameter	Min	Max	Unit
All Configuration Mode				
t_{PRGM}	CRESETB LOW Pulse Accepted	145	—	ns
Slave SPI				
f_{CCLK}	SPI_SCK Input Clock Frequency	—	110	MHz
t_{STSU}	MOSI Setup Time	0.5	—	ns
t_{STH}	MOSI Hold Time	2.0	—	ns
t_{STCO}	SPI_SCK Falling Edge to Valid MISO Output	—	13.3	ns
t_{SCS}	Chip Select HIGH Time	42	—	ns
t_{SCSS}	Chip Select Setup Time	0.5	—	ns
t_{SCSH}	Chip Select Hold Time	0.5	—	ns
Master SPI				
f_{CCLK}	MCK Output Clock Frequency	—	52.8	MHz
I^2C*				
f_{MAX}	Maximum SCL Clock Frequency (Fast-Mode Plus	—	1	MHz

***Note**: Refer to the I^2C specification for timing requirements when configuring with I^2C port.

5.19. Preliminary SRAM Configuration Time from NVCM

Over recommended operating conditions.

Table 5.21. Preliminary SRAM Configuration Time from NVCM

Symbol	Parameter	Typ	Unit
$t_{CONFIGURATION}$	POR to Device I/O Active[1]	83	ms

Note:

1. Before and during configuration, the I/Os are held in tristate with weak internal pullups enabled. I/Os are released to user functionality when the device has finished configuration.

6. Pinout Information

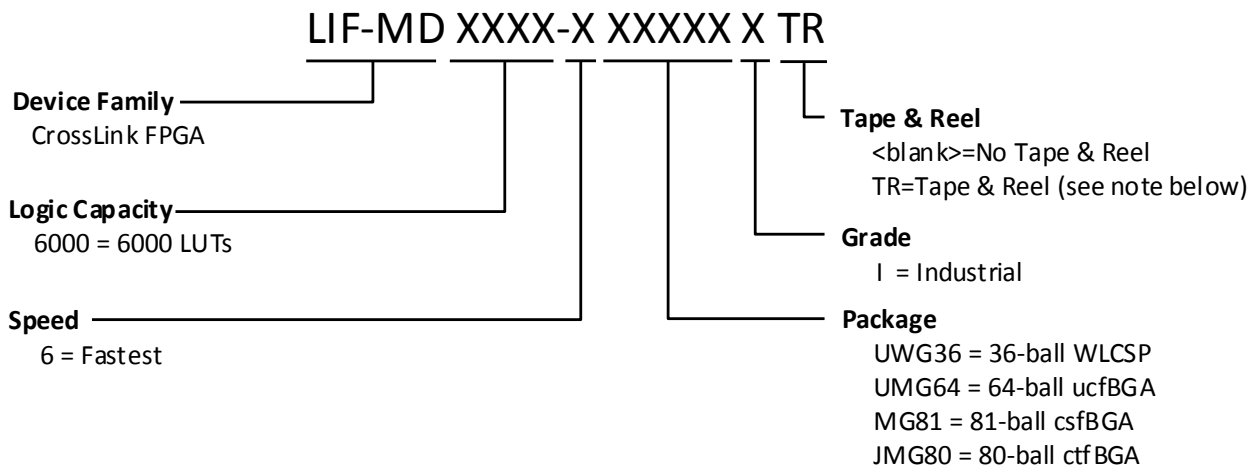
6.1. WLCSP36 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	GNDMU_DPHY1	GND	—	—
A2	VCCMU_DPHY1	DPHY1	—	—
A3	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
A4	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
A5	VCCAUX	VCCAUX	—	—
A6	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
B1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B2	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
B3	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
B4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
B5	PB16D	2	PCLKC2_1	Comp_OF_PB16C
B6	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
C1	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
C2	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
C3	PB52	0	SPI_SS/CSN/SCL	—
C4	VCC	VCCAUX	—	—
C5	PB16C	2	PCLKT2_1	True_OF_PB16D
C6	GND	GND	—	—
D1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
D2	PB48	0	PCLKT0_1/USER_SCL	—
D3	PB47	0	PCLKT0_0/USER_SDA	—
D4	CRESET_B	0	—	—
D5	PB16B	2	PCLKC2_0	Comp_OF_PB16A
D6	PB6B	2	—	Comp_OF_PB6A
E1	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
E2	VCCIO0	0	—	—
E3	GND	GND	—	—
E4	PB50	0	MOSI	—
E5	PB16A	2	PCLKT2_0	True_OF_PB16B
E6	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F1	PB51	0	MISO	—
F2	PB49	0	PMU_WKUPN/CDONE	—
F3	PB53	0	SPI_SCK/MCK/SDA	—
F4	PB12A	2	GPLLT2_0	True_OF_PB12B
F5	PB12B	2	GPLLC2_0	Comp_OF_PB12A
F6	VCCIO2	2	—	—

6.4. csfBGA81 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
A2	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A3	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
A4	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
A5	VCCA_DPHY1	DPHY1	—	—
A6	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A7	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
A8	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
A9	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
B1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
B3	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
B4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
B5	GNDPLL_DPHYX	GND	—	—
B6	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B7	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
B8	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
B9	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
C1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
C2	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
C3	GNDA_DPHY1	DPHY1	—	—
C4	VCCPLL_DPHY1	DPHY1	—	—
C5	GND	GND	—	—
C6	VCCPLL_DPHY0	DPHY0	—	—
C7	GNDA_DPHY0	DPHY0	—	—
C8	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
C9	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
D1	PB34A	1	GR_PCLK1_0	True_OF_PB34B
D2	PB34B	1	—	Comp_OF_PB34A
D3	VCCA_DPHY1	DPHY1	—	—
D4	GND	GND	—	—
D5	VCCAUX	VCCAUX	—	—
D6	GND	GND	—	—
D7	VCCA_DPHY0	DPHY0	—	—
D8	PB16B	2	PCLKC2_0	Comp_OF_PB16A
D9	PB16A	2	PCLKT2_0	True_OF_PB16B
E1	PB38A	1	—	True_OF_PB38B
E2	PB38B	1	—	Comp_OF_PB38A
E3	VCC	VCC	—	—
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCCIO2	2	—	—

7. CrossLink Part Number Description



7.1. Ordering Part Numbers

Industrial

Part Number	Grade	Package	Pins	Temp.	LUTs (K)
LIF-MD6000-6UWG36ITR	–6	Lead free WLCSP	36	Industrial	5.9
LIF-MD6000-6UMG64I	–6	Lead free ucfBGA	64	Industrial	5.9
LIF-MD6000-6MG81I	–6	Lead free csfBGA	81	Industrial	5.9
LIF-MD6000-6JMG80I	–6	Lead free ctfBGA	80	Industrial	5.9

Note: UWG36 package is available in shipments of 5000 pieces/reel (TR), 1000 pieces/reel (TR1K), and 50 pieces/reel (TR50 – for samples only).