Lattice Semiconductor Corporation - LIF-MD6000-6UWG36ITR1K Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1484
Number of Logic Elements/Cells	5936
Total RAM Bits	184320
Number of I/O	17
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP (2.54x2.59)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lif-md6000-6uwg36itr1k

Figures

Tables

1. General Description

CrossLink™ from Lattice Semiconductor is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. The device is based on Lattice mobile FPGA technology. It combines the extreme flexibility of an FPGA with the low power, low cost and small footprint of an ASIC.

CrossLink supports video interfaces including MIPI® DPI, MIPI DBI, CMOS camera and display interfaces, OpenLDI, FPD-Link, FLATLINK, MIPI D-PHY, MIPI CSI-2, MIPI DSI, SLVS200, SubLVDS, HiSPi and more.

Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for CrossLink. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

The Lattice Diamond® design software allows large complex designs to be efficiently implemented using CrossLink. Synthesis library support for CrossLink devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the CrossLink device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Interfaces on CrossLink provide a variety of bridging solutions for smart phone, tablets, wearables, VR, AR, Drone, Smart Home, HMI as well as adjacent ISM markets. The device is capable of supporting high-resolution, high-bandwidth content for mobile cameras and displays at 4k UHD and beyond.

1.1. Features

- Ultra-low power
  - Sleep Mode Support
  - Normal Operation – From 5 mW to 150 mW
- Ultra small footprint packages
  - 36-ball WLCSP (6 mm^2)
  - 64-ball ucfBGA (12 mm^2)
  - 80-ball ctfBGA (40 mm^2)
  - 81-ball csfBGA (20 mm^2)
- Programmable architecture
  - 5936 LUTs
  - 180 kb block RAM
  - 47 kb distributed RAM
- Two hardened 4-lane MIPI D-PHY interfaces
  - Transmit and receive
  - 6 Gb/s per D-PHY interface
- Programmable source synchronous I/O
  - MIPI D-PHY Rx, LVDS Rx, LVDS Tx, SubLVDS Rx, SLVS200 Rx, HiSPi Rx
  - 1200 Mb/s per I/O
  - Four high-speed clock inputs
- Programmable CMOS I/O
  - LVTTL and LVCMOS
    - 3.3 V, 2.5 V, 1.8 V and 1.2 V (outputs)
  - LVDS, LVCMOS differential I/Os
- Flexible device configuration
  - One Time Programmable (OTP) non-volatile configuration memory
  - Master SPI boot from external flash
    - Dual image booting supported
  - I^2C programming
  - SPI programming
  - TransFR™ I/O for simple field updates
- Enhanced system level support
  - Reveal logic analyzer
  - TraceID for system tracking
  - On-chip hardened I^2C block
- Applications examples
  - 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge
  - 1:2 MIPI DSI Display Interface Bridge
  - MIPI DSI to/from FPD-Link/OpenLDI LVDS Display Interface Bridge
  - MIPI DSI to/from CMOS Display Interface Bridge
  - MIPI CSI-2 to/from CMOS Image Sensor Interface Bridge
  - SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

2. Application Examples

2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge

Figure 2.1 shows the block diagram for the 2:1 MIPI CSI-2 image sensor aggregator bridge. This solution merges image outputs from multiple sensors into a single CSI-2 output to an application processor.

Table 2.1 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting any input encoding, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. Up to 8 image sensor inputs can be aggregated, depending on data rate and number of lanes. For details, refer to FPGA-IPUG-02002, 2:1 MIPI CSI-2 Bridge Soft IP User Guide.

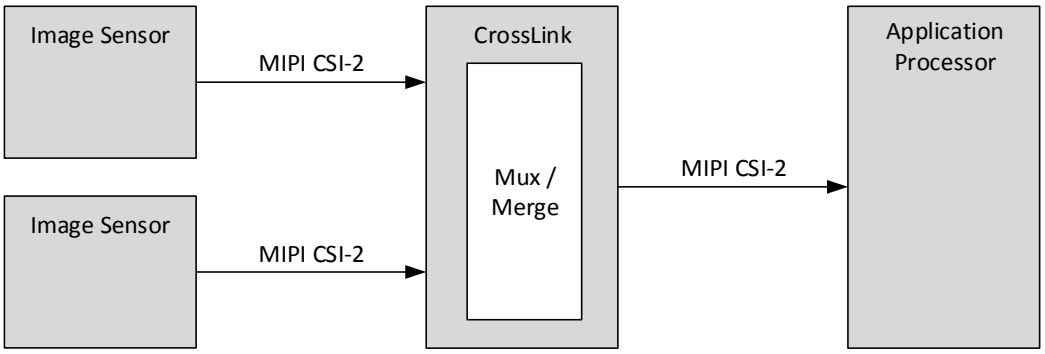


Figure 2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge

Table 2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge Overview

Application Example Details	
Input Type	2 x 1080p60, 12-bit RAW 2 x 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Programmable Fabric Operation(s)	Merge Image Sensor Outputs with no Frame drop Mux/Merge in flexible combinations
Output Type	1 x 1080p60, 12-bit RAW 1 x 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Additional System Functions	Support for I²C Bridge/Mux for Camera Configuration GPIO for image sensor sync and reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~55 mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~85% of LUT4; ~100% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Figure 2.4 shows the block diagram for the MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge. This solution bridges the MIPI DSI output from the application processor to a single or dual channel FPD-Link/OpenLDI LVDS display input.

Table 2.4 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting both RGB666 and RGB888, variable number of LVDS data lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02003, MIPI DSI to OpenLDI/FPD-Link/LVDS Interface Bridge Soft IP User Guide.

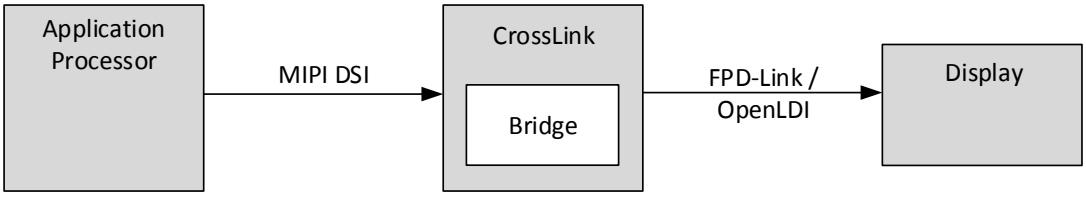


Figure 2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Table 2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Bridge
Output Type	1080p60, 24-bit RGB 2 Channels (2 x 4 Data Lanes and 2 x 1 Clock Lane) @ 74.25MHz FPD-Link Clock
Additional System Functions	Display Configuration Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	TBD mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~30% of LUT4; ~30% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.5. CMOS to MIPI DSI Display Interface Bridge

Figure 2.5 shows the block diagram for the CMOS to MIPI DSI display interface bridge. This solution bridges the CMOS parallel output from the application processor to a DSI display input.

Table 2.5 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

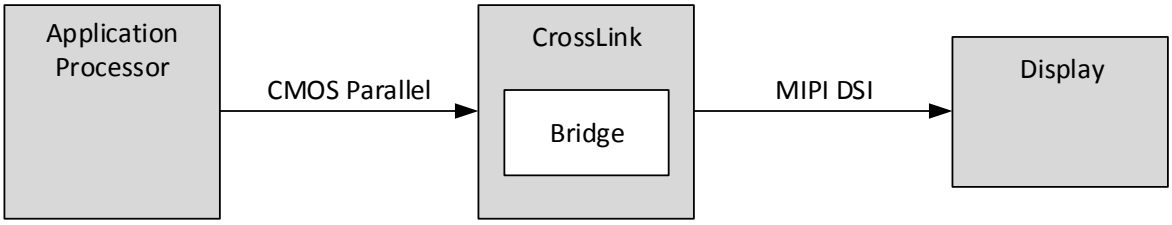


Figure 2.5. CMOS to MIPI DSI Display Interface Bridge

Table 2.5. CMOS to MIPI DSI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB CMOS Parallel @ 148.5 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~80 mW
Device I/O Used	28 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Figure 2.6 shows the block diagram for the CMOS to MIPI CSI-2 Image Sensor Interface Bridge. This solution bridges the CMOS parallel output from an image sensor to a CSI-2 input of an application processor.

Table 2.6 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

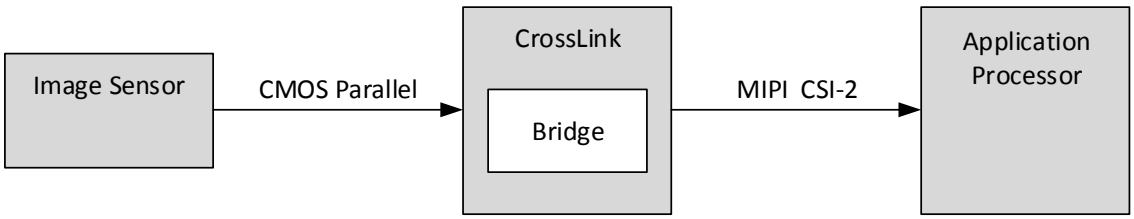


Figure 2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Table 2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 12-bit RAW CMOS Parallel @ 74.25 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 12-bit RAW 4-Lane MIPI D-PHY @ ~450 Mb/s per lane
Additional System Functions	I^2C for Camera Configuration GPIO for image sensor reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~75 mW
Device I/O Used	16 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

Figure 2.9 shows the block diagram for a SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge. This solution bridges from an image sensor SubLVDS output to CSI-2 output to an application processor.

Table 2.9 provides additional details for a specific application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting RAW10 or RAW12 pixel width, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02006, SubLVDS to MIPI CSI-2 IP Image Sensor Interface Bridge Soft IP User Guide.

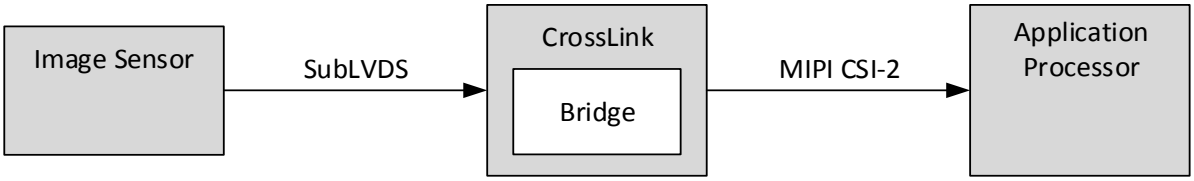


Figure 2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

Table 2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	4k2k@64.7fps, RAW10 SubLVDS 10 data lane @ 600 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	4k2k@64.7fps, RAW10 CSI-2 over 4-Lane MIPI D-PHY @ 1.5 Gb/s per lane
Additional System Functions	Image Frame Control GPIO for reset and power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~130 mW
Device I/O Used	22 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	80% of LUT4; ~60% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

4.3. Programmable FPGA Fabric

4.3.1. FPGA Fabric Overview

CrossLink is built around a programmable logic fabric consisting of 5936 four input lookup tables (LUT4) arranged alongside dedicated registers in Programmable Functional Units (PFU). These PFU blocks are the building blocks for logic, arithmetic, RAM and ROM functions. The PFU blocks are connected via a programmable routing network. The Lattice Diamond design software configures the PFU blocks and the programmable routing for each unique design. Interspersed between rows of PFU are rows of sysMEM™ Embedded Block RAM (EBR), with programmable I/O banks, embedded I^2C and embedded MIPI D-PHY arranged on the top and bottom of the device as shown in Figure 4.2.

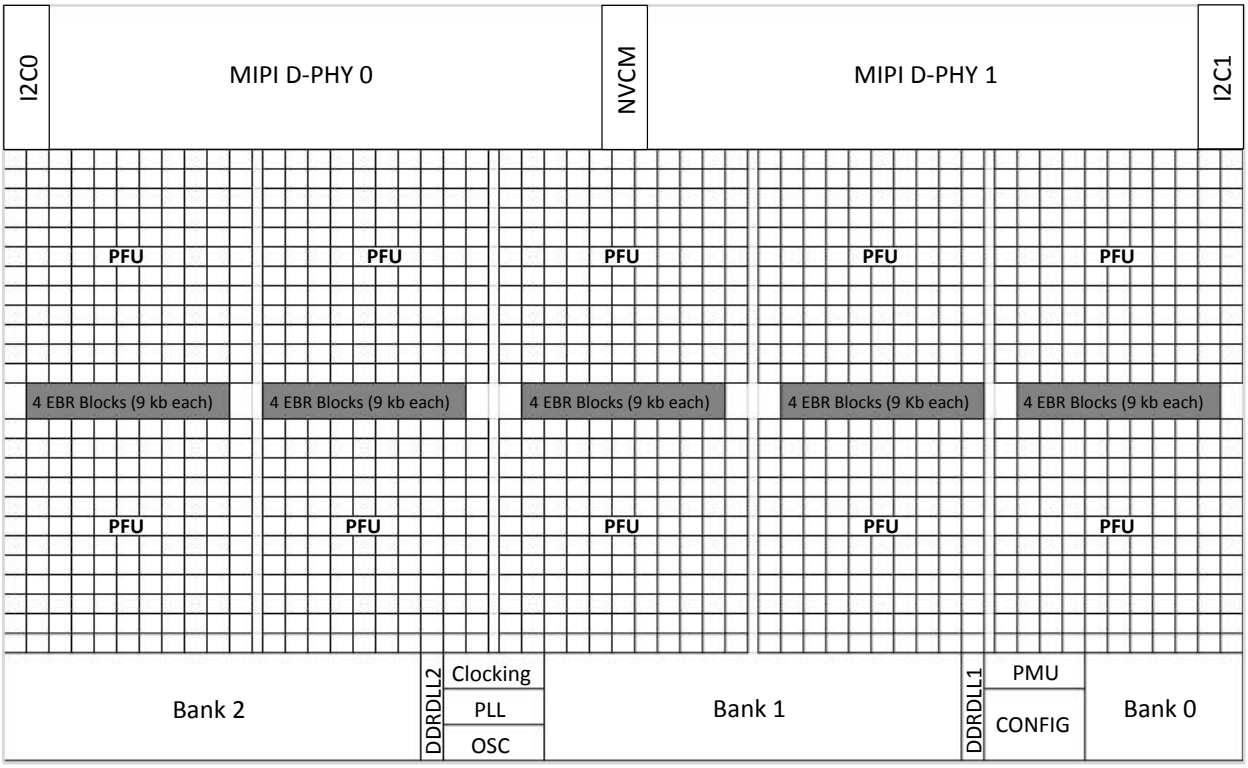


Figure 4.2. CrossLink Device Simplified Block Diagram (Top Level)

4.3.2. Clocking Overview

The CrossLink device family provides resources to support a wide range of clocking requirements for programmable video bridging. These resources are listed below. For details, refer to FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide.

- sysCLOCK PLL
  - Flexible Frequency Synthesis (See Table 5.14 for input frequency range and output frequency range.)
  - Dynamically selectable Clock Input
  - Four Clock Outputs
    - Independent, dynamic enable control
    - Programmable phase adjustment
  - Standby Input
  - Lock Output
- Clock Distribution Network
  - Eight Primary Clocks
    - Dedicated Clock input pins (PCLK)
    - Source from PLL, Clock Divider, Hard D-PHY blocks or On-chip Oscillator

- Four Edge Clocks for high-speed DDR interfaces
  - 2 per Programmable I/O bank
  - Source from PCLK pins, PLL or DLL blocks
  - Programmable Clock divider per Edge Clock
  - Delay primitives for 90 degree phase shifting of clock/data (DDRDLL, DLLDEL)
- Dynamic Clock Control
  - Fabric control to disable clock nets for power savings
- Dynamic Clock Select
  - Smart clock multiplexer with two independent inputs and glitchless output support
- Two On-Chip Oscillators
  - Always-on Low Frequency (LFCLKOUT) with nominal frequency of 10 kHz
  - High-Frequency (HFCLKOUT) with nominal frequency of 48 MHz, programmable output dividers, and dynamic enable control

4.3.3. Embedded Block RAM Overview

CrossLink devices also contain sysMEM Embedded Block RAM (EBR). The EBR consists of a 9 kB RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Supported modes and other general information on the EBR are listed below. For details, refer to FPGA-TN-02017, CrossLink Memory Usage Guide.

- Support for different memory configurations
  - Single Port
  - True Dual Port
  - Pseudo Dual Port
  - ROM
  - FIFO (logic wrapper added automatically by design tools)
- Flexible customization features
  - Initialization of RAM/ROM
  - Memory cascading (handled automatically by design tools)
  - Optional parity bit support
  - Byte-enable
  - Multiple block size options
  - RAM modes support optional Write Through or Read-Before-Write modes

4.4. System Resources

4.4.1. CMOS GPIO (Bank 0)

CrossLink provides dedicated CMOS GPIO on Bank 0 of the device. These GPIO do not include differential signaling support. A summary of the features associated with these GPIOs is listed below:

- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs)
  - LVTTL33
- Tri-state control for output
- Input/output register blocks
- Open-drain option and programmable input hysteresis
- Internal pull-up resistors with configurable values of 3.3 kΩ, 6.8 kΩ, 10 kΩ

5.3. Preliminary Power Supply Ramp Rates

Table 5.3. Preliminary Power Supply Ramp Rates[1]

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies except V_{CCAUX}	0.6	10	V/ms

Note:

1. Assume monotonic ramp rates.

5.4. Preliminary Power-On-Reset Voltage Levels

Table 5.4. Preliminary Power-On-Reset Voltage Levels[1, 3, 4]

Symbol	Parameter		Min	Typ	Max	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	0.62	0.68	0.93	V
		V_{CCIO0}[2]	0.87	1.08	1.50	V
		V_{CCAUX}	0.90	—	1.53	V
V_{PORDN}	Power-On-Reset ramp down trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	—	—	0.79	V
		V_{CCIO0}[2]	—	—	1.50	V
		V_{CCAUX}	—	—	1.53	V

Notes:

1. These POR ramp up trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. Only V_{CCIO0} (Config Bank) has a Power-On-Reset ramp up trip point. All other VCCIOs do not have Power-On-Reset ramp up detection.
3. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.
4. Configuration starts after V_{CC}, V_{CCIO0} and V_{CCAUX} reach V_{PORUP}. For details, see $t_{REFRESH}$ time in Table 5.21 on page 38.

5.5. ESD Performance

Refer to the LIFMD Product Family Qualification Summary for complete qualification data, including ESD performance.

5.7. Preliminary CrossLink Supply Current

Over recommended operating conditions.

Table 5.6. Preliminary CrossLink Supply Current

Symbol	Parameter	Typ	Unit
Normal Operation[1]			
I_{CC}	Core Power Supply Current	7.17	mA
I_{CCPLL}	PLL Power Supply Current	0.05	mA
$I_{CCAUX25VPP}$	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	2.65	mA
I_{CCIOx}	Bank x Power Supply Current (per Bank)	0.06	mA
I_{CCA_DPHYx}	V_{CCA_DPHYx} Power Supply Current	8.33	mA
I_{CCPLL_DPHYx}	V_{CCPLL_DPHYx} Power Supply Current	1.31	mA
Standby Current[2]			
$I_{CCSTDBY}$	Core Power Supply Standby Current	2.73	mA
$I_{CCPLLSTDBY}$	PLL Power Supply Standby Current	—	mA
$I_{CCAUX25VPPSTDBY}$	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Standby Current	0.46	mA
$I_{CCIOSTDBY}$	Bank Power Supply Standby Current (per Bank)	0	mA
$I_{CCA\_DPHYxSTDBY}$	V_{CCA_DPHYx} Power Supply Standby Current	0.01	mA
$I_{CCPLL\_DPHYxSTDBY}$	V_{CCPLL_DPHYx} Power Supply Standby Current	0.01	mA
Sleep/Power Down Mode Current[3]			
I_{CC_SLEEP}	Core Power Supply Sleep Current	0.48	mA
I_{CCGPLL_SLEEP}	PLL Power Supply Current	0.05	mA
I_{CCAUX_SLEEP}	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	0.03	mA
I_{CCIOx_SLEEP}	Bank Power Supply Current (per Bank)	0.06	mA
$I_{CCPLL\_DPHY\_SLEEP}$	V_{CCPLL_DPHY} Power Supply Sleep Current	0.01	mA
$I_{CCA\_DPHY\_SLEEP}$	V_{CCA_DPHY} Power Supply Sleep Current	0.05	mA

Notes:

1. **Normal Operation**
   Typical design as defined in 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge section, under the following conditions:
   a. T_J = 25 °C, all power supplies at nominal voltages.
   b. Typical processed device in csfBGA81 package.
   c. To determine power for all other applications and operating conditions, use Power Calculator in Lattice Diamond design software
2. **Standby Operation**
   A typically processed device in csfBGA81 package with blank pattern programmed, under the following conditions:
   a. All outputs are tri-stated, all inputs are held at either V_{CCIO}, or GND.
   b. All clock inputs are at 0 MHz.
   c. T_J = 25 °C, all power supplies at nominal voltages.
   d. No pull-ups on I/O.
3. **Sleep/Power Down Mode**
   Typical design as defined in 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge section, under following conditions:
   a. Design is put into Sleep/Power Down Mode with user logic powers down D-PHY, and enters into Sleep Mode in PMU.
   b. T_J = 25 °C, all power supplies at nominal voltages.
   c. Typical processed device in csfBGA81 package.
4. **For ucfBGA64 package**
   a. V_{CCA_DPHY0} and V_{CCA_DPHY1} are tied together as V_{CC_DPHYX}.
   b. V_{CCPLL_DPHY0} and V_{CCPLL_DPHY1} are tied together as V_{CC_DPHYX}.
5. **For WLCS36 package**
   a. V_{CCGPLL} and V_{CCIO1} (Bank 1) are tied together to V_{CC}.
   b. V_{CCPLL_DPHY} and V_{CCA_DPHY} are tied together as V_{CCMU_DPHY}.
6. To determine the CrossLink start-up peak current, use the Power Calculator tool in the Lattice Diamond design software.

5.8. Preliminary Power Management Unit (PMU) Timing

Table 5.7. Preliminary PMU Timing[1]

Symbol	Parameter	Device	Max	Unit
$t_{PMUWAKE}$	Time for PMU to wake from Sleep mode	All Devices	1	ms

Note:

1. For details on PMU usage, refer to FPGA-TN-02018, Power Management and Calculation for CrossLink Devices.

5.9. sysI/O Recommended Operating Conditions

Table 5.8. sysI/O Recommended Operating Conditions[1]

Standard	V_{CCIO}		
	Min	Typ	Max
LVCMOS33/LVTTL33	3.135	3.30	3.465
LVCMOS25	2.375	2.50	2.625
LVCMOS18	1.710	1.80	1.890
LVCMOS12 (Output only)	1.140	1.20	1.260
subLDVS (Input only)	2.375	2.50	2.625
SLVS (Input only)[2]	2.375	2.50	2.625
LVDS	2.375	2.50	2.625
MIPI (Input only)	1.140	1.20	1.260

Note:

1. For input voltage compatibility, refer to FPGA-TN-02016, CrossLink sysI/O Usage Guide.
2. For SLVS/MIPI interface I/O placement, see the Programmable I/O Banks section.

5.10. Preliminary sysI/O Single-Ended DC Electrical Characteristics

Table 5.9. Preliminary sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL} (mA)	I_{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS33/ LVTTL33	–0.3	0.8	2.0	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	8	–8
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS25	–0.3	0.7	1.7	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	6	–6
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	4	–4
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS12 (Output only)	—	—	—	—	0.40	V_{CCIO} – 0.4	2	–2
					0.20	V_{CCIO} – 0.2	0.1	–0.1

5.11. Preliminary sysI/O Differential Electrical Characteristics

5.11.1. Preliminary LVDS/subLVDS/SLVS

Over recommended operating conditions.

Table 5.10. LVDS/subLVDS[1]/SLVS[1, 2]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INPM}	Input Voltage	—	0.00	—	2.40	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two inputs	–100	—	100	mV
$V_{THD(subLVDS)}$	Differential Input Threshold	Difference between the two inputs	–90	—	90	mV
$V_{THD(SLVS)}$	Differential Input Threshold	Difference between the two inputs	TBD	—	TBD	mV
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ω	—	1.43	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ω	0.90	1.08	—	V
V_{OD}	Output Voltage Differential	$\lvert V_{OP} - V_{OM} \rvert$, RT = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OH} + V_{OL})/2$, RT = 100 Ω	1.13	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V driver outputs shorted to each other	—	—	12	mA

Notes:

1. Inputs only for subLVDS and SLVS.
2. For SLVS/MIPI interface I/O placement, see the Programmable I/O Banks section.

5.12. Preliminary CrossLink Maximum General Purpose I/O Buffer Speed

Over recommended operating conditions.

Table 5.12. Preliminary CrossLink Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V, csfBGA81, ctfBGA80, ucfBGA64 packages	600	MHz
	LVDS, V_{CCIO} = 2.5 V, WLCSP36 package	500	MHz
subLVDS	subLVDS, V_{CCIO} = 2.5 V, csfBGA81, ctfBGA80, ucfBGA64 packages	TBD	MHz
	subLVDS, V_{CCIO} = 2.5 V, WLCSP36 package	TBD	MHz
MIPI D-PHY (HS Mode)[6]	MIPI D-PHY, csfBGA81, ctfBGA80, ucfBGA64 packages	600	MHz
	MIPI D-PHY, WLCSP36 package	500	MHz
SLVS	SLVS, VCCIO=2.5 V, csfBGA81, ctfBGA80, ucfBGA64 packages	TBD	MHz
	SLVS, VCCIO=2.5 V, WLCSP36 package	TBD	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	300	MHz
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	300	MHz
LVCMOS25D	Differential LVCMOS, V_{CCIO} = 2.5 V	300	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	300	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	155	MHz
Maximum Output Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V, csfBGA81, ctfBGA80, ucfBGA64 packages	600	MHz
	LVDS, V_{CCIO} = 2.5 V, WLCSP36 package	500	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	300	MHz
LVTTL33D	Differential LVTTL, V_{CCIO} = 3.3 V	300	MHz
LVCMOS33	LVCMOS, 3.3 V	300	MHz
LVCMOS33D	Differential LVCMOS, 3.3 V	300	MHz
LVCMOS25	LVCMOS, 2.5 V	300	MHz
LVCMOS25D	Differential LVCMOS, 2.5 V	300	MHz
LVCMOS18	LVCMOS, 1.8 V	155	MHz
LVCMOS12	LVCMOS, V_{CCIO} = 1.2 V	70	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Table 5.22.
4. Actual system operation may vary depending on user logic implementation.
5. Maximum data rate equals two times the clock rate when utilizing DDR.
6. This is the maximum MIPI D-PHY input rate on the programmable I/O banks 1 and 2. The hardened MIPI D-PHY input and output rates are described in Hardened MIPI D-PHY Performance section. For SLVS/MIPI interface I/O placement, see the Programmable I/O Banks section.

5.13. Preliminary CrossLink External Switching Characteristics

Over recommended commercial operating conditions.

Table 5.13. Preliminary CrossLink External Switching Characteristics[4, 5]

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Clocks					
Primary Clock					
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	150	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	ns
t_{ISKEW_PRI}	Primary Clock Skew Within a Clock	—	—	450	ps
Edge Clock					
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	600	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	0.783	—	ns
t_{ISKEW_EDGE}	Edge Clock Skew Within a Bank	—	—	120	ps
Generic SDR Interface[1]					
General Purpose I/O Pin Parameters Using Clock Tree Without PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	6.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	—	–0.90	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.82	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	—	1.02	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	—	0	—	ns
General Purpose I/O Pin Parameters Using Clock Tree With PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	5.2	ns
t_{SU}	Clock to Data Setup – PIO Input Register	—	0.17	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.01	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	—	1.70	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	—	0	—	ns
Generic DDR Interfaces[2]					
Generic DDRX8 or DDRX4 I/O with Clock and Data Centered at General Purpose Pins (GDDRX8_RX/TX.ECLK.Centered or GDDRX4_RX/TX.ECLK.Centered)					
$t_{SU\_GDDRX4\_8}$	Input Data Set-Up Before CLK Rising and Falling edges	—	0.167	—	ns
$t_{HO\_GDDRX4\_8}$	Input Data Hold After CLK Rising and Falling edges	—	0.167	—	ns
$t_{DVB\_GDDRX4\_8}$	Output Data Valid Before CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	–0.120	—	ns+1/2UI
$t_{DVA\_GDDRX4\_8}$	Output Data Valid After CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	–0.120	—	ns+1/2UI
$f_{MAX\_GDDRX4\_8}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz

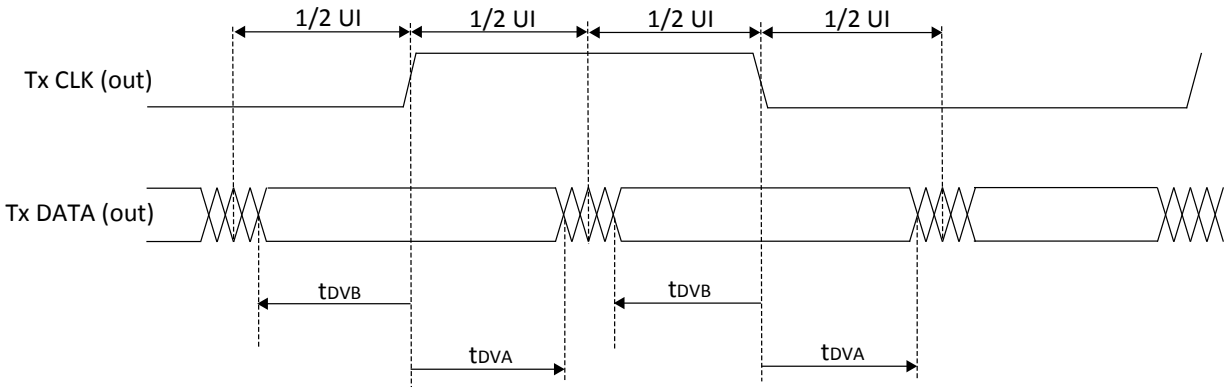


Figure 5.3. Transmit TX.CLK.Centered Output Waveforms

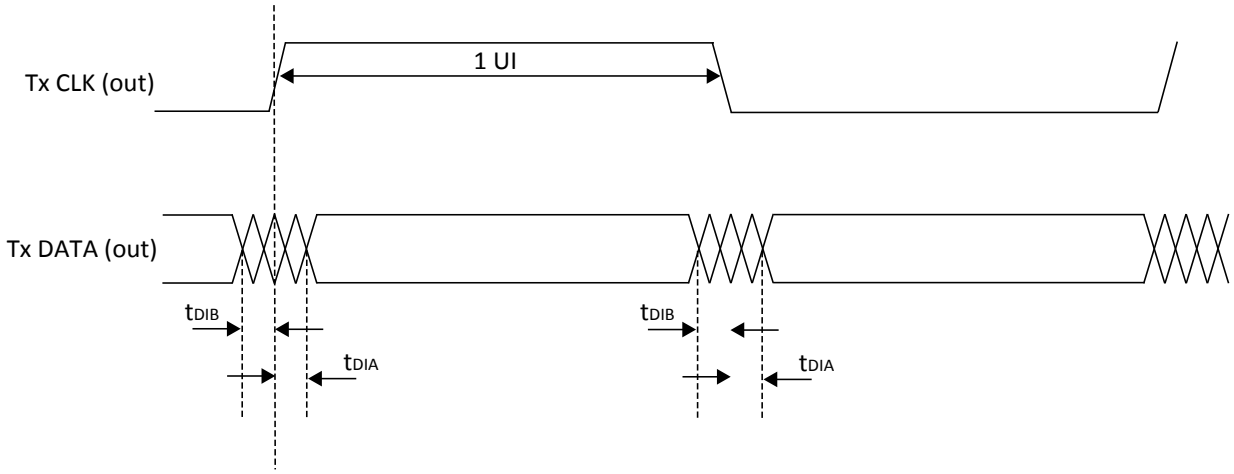
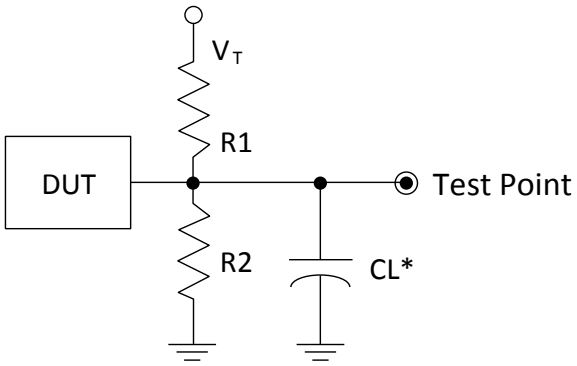


Figure 5.4. Transmit TX.CLK.Aligned Waveforms

5.20. Switching Test Conditions

Figure 5.6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 5.22.



*CL Includes Test Fixture and Probe Capacitance

Figure 5.6. Output Test Load, LVTTL and LVCMOS Standards

Table 5.22. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	$V_{OH} - 0.10$	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	$V_{OL} + 0.10$	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

6.5. Dual Function Pin Descriptions

The following table describes the dual functions available to certain pins on the CrossLink device. These pins may alternatively be used as general purpose I/O when the described dual function is not enabled.

Signal Name	I/O	Description
General Purpose		
USER_SCL	I/O	User Slave I2C0 clock input and Master I²C0 clock output. Enables PMU wake-up via I2C0.
USER_SDA	I/O	User Slave I2C0 data input and Master I²C0 data output. Enables PMU wakeup via I2C0.
PMU_WKUPN	—	This pin wakes the PMU from sleep mode when toggled low.
Clock Functions		
GPLL2_0[T, C]_IN	I	General Purpose PLL (GPLL) input pads: T = true and C = complement. These pins can be used to input a reference clock directly to the General Purpose PLL. These pins do not provide direct access to the primary clock network.
GR_PCLK[Bank]0	I	These pins provide a short General Routing path to the primary clock network. Refer to FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide for details.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins provide direct access to the primary and edge clock networks.
MIPI_CLK[T/C][Bank]_0	I/O	MIPI D-PHY Reference CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins can be used to input a reference clock directly to the D-PHY PLLs. These pins do not provide direct access to the primary clock network.
Configuration		
CDONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. Holding CDONE delays configuration.
SPI_SCK	I	Input Configuration Clock for configuring CrossLink in Slave SPI mode (SSPI).
MCK	O	Output Configuration Clock for configuring CrossLink in Master SPI mode (MSPI).
SPI_SS	I	Input Chip Select for configuring CrossLink in Slave SPI mode (SSPI).
CSN	O	Output Chip Select for configuring CrossLink in Master SPI mode (MSPI).
MOSI	I/O	Data Output when configuring CrossLink in Master SPI mode (MSPI), data input when configuring CrossLink in Slave SPI mode (SSPI).
MISO	I/O	Data Input when configuring CrossLink in Master SPI mode (MSPI), data output when configuring CrossLink in Slave SPI mode (SSPI).
SCL	I/O	Slave I²C clock I/O when configuring CrossLink in I²C mode.
SDA	I/O	Slave I²C data I/O when configuring CrossLink in I²C mode.

6.6. Dedicated Function Pin Descriptions

Signal Name	I/O	Description
Configuration		
CRESET_B	I	Configuration Reset, active LOW.
MIPI D-PHY		
DPHY[num]_CK[P/N]	I/O	MIPI D-PHY Clock [num] = D-PHY 0 or 1, P = Positive, N = Negative.
DPHY[num]_D[P/N][lane]	I/O	MIPI D-PHY Data [num] = D-PHY 0 or 1, P = Positive, N = Negative, Lane = data lane in the D-PHY block 0, 1, 2 or 3.

References

For more information, refer to the following technical notes:

- FPGA-TN-02012, CrossLink High-Speed I/O Interface
- FPGA-TN-02013, CrossLink Hardware Checklist
- FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide
- FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide
- FPGA-TN-02016, CrossLink sysI/O Usage Guide
- FPGA-TN-02017, CrossLink Memory Usage Guide
- FPGA-TN-02018, Power Management and Calculation for CrossLink Devices
- FPGA-TN-02019, CrossLink I2C Hardened IP Usage Guide
- FPGA-TN-02020, Advanced CrossLink I2C Hardened IP Reference Guide

For package information, refer to the following technical notes:

- TN1074, PCB Layout Recommendations for BGA Packages
- TN1076, Solder Reflow Guide for Surface Mount Devices
- TN1242, Wafer-Level Chip-Scale Package Guide
- Thermal Management
- Package Diagrams

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- MIPI Standards (D-PHY): www.mipi.org

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
March 2017	1.1	Updated I/O placements on banks containing MIPI interface in Programmable I/O Banks section. Updated DC and Switching Characteristics section: • Updated Table 5.4. Preliminary Power-On-Reset Voltage Levels1, [3, 4], added row of V_{PORDN} • Added Note 5 to Table 5.5. Preliminary DC Electrical Characteristics • Updated Table 5.6. Preliminary CrossLink Supply Current, added notes • Updated max values of V_{THD} and $V_{THD(subLVDS)}$ in Table 5.10. LVDS/subLVDS1/SLVS1, [2] • Maximum input frequency values of subLVDS and SLVS are TBD in Table 5.12. Preliminary CrossLink Maximum I/O Buffer Speed • Updated Table 5.13. Preliminary CrossLink External Switching Characteristics4, [5] • Updated min values of t_{SU_MIPIX4} and t_{HO_MIPIX4} in Table 5.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s) and Table 5.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s) • Updated Table 5.20. CrossLink sysCONFIG Port Timing Specifications • Updated Table 5.21. Preliminary SRAM Configuration Time from NVCM Updated Pinout Information section Updated CrossLink Part Number Description
July 2016	1.0	Updated document numbers.
May 2016	1.0	First preliminary release.