Lattice Semiconductor Corporation - LIF-MD6000-6UWG36ITR50 Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	1484
Number of Logic Elements/Cells	5936
Total RAM Bits	184320
Number of I/O	17
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP (2.54x2.59)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lif-md6000-6uwg36itr50

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CSI	Camera Serial Interface
DSI	Display Serial Interface
EBR	Embedded Block RAM
ECLK	Edge Clock
FPD	Flat Panel Display
I^2C	Inter-Integrated Circuit
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
NVCM	Non-Volatile Configuration Memory
OTP	One Time Programmable
PCLK	Primary Clock
PFU	Programmable Functional Unit
PLL	Phase Locked Loops
PMU	Power Management Unit
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
WLCSP	Wafer Level Chip Scale Packaging

2. Application Examples

2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge

Figure 2.1 shows the block diagram for the 2:1 MIPI CSI-2 image sensor aggregator bridge. This solution merges image outputs from multiple sensors into a single CSI-2 output to an application processor.

Table 2.1 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting any input encoding, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. Up to 8 image sensor inputs can be aggregated, depending on data rate and number of lanes. For details, refer to FPGA-IPUG-02002, 2:1 MIPI CSI-2 Bridge Soft IP User Guide.

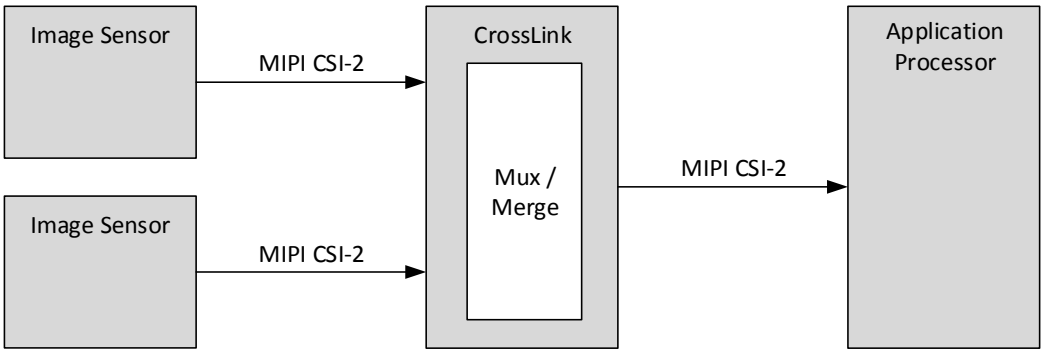

Figure 2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge

Table 2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge Overview

Application Example Details	
Input Type	2 x 1080p60, 12-bit RAW 2 x 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Programmable Fabric Operation(s)	Merge Image Sensor Outputs with no Frame drop Mux/Merge in flexible combinations
Output Type	1 x 1080p60, 12-bit RAW 1 x 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Additional System Functions	Support for I²C Bridge/Mux for Camera Configuration GPIO for image sensor sync and reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~55 mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~85% of LUT4; ~100% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Figure 2.4 shows the block diagram for the MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge. This solution bridges the MIPI DSI output from the application processor to a single or dual channel FPD-Link/OpenLDI LVDS display input.

Table 2.4 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting both RGB666 and RGB888, variable number of LVDS data lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02003, MIPI DSI to OpenLDI/FPD-Link/LVDS Interface Bridge Soft IP User Guide.

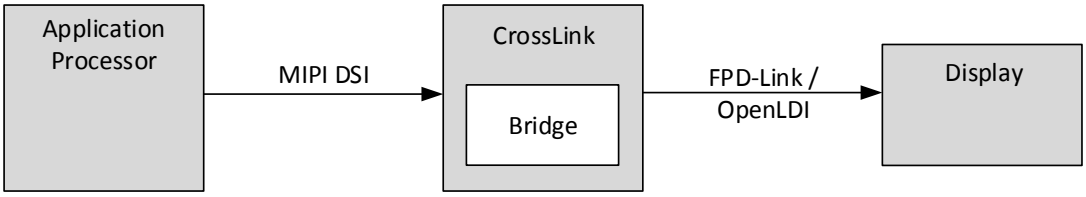

Figure 2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Table 2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Bridge
Output Type	1080p60, 24-bit RGB 2 Channels (2 x 4 Data Lanes and 2 x 1 Clock Lane) @ 74.25MHz FPD-Link Clock
Additional System Functions	Display Configuration Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	TBD mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~30% of LUT4; ~30% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

Figure 2.9 shows the block diagram for a SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge. This solution bridges from an image sensor SubLVDS output to CSI-2 output to an application processor.

Table 2.9 provides additional details for a specific application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting RAW10 or RAW12 pixel width, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02006, SubLVDS to MIPI CSI-2 IP Image Sensor Interface Bridge Soft IP User Guide.

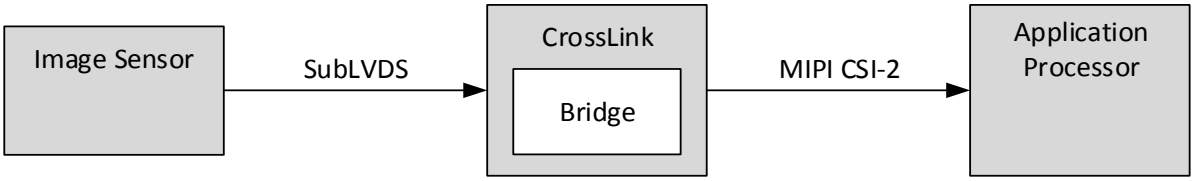

Figure 2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

Table 2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	4k2k@64.7fps, RAW10 SubLVDS 10 data lane @ 600 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	4k2k@64.7fps, RAW10 CSI-2 over 4-Lane MIPI D-PHY @ 1.5 Gb/s per lane
Additional System Functions	Image Frame Control GPIO for reset and power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~130 mW
Device I/O Used	22 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	80% of LUT4; ~60% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

3. Product Feature Summary

Table 3.1 lists CrossLink device information and packages.

Table 3.1. CrossLink Feature Summary

Device	**CrossLink**
LUTs	5936
sysMEM Blocks (9 kb)	20
Embedded Memory (kb)	180
Distributed RAM Bits (kb)	47
General Purpose PLL	1
NVCM	Yes
Embedded I^2C	2
Oscillator (10 KHz)	1
Oscillator (48 MHz)	1
Hardened MIPI D-PHY	2[1, 2]
Packages	**I/O**
36 WLCSP[2] (2.535 × 2.583 mm^2, 0.6 mm)	17
64 ucfBGA (3.5 × 3.5 mm^2, 1 mm)	29
80 ctfBGA (6.5 x 6.5 mm^2, 1 mm)	36
81 csfBGA (4.5 × 4.5 mm^2, 1 mm)	37

Notes:

1. Additional D-PHY Rx interfaces are available using programmable I/O.
2. Only one Hardened D-PHY is available in 36 WLCSP package.

- Four Edge Clocks for high-speed DDR interfaces
  - 2 per Programmable I/O bank
  - Source from PCLK pins, PLL or DLL blocks
  - Programmable Clock divider per Edge Clock
  - Delay primitives for 90 degree phase shifting of clock/data (DDRDLL, DLLDEL)
- Dynamic Clock Control
  - Fabric control to disable clock nets for power savings
- Dynamic Clock Select
  - Smart clock multiplexer with two independent inputs and glitchless output support
- Two On-Chip Oscillators
  - Always-on Low Frequency (LFCLKOUT) with nominal frequency of 10 kHz
  - High-Frequency (HFCLKOUT) with nominal frequency of 48 MHz, programmable output dividers, and dynamic enable control

4.3.3. Embedded Block RAM Overview

CrossLink devices also contain sysMEM Embedded Block RAM (EBR). The EBR consists of a 9 kB RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Supported modes and other general information on the EBR are listed below. For details, refer to FPGA-TN-02017, CrossLink Memory Usage Guide.

- Support for different memory configurations
  - Single Port
  - True Dual Port
  - Pseudo Dual Port
  - ROM
  - FIFO (logic wrapper added automatically by design tools)
- Flexible customization features
  - Initialization of RAM/ROM
  - Memory cascading (handled automatically by design tools)
  - Optional parity bit support
  - Byte-enable
  - Multiple block size options
  - RAM modes support optional Write Through or Read-Before-Write modes

4.4. System Resources

4.4.1. CMOS GPIO (Bank 0)

CrossLink provides dedicated CMOS GPIO on Bank 0 of the device. These GPIO do not include differential signaling support. A summary of the features associated with these GPIOs is listed below:

- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs)
  - LVTTL33
- Tri-state control for output
- Input/output register blocks
- Open-drain option and programmable input hysteresis
- Internal pull-up resistors with configurable values of 3.3 kΩ, 6.8 kΩ, 10 kΩ

4.4.2. Power Management Unit

The embedded Power Management Unit (PMU) allows low-power Sleep State of the device. Figure 4.3 shows the block diagram of the PMU IP.

When instantiated in the design, PMU is always on, and uses the low-speed clock from oscillator of the device to perform its operations.

The typical use case for the PMU is through a user implemented state machine that controls the sleep and wake up of the device. The state machine implemented in the FPGA fabric identifies when the device needs to go into sleep mode, issues the command through PMU's FPGA fabric interface, assigns the parameters for sleep (time to wake up and so on) and issues Sleep command.

The device can be woken up externally using the PMU Wake-Up (USRWKUP) pin, or from the PMU Watch Dog Timer expiry or from I2C0 (address decoding detection or FIFO full in one of hardened I^2C).

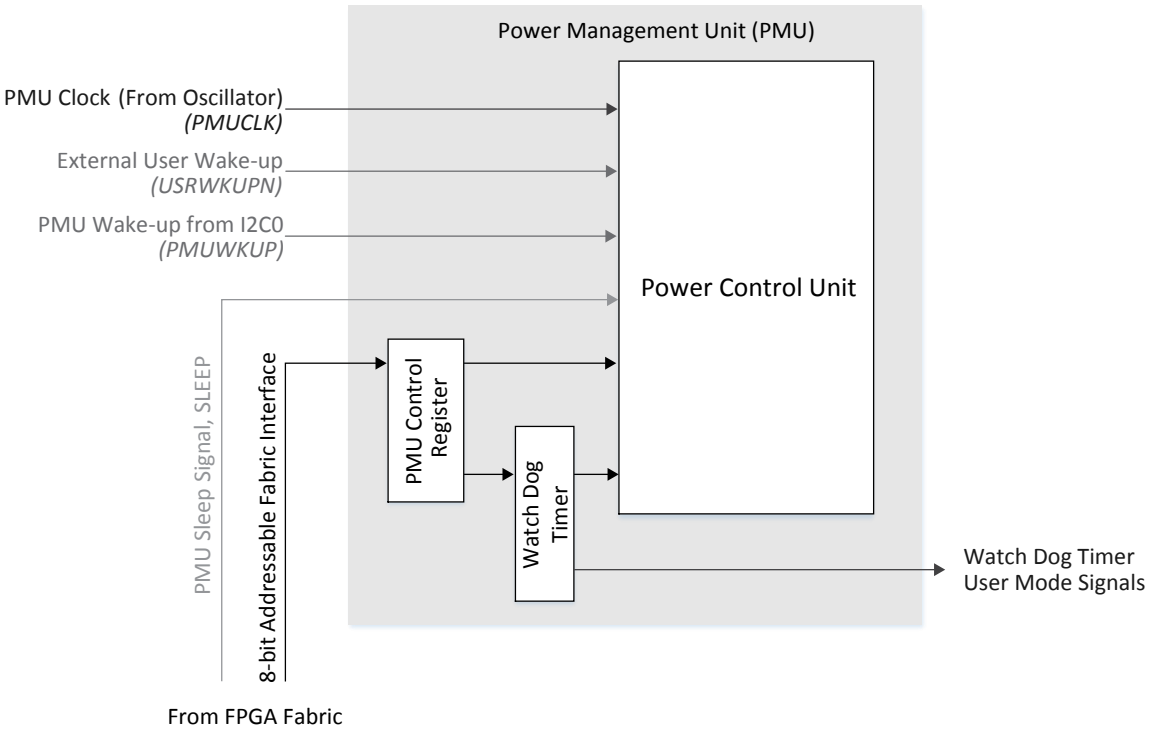

Figure 4.3. CrossLink MIPI D-PHY Block

4.4.2.1. PMU State Machine

PMU can place the device in two mutually exclusive states – Normal State and Sleep State. Figure 4.4 on the next page shows the PMU State Machine triggers for transition from one state to the other.

- Normal state – All elements of the device are active to the extent required by the design. In this state, the device is at fully active and performing as required by the application.
  Note that the power consumption of the device is highest in this state.
- Sleep state – The device is power gated such that the device is not operational. The configuration of the device and the EBR contents are retained; thus in Sleep mode, the device does not lose configuration SRAM and EBR contents. When it transitions to Normal state, device operates with these contents preserved.
  The PMU is active along with the associated GPIOs.
  The power consumption of the device is lowest in this state. This helps reduce the overall power consumption for the device.

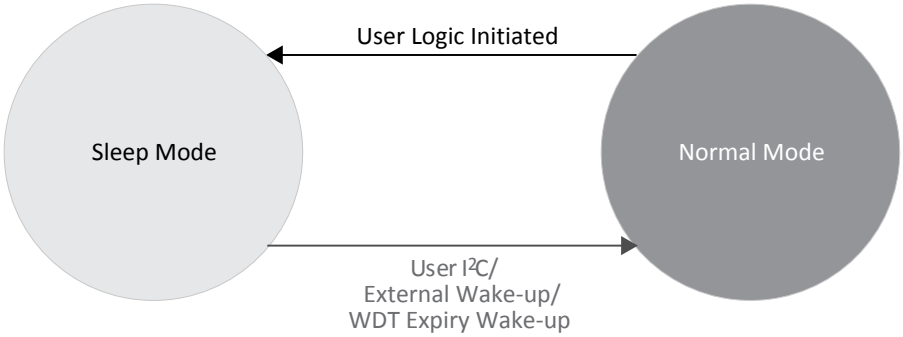

Figure 4.4. CrossLink PMU State Machine

For more details, refer to FPGA-TN-02018, Power Management and Calculation for CrossLink Devices.

4.4.3. Device Configuration

The CrossLink SRAM can be configured as follows:

- Internal Non Volatile Configuration Memory (NVCM)
  - NVCM can be programmed using either the SPI or I²C port
- Standard Serial Peripheral Interface (Master SPI Mode) Interface to external SPI Flash
- System microprocessor to drive a serial Slave SPI port (SSPI mode)
- System microprocessor to drive a serial Slave I²C port

For more information, refer to FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide. In addition to the flexible configuration modes, the CrossLink configuration engine supports the following special features:

- TransFR (Transparent Field Reconfiguration) allowing users to update logic in field without interrupting system operation by freezing I/O states during configuration
- Dual-Boot Support for primary and golden bitstreams provides automatic recovery from configuration failures
- Security and One-Time Programmable (OTP) modes protect bitstream integrity and prevent readback
- 64-bit unique TraceID per device

4.4.4. User I²C IP

CrossLink devices have two I²C IP cores that can be configured either as an I²C master or as an I²C slave. The I2C0 core has pre-assigned pins, and supports PMU wakeup over I²C. The pins for the I2C1 interface are not pre-assigned – user can use any General Purpose I/O pins.

The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I²C, refer to FPGA-TN-02019, CrossLink I2C Hardened IP Usage Guide.

5. DC and Switching Characteristics

5.1. Absolute Maximum Ratings

Table 5.1. Absolute Maximum Ratings[1, 2, 3]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Core Supply Voltage	–0.5	1.32	V
V_{CCPLL}	PLL Supply Voltage	–0.5	1.32	V
V_{CCAUX}	Auxiliary Supply Voltage for Bank 1, 2 and NVCM	–0.5	2.75	V
V_{CCIO}	I/O Driver Supply Voltage for Banks 0, 1, 2	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CC_DPHY} V_{CCA_DPHY} V_{CCPLL_DPHY} V_{CCMU_DPHY}	MIPI D-PHY Supply Voltages	–0.5	1.32	V
—	Voltage Applied on MIPI D-PHY Pins	–0.5	1.32	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature (TJ)	—	+125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

5.2. Recommended Operating Conditions

Table 5.2. Recommended Operating Conditions[1, 2]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V
V_{CCAUX}	Auxiliary Supply Voltage for Bank 1, 2 and NVCM	2.375	2.625	V
V_{CCIO}	I/O Driver Supply Voltage for Bank 0, 1, 2	1.14	3.465	V
T_{JIND}	Junction Temperature, Industrial Operation	–40	100	°C
D-PHY External Power Supply				
V_{CC_DPHYx}	Supply Voltage for D-PHY	1.14	1.26	V
V_{CCA_DPHYx}	Analog Supply Voltage for D-PHY	1.14	1.26	V
V_{CCPLL_DPHYx}	PLL Supply voltage for D-PHY	1.14	1.26	V
V_{CCMU_DPHY}	Supply for V_{CC_DPHY1}, V_{CCA_DPHY1} and V_{CCPLL_DPHY1} on the WLCSP36	1.14	1.26	V

Notes:

1. For Correct Operation, all supplies must be held in their valid operation range.
2. Like power supplies, must be tied together if they are at the same supply voltage. Follow the noise filtering recommendations in FPGA-TN-02013, CrossLink Hardware Checklist.

5.8. Preliminary Power Management Unit (PMU) Timing

Table 5.7. Preliminary PMU Timing[1]

Symbol	Parameter	Device	Max	Unit
$t_{PMUWAKE}$	Time for PMU to wake from Sleep mode	All Devices	1	ms

Note:

1. For details on PMU usage, refer to FPGA-TN-02018, Power Management and Calculation for CrossLink Devices.

5.9. sysI/O Recommended Operating Conditions

Table 5.8. sysI/O Recommended Operating Conditions[1]

Standard	V_{CCIO}		
	Min	Typ	Max
LVCMOS33/LVTTL33	3.135	3.30	3.465
LVCMOS25	2.375	2.50	2.625
LVCMOS18	1.710	1.80	1.890
LVCMOS12 (Output only)	1.140	1.20	1.260
subLDVS (Input only)	2.375	2.50	2.625
SLVS (Input only)[2]	2.375	2.50	2.625
LVDS	2.375	2.50	2.625
MIPI (Input only)	1.140	1.20	1.260

Note:

1. For input voltage compatibility, refer to FPGA-TN-02016, CrossLink sysI/O Usage Guide.
2. For SLVS/MIPI interface I/O placement, see the Programmable I/O Banks section.

5.10. Preliminary sysI/O Single-Ended DC Electrical Characteristics

Table 5.9. Preliminary sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL} (mA)	I_{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS33/ LVTTL33	–0.3	0.8	2.0	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	8	–8
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS25	–0.3	0.7	1.7	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	6	–6
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	4	–4
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS12 (Output only)	—	—	—	—	0.40	V_{CCIO} – 0.4	2	–2
					0.20	V_{CCIO} – 0.2	0.1	–0.1

5.13. Preliminary CrossLink External Switching Characteristics

Over recommended commercial operating conditions.

Table 5.13. Preliminary CrossLink External Switching Characteristics[4, 5]

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Clocks					
Primary Clock					
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	150	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	ns
t_{ISKEW_PRI}	Primary Clock Skew Within a Clock	—	—	450	ps
Edge Clock					
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	600	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	0.783	—	ns
t_{ISKEW_EDGE}	Edge Clock Skew Within a Bank	—	—	120	ps
Generic SDR Interface[1]					
General Purpose I/O Pin Parameters Using Clock Tree Without PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	6.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	—	–0.90	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.82	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	—	1.02	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	—	0	—	ns
General Purpose I/O Pin Parameters Using Clock Tree With PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	5.2	ns
t_{SU}	Clock to Data Setup – PIO Input Register	—	0.17	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.01	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	—	1.70	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	—	0	—	ns
Generic DDR Interfaces[2]					
Generic DDRX8 or DDRX4 I/O with Clock and Data Centered at General Purpose Pins (GDDRX8_RX/TX.ECLK.Centered or GDDRX4_RX/TX.ECLK.Centered)					
$t_{SU\_GDDRX4\_8}$	Input Data Set-Up Before CLK Rising and Falling edges	—	0.167	—	ns
$t_{HO\_GDDRX4\_8}$	Input Data Hold After CLK Rising and Falling edges	—	0.167	—	ns
$t_{DVB\_GDDRX4\_8}$	Output Data Valid Before CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	–0.120	—	ns+1/2UI
$t_{DVA\_GDDRX4\_8}$	Output Data Valid After CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	–0.120	—	ns+1/2UI
$f_{MAX\_GDDRX4\_8}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz

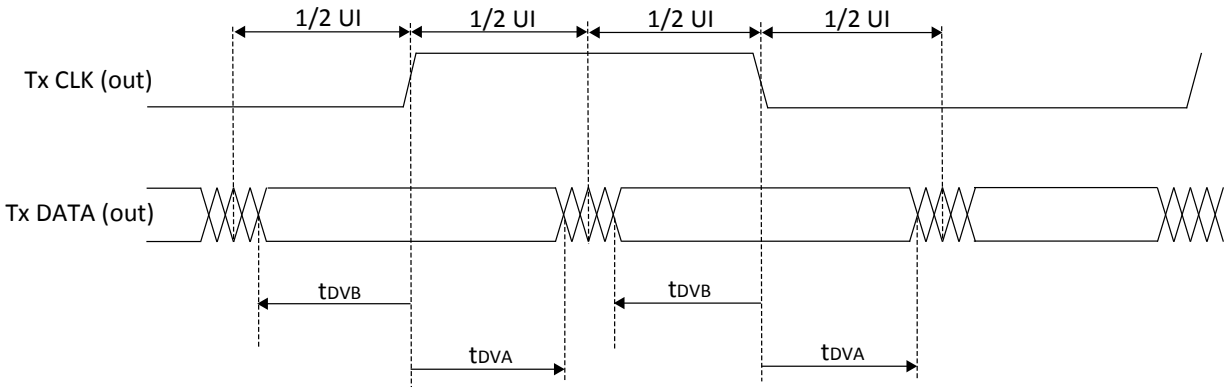

Figure 5.3. Transmit TX.CLK.Centered Output Waveforms

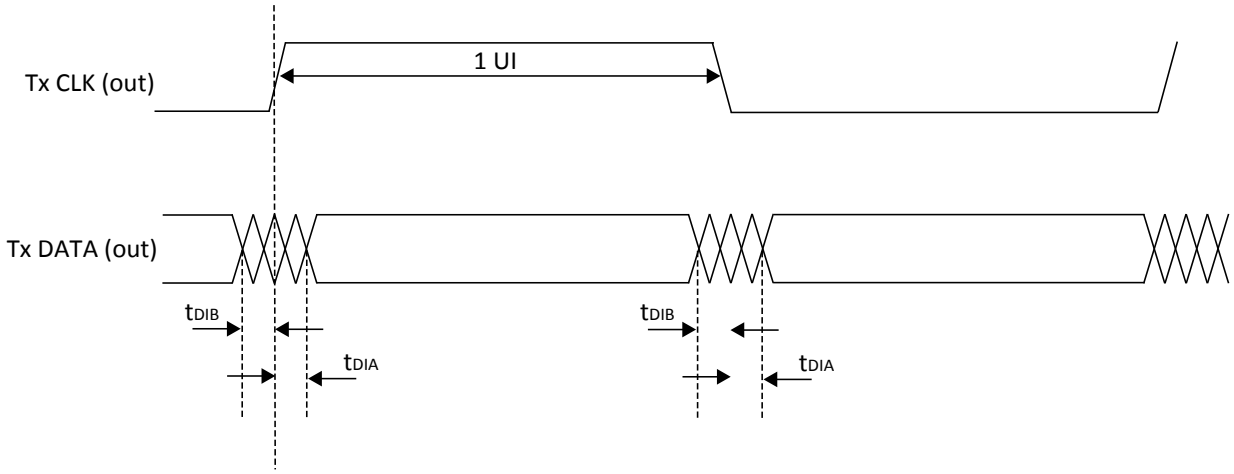

Figure 5.4. Transmit TX.CLK.Aligned Waveforms

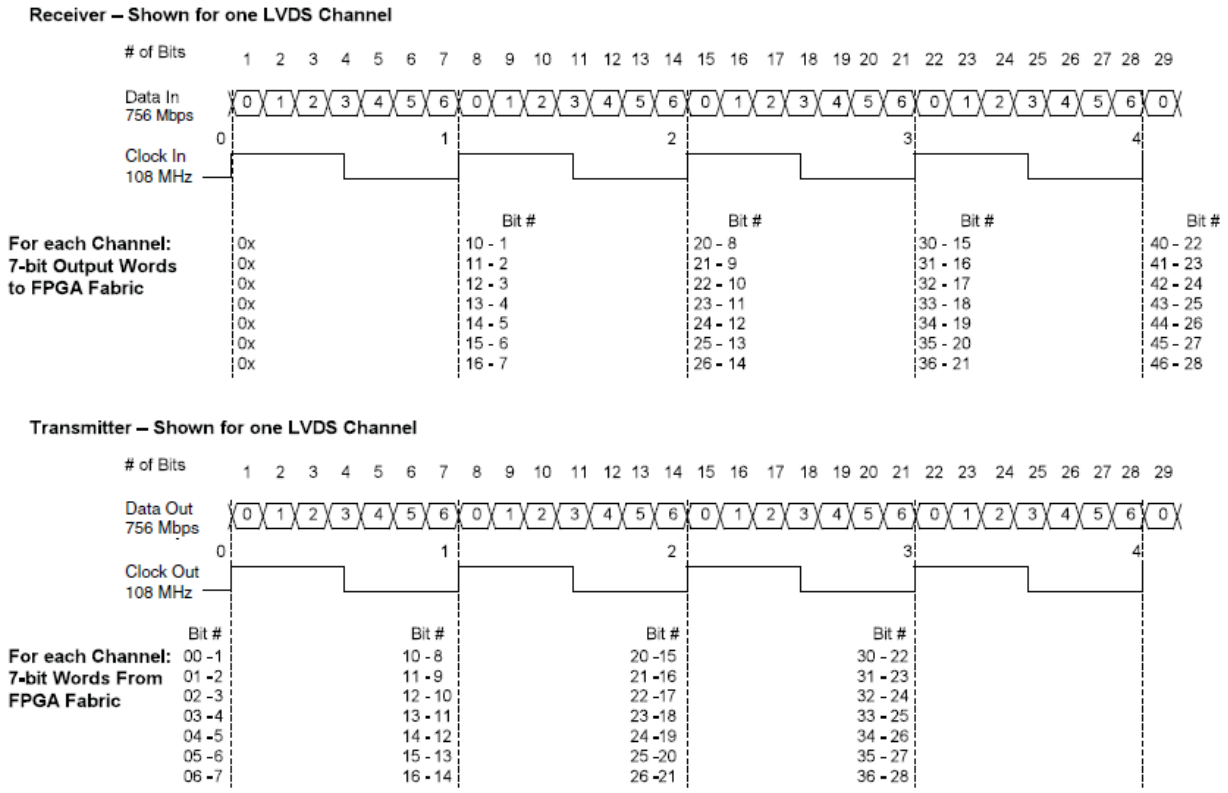

Figure 5.5. DDRX71, DDRX141 Video Timing Waveforms

5.18. CrossLink sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 5.20. CrossLink sysCONFIG Port Timing Specifications

Symbol	Parameter	Min	Max	Unit
All Configuration Mode				
t_{PRGM}	CRESETB LOW Pulse Accepted	145	—	ns
Slave SPI				
f_{CCLK}	SPI_SCK Input Clock Frequency	—	110	MHz
t_{STSU}	MOSI Setup Time	0.5	—	ns
t_{STH}	MOSI Hold Time	2.0	—	ns
t_{STCO}	SPI_SCK Falling Edge to Valid MISO Output	—	13.3	ns
t_{SCS}	Chip Select HIGH Time	42	—	ns
t_{SCSS}	Chip Select Setup Time	0.5	—	ns
t_{SCSH}	Chip Select Hold Time	0.5	—	ns
Master SPI				
f_{CCLK}	MCK Output Clock Frequency	—	52.8	MHz
I^2C*				
f_{MAX}	Maximum SCL Clock Frequency (Fast-Mode Plus	—	1	MHz

***Note**: Refer to the I^2C specification for timing requirements when configuring with I^2C port.

5.19. Preliminary SRAM Configuration Time from NVCM

Over recommended operating conditions.

Table 5.21. Preliminary SRAM Configuration Time from NVCM

Symbol	Parameter	Typ	Unit
$t_{CONFIGURATION}$	POR to Device I/O Active[1]	83	ms

Note:

1. Before and during configuration, the I/Os are held in tristate with weak internal pullups enabled. I/Os are released to user functionality when the device has finished configuration.

6.2. ucfBGA64 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
A2	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A3	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
A4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
A5	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A6	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
A7	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
A8	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
B1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
B2	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
B3	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
B4	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
B5	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B6	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
B7	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
B8	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
C1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
C2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
C3	PB47	0	PCLKT0_0/USER_SDA	—
C4	VCCPLL_DPHYX	DPHY	—	—
C5	VCCA_DPHYX	DPHY	—	—
C6	GNDA_DPHYX	GND	—	—
C7	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
C8	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
D1	PB34B	1	—	Comp_OF_PB34A
D2	PB34A	1	GR_PCLK1_0	True_OF_PB34B
D3	PB52	0	SPI_SS/CSN/SCL	—
D4	GND	GND	—	—
D5	VCC	VCC	—	—
D6	VCCAUX	VCCAUX	—	—
D7	PB16A	2	PCLKT2_0	True_OF_PB16B
D8	PB12A	2	GPLLT2_0	True_OF_PB12B
E1	PB51	0	MISO	—
E2	CRESET_B	0	—	—
E3	PB48	0	PCLKT0_1/USER_SCL	—
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCCIO2	2	—	—
E7	PB16B	2	PCLKC2_0	Comp_OF_PB16A
E8	PB12B	2	GPLLC2_0	Comp_OF_PB12A
F1	PB53	0	SPI_SCK/MCK/SDA	—
F2	PB50	0	MOSI	—

ucfBGA64 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
F3	VCCIO0	0	—	—
F4	VCCIO1	1	—	—
F5	GND	GND	—	—
F6	VCCIO2	2	—	—
F7	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F8	PB6B	2	—	Comp_OF_PB6A
G1	PB38D	1	—	Comp_OF_PB38C
G2	PB38C	1	—	True_OF_PB38D
G3	PB49	0	PMU_WKUPN/CDONE	—
G4	VCCGPLL	VCCGPLL	—	—
G5	PB29B	1	PCLKC1_0	Comp_OF_PB29A
G6	PB29A	1	PCLKT1_0	True_OF_PB29B
G7	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
G8	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
H1	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
H2	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
H3	PB29C	1	PCLKT1_1	True_OF_PB29D
H4	PB29D	1	PCLKC1_1	Comp_OF_PB29C
H5	PB16D	2	PCLKC2_1	Comp_OF_PB16C
H6	PB16C	2	PCLKT2_1	True_OF_PB16D
H7	PB12D	2	—	Comp_OF_PB12C
H8	PB12C	2	—	True_OF_PB12D

6.4. csfBGA81 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
A2	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A3	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
A4	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
A5	VCCA_DPHY1	DPHY1	—	—
A6	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A7	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
A8	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
A9	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
B1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
B3	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
B4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
B5	GNDPLL_DPHYX	GND	—	—
B6	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B7	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
B8	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
B9	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
C1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
C2	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
C3	GNDA_DPHY1	DPHY1	—	—
C4	VCCPLL_DPHY1	DPHY1	—	—
C5	GND	GND	—	—
C6	VCCPLL_DPHY0	DPHY0	—	—
C7	GNDA_DPHY0	DPHY0	—	—
C8	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
C9	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
D1	PB34A	1	GR_PCLK1_0	True_OF_PB34B
D2	PB34B	1	—	Comp_OF_PB34A
D3	VCCA_DPHY1	DPHY1	—	—
D4	GND	GND	—	—
D5	VCCAUX	VCCAUX	—	—
D6	GND	GND	—	—
D7	VCCA_DPHY0	DPHY0	—	—
D8	PB16B	2	PCLKC2_0	Comp_OF_PB16A
D9	PB16A	2	PCLKT2_0	True_OF_PB16B
E1	PB38A	1	—	True_OF_PB38B
E2	PB38B	1	—	Comp_OF_PB38A
E3	VCC	VCC	—	—
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCCIO2	2	—	—

6.5. Dual Function Pin Descriptions

The following table describes the dual functions available to certain pins on the CrossLink device. These pins may alternatively be used as general purpose I/O when the described dual function is not enabled.

Signal Name	I/O	Description
General Purpose		
USER_SCL	I/O	User Slave I2C0 clock input and Master I²C0 clock output. Enables PMU wake-up via I2C0.
USER_SDA	I/O	User Slave I2C0 data input and Master I²C0 data output. Enables PMU wakeup via I2C0.
PMU_WKUPN	—	This pin wakes the PMU from sleep mode when toggled low.
Clock Functions		
GPLL2_0[T, C]_IN	I	General Purpose PLL (GPLL) input pads: T = true and C = complement. These pins can be used to input a reference clock directly to the General Purpose PLL. These pins do not provide direct access to the primary clock network.
GR_PCLK[Bank]0	I	These pins provide a short General Routing path to the primary clock network. Refer to FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide for details.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins provide direct access to the primary and edge clock networks.
MIPI_CLK[T/C][Bank]_0	I/O	MIPI D-PHY Reference CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins can be used to input a reference clock directly to the D-PHY PLLs. These pins do not provide direct access to the primary clock network.
Configuration		
CDONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. Holding CDONE delays configuration.
SPI_SCK	I	Input Configuration Clock for configuring CrossLink in Slave SPI mode (SSPI).
MCK	O	Output Configuration Clock for configuring CrossLink in Master SPI mode (MSPI).
SPI_SS	I	Input Chip Select for configuring CrossLink in Slave SPI mode (SSPI).
CSN	O	Output Chip Select for configuring CrossLink in Master SPI mode (MSPI).
MOSI	I/O	Data Output when configuring CrossLink in Master SPI mode (MSPI), data input when configuring CrossLink in Slave SPI mode (SSPI).
MISO	I/O	Data Input when configuring CrossLink in Master SPI mode (MSPI), data output when configuring CrossLink in Slave SPI mode (SSPI).
SCL	I/O	Slave I²C clock I/O when configuring CrossLink in I²C mode.
SDA	I/O	Slave I²C data I/O when configuring CrossLink in I²C mode.

6.6. Dedicated Function Pin Descriptions

Signal Name	I/O	Description
Configuration		
CRESET_B	I	Configuration Reset, active LOW.
MIPI D-PHY		
DPHY[num]_CK[P/N]	I/O	MIPI D-PHY Clock [num] = D-PHY 0 or 1, P = Positive, N = Negative.
DPHY[num]_D[P/N][lane]	I/O	MIPI D-PHY Data [num] = D-PHY 0 or 1, P = Positive, N = Negative, Lane = data lane in the D-PHY block 0, 1, 2 or 3.

6.7. Pin Information Summary

Pin Type	CrossLink			
	WLCSP36	ucfBGA64	ctfBGA80	csfBGA81
General Purpose I/O per Bank				
Bank 0	7	6	7	7
Bank 1	0	10	14	14
Bank 2	10	12	16	16
Total General Purpose Single Ended IO	**17**	**28**	**37**	**37**
Differential I/O pairs per Bank				
Bank 0	0	0	0	0
Bank 1	0	5	7	7
Bank 2	5	6	8	8
Total General Purpose Differential I/O pairs	5	11	15	15
D-PHY	1	2	2	2
D-PHY Clock/Data	10	20	20	20
D-PHY VCC	1	2	4	4
D-PHY GND	1	1	3	3
VCC/VCCIOx/VCCAUX/VCCGPLL	4	8	9	10
GND	3	4	9	9
CRESETB	1	1	1	1
Total Balls	**36**	**64**	**80**	**81**

References

For more information, refer to the following technical notes:

- FPGA-TN-02012, CrossLink High-Speed I/O Interface
- FPGA-TN-02013, CrossLink Hardware Checklist
- FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide
- FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide
- FPGA-TN-02016, CrossLink sysI/O Usage Guide
- FPGA-TN-02017, CrossLink Memory Usage Guide
- FPGA-TN-02018, Power Management and Calculation for CrossLink Devices
- FPGA-TN-02019, CrossLink I2C Hardened IP Usage Guide
- FPGA-TN-02020, Advanced CrossLink I2C Hardened IP Reference Guide

For package information, refer to the following technical notes:

- TN1074, PCB Layout Recommendations for BGA Packages
- TN1076, Solder Reflow Guide for Surface Mount Devices
- TN1242, Wafer-Level Chip-Scale Package Guide
- Thermal Management
- Package Diagrams

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- MIPI Standards (D-PHY): www.mipi.org

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
March 2017	1.1	Updated I/O placements on banks containing MIPI interface in Programmable I/O Banks section. Updated DC and Switching Characteristics section: • Updated Table 5.4. Preliminary Power-On-Reset Voltage Levels1, [3, 4], added row of V_{PORDN} • Added Note 5 to Table 5.5. Preliminary DC Electrical Characteristics • Updated Table 5.6. Preliminary CrossLink Supply Current, added notes • Updated max values of V_{THD} and $V_{THD(subLVDS)}$ in Table 5.10. LVDS/subLVDS1/SLVS1, [2] • Maximum input frequency values of subLVDS and SLVS are TBD in Table 5.12. Preliminary CrossLink Maximum I/O Buffer Speed • Updated Table 5.13. Preliminary CrossLink External Switching Characteristics4, [5] • Updated min values of t_{SU_MIPIX4} and t_{HO_MIPIX4} in Table 5.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s) and Table 5.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s) • Updated Table 5.20. CrossLink sysCONFIG Port Timing Specifications • Updated Table 5.21. Preliminary SRAM Configuration Time from NVCM Updated Pinout Information section Updated CrossLink Part Number Description
July 2016	1.0	Updated document numbers.
May 2016	1.0	First preliminary release.