**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-8FX |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, LINbus, SIO, UART/USART |
| Peripherals | LCD, LVD, POR, PWM, WDT |
| Number of I/O | 52 |
| Program Memory Size | 60KB (60K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb95f168japmc-ge1 |

*(Continued)*

| Parameter \ Part number | | MB95168MA | MB95F168MA | MB95F168NA | MB95F168JA |
|---|---|---|---|---|---|
| Peripheral functions | LCD controller (LCDC) | COM output : 4 (Max)<br>SEG output : 32 (Max)<br>LCD drive power supply (bias) pin : 4<br>32 SEG × 4 COM : 128 pixels can be displayed.<br>Duty LCD mode<br>Operable in LCD standby mode<br>With blinking function<br>Built-in division resistance for LCD drive | | | |
| | 8/16-bit compound timer (2 channels) | Each channel of the timer can be used as "8-bit timer × 2 channels" or "16-bit timer × 1 channel".<br>Built-in timer function, PWC function, PWM function, capture function, and square wave form output<br>Count clock : 7 internal clocks and external clock can be selected. | | | |
| | 16-bit PPG (1 channel) | PWM mode or one-shot mode can be selected.<br>Counter operating clock : Eight selectable clock sources<br>Support for external trigger start | | | |
| | 8/16-bit PPG (2 channels) | Each channel of the PPG can be used as "8-bit PPG × 2 channels" or "16-bit PPG × 1 channel".<br>Counter operating clock : Eight selectable clock sources | | | |
| | Watch counter | Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s)<br>Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60) | | | |
| | Watch prescaler (1 channel) | 4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s) | | | |
| | External interrupt (8 channels) | Interrupt by edge detection (rising, falling, or both edges can be selected.)<br>Can be used to recover from standby modes. | | | |
| Flash memory | | — | Supports automatic programming, Embedded Algorithm<br>Write/Erase/Erase-Suspend/Resume commands<br>A flag indicating completion of the algorithm<br>Number of write/erase cycles (Minimum) : 10000 times<br>Data retention time: 20 years<br>Erase can be performed on each block<br>Block protection with external programming voltage<br>Flash Security Feature for protecting the content of the Flash | | |
| Standby mode | | Sleep, stop, watch, and time-base timer | | | |

* : For details of option, refer to "■ MASK OPTION".

Note : Part number of evaluation product in MB95160MA series is MB95FV100D-103. When using it, the MCU board (MB2146-303A-E) is required.

## ■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

• Notes on Using Evaluation Products

The evaluation product has not only the functions of the MB95160MA series but also those of other products to support software development for multiple series and models of the F²MC-8FX family. The I/O addresses for peripheral resources not used by the MB95160MA series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Particularly, do not use word access to odd numbered byte address in the prohibited areas (If these access are used, the address may be read or written unexpectedly).

Also, as the read values of prohibited addresses on the evaluation product are different to the values on the Flash memory products or Mask ROM products, do not use these values in the program.

The functions corresponding to certain bits in single-byte registers may not be supported depending on the type of Flash memory products and Mask ROM products. However, reading or writing to these bits will not cause malfunction of the hardware. Also, the products with either evaluation, Flash memory or Mask ROM are designed to have the same operation in software and hardware.

• Difference of Memory Spaces

If the amount of memory on the evaluation product is different from that of the Flash memory and Mask ROM products, carefully check the difference in the amount of memory from the model to be actually used when developing software.

For details of memory space, refer to “■ CPU CORE”.

• Current Consumption

Current in Flash memory products is consumed more than Mask ROM products.
For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

• Package

For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSIONS”.

• Operating voltage

The operating voltage is different among the evaluation, Flash memory products and Mask ROM products.

For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”

## ■ PIN DESCRIPTION

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 1 | $AV_{CC}$ | — | A/D converter power supply pin |
| 2 | AVR | — | A/D converter reference input pin |
| 3 | P14/PPG0 | H | General-purpose I/O port.<br>The pin is shared with 16-bit PPG ch.0 output. |
| 4 | P13/TRG0/ ADTG | | General-purpose I/O port.<br>The pin is shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D converter trigger input (ADTG) . |
| 5 | P12/UCK0 | | General-purpose I/O port.<br>The pin is shared with UART/SIO ch.0 clock I/O. |
| 6 | P11/UO0 | | General-purpose I/O port.<br>The pin is shared with UART/SIO ch.0 data output. |
| 7 | P10/UI0 | G | General-purpose I/O port.<br>The pin is shared with UART/SIO ch.0 data input. |
| 8 | P24/EC0/ SDA0 | I | General-purpose I/O port.<br>The pin is shared with 8/16-bit compound timer ch.0 clock input (EC0) and $I^2C$ ch.0 data I/O (SDA0) . |
| 9 | P23/TO01/ SCL0 | | General-purpose I/O port.<br>The pin is shared with 8/16-bit compound timer ch.0 output (TO01) and $I^2C$ ch.0 clock I/O (SCL0) . |
| 10 | P22/TO00 | H | General-purpose I/O port.<br>The pin is shared with 8/16-bit compound timer ch.0 output. |
| 11 | P21/PPG01 | | General-purpose I/O port.<br>The pin is shared with 8/16-bit PPG ch.0 output. |
| 12 | P20/PPG00 | | General-purpose I/O port.<br>The pin is shared with 8/16-bit PPG ch.0 output. |
| 13 | MOD | B | Operating mode designation pin |
| 14 | X0 | A | Main clock oscillation pins |
| 15 | X1 | | |
| 16 | $V_{SS}$ | — | Power supply pin (GND) |
| 17 | $V_{CC}$ | — | Power supply pin |
| 18 | C | — | Capacitor connection pin |
| 19 | X1A | A | Sub clock oscillation pins (32 kHz) |
| 20 | X0A | | |
| 21 | $\overline{RST}$ | B’ | Reset pin |
| 22 | P90/V3 | R | General-purpose I/O ports.<br>The pins are shared with power supply pin for LCDC drive. |
| 23 | P91/V2 | | |
| 24 | P92/V1 | | |
| 25 | P93/V0 | | |

*(Continued)*

• Mode Pin (MOD)

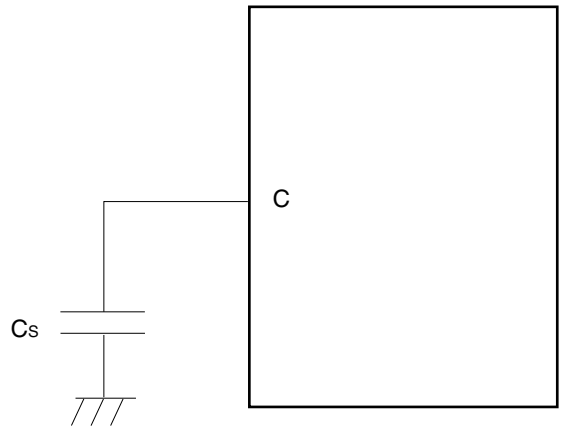
Connect the MOD pin directly to $V_{CC}$ or $V_{SS}$.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pin to $V_{CC}$ or $V_{SS}$ and to provide a low-impedance connection.

• C Pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of $V_{CC}$ pin must have a capacitance value higher than $C_S$. For connection of smoothing capacitor $C_S$, refer to the diagram below.

• C pin connection diagram




• Analog Power Supply

Always set the same potential to $AV_{CC}$ and $V_{CC}$ pins. When $V_{CC} > AV_{CC}$, the current may flow through the AN00 to AN07 pins.

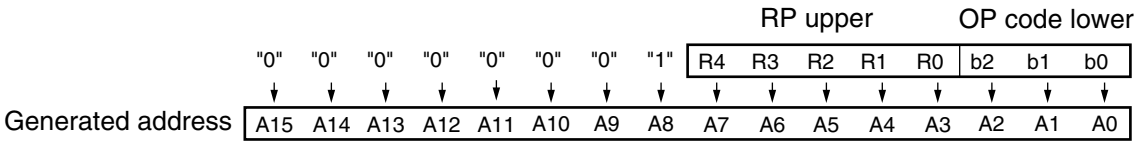
• Treatment of Power Supply Pins on A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter is not in use.

Noise riding on the $AV_{CC}$ pin may cause accuracy degradation. So, connect approx. 0.1 μF ceramic capacitor as a bypass capacitor between $AV_{CC}$ and $AV_{SS}$ pins in the vicinity of this device.

The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

• Rule for Conversion of Actual Addresses in the General-purpose Register Area




The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to $0080_H$ to $00FF_H$.

| Direct bank pointer (DP2 to DP0) | Specified address area | Mapping area |
|---|---|---|
| $XXX_B$ (no effect to mapping) | $0000_H$ to $007F_H$ | $0000_H$ to $007F_H$ (without mapping) |
| $000_B$ (initial value) | $0080_H$ to $00FF_H$ | $0080_H$ to $00FF_H$ (without mapping) |
| $001_B$ | | $0100_H$ to $017F_H$ |
| $010_B$ | | $0180_H$ to $01FF_H$ |
| $011_B$ | | $0200_H$ to $027F_H$ |
| $100_B$ | | $0280_H$ to $02FF_H$ |
| $101_B$ | | $0300_H$ to $037F_H$ |
| $110_B$ | | $0380_H$ to $03FF_H$ |
| $111_B$ | | $0400_H$ to $047F_H$ |

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

H flag : Set to “1” when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. This flag is for decimal adjustment instructions.

I flag : Interrupt is enabled when this flag is set to “1”. Interrupt is disabled when this flag is set to “0”. The flag is set to “0” when reset.

IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

| IL1 | IL0 | Interrupt level | Priority |
|---|---|---|---|
| 0 | 0 | 0 | High |
| 0 | 1 | 1 | ↕ |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | Low (no interruption) |

N flag : Set to “1” if the MSB is set to “1” as the result of an arithmetic operation. Cleared to “0” when the bit is set to “0”.

Z flag : Set to “1” when an arithmetic operation results in “0”. Cleared to “0” otherwise.

V flag : Set to “1” if the complement on 2 overflows as a result of an arithmetic operation. Cleared to “0” otherwise.

C flag : Set to “1” when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. Set to the shift-out value in the case of a shift instruction.

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0059H | TDR0 | UART/SIO serial output data register ch.0 | R/W | 00000000B |
| 005AH | RDR0 | UART/SIO serial input data register ch.0 | R | 00000000B |
| 005BH to 005FH | — | (Disabled) | — | — |
| 0060H | IBCR00 | I²C bus control register 0 ch.0 | R/W | 00000000B |
| 0061H | IBCR10 | I²C bus control register 1 ch.0 | R/W | 00000000B |
| 0062H | IBSR0 | I²C bus status register ch.0 | R | 00000000B |
| 0063H | IDDR0 | I²C data register ch.0 | R/W | 00000000B |
| 0064H | IAAR0 | I²C address register ch.0 | R/W | 00000000B |
| 0065H | ICCR0 | I²C clock control register ch.0 | R/W | 00000000B |
| 0066H to 006BH | — | (Disabled) | — | — |
| 006CH | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000B |
| 006DH | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000B |
| 006EH | ADDH | 8/10-bit A/D converter data register (upper byte) | R/W | 00000000B |
| 006FH | ADDL | 8/10-bit A/D converter data register (lower byte) | R/W | 00000000B |
| 0070H | WCSR | Watch counter status register | R/W | 00000000B |
| 0071H | — | (Disabled) | — | — |
| 0072H | FSR | Flash memory status register | R/W | 000X0000B |
| 0073H | SWRE0 | Flash memory sector writing control register 0 | R/W | 00000000B |
| 0074H | SWRE1 | Flash memory sector writing control register 1 | R/W | 00000000B |
| 0075H | — | (Disabled) | — | — |
| 0076H | WREN | Wild register address compare enable register | R/W | 00000000B |
| 0077H | WROR | Wild register data test setting register | R/W | 00000000B |
| 0078H | — | Register bank pointer (RP) , Mirror of direct bank pointer (DP) | — | — |
| 0079H | ILR0 | Interrupt level setting register 0 | R/W | 11111111B |
| 007AH | ILR1 | Interrupt level setting register 1 | R/W | 11111111B |
| 007BH | ILR2 | Interrupt level setting register 2 | R/W | 11111111B |
| 007CH | ILR3 | Interrupt level setting register 3 | R/W | 11111111B |
| 007DH | ILR4 | Interrupt level setting register 4 | R/W | 11111111B |
| 007EH | ILR5 | Interrupt level setting register 5 | R/W | 11111111B |
| 007FH | — | (Disabled) | — | — |
| 0F80H | WRARH0 | Wild register address setting register (upper byte) ch.0 | R/W | 00000000B |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0FAA$_H$ | PDCRH0 | 16-bit PPG down counter register (upper byte) ch.0 | R | 00000000$_B$ |
| 0FAB$_H$ | PDCRL0 | 16-bit PPG down counter register (lower byte) ch.0 | R | 00000000$_B$ |
| 0FAC$_H$ | PCSRH0 | 16-bit PPG cycle setting buffer register (upper byte) ch.0 | R/W | 11111111$_B$ |
| 0FAD$_H$ | PCSRL0 | 16-bit PPG cycle setting buffer register (lower byte) ch.0 | R/W | 11111111$_B$ |
| 0FAE$_H$ | PDUTH0 | 16-bit PPG duty setting buffer register (upper byte) ch.0 | R/W | 11111111$_B$ |
| 0FAF$_H$ | PDUTL0 | 16-bit PPG duty setting buffer register (lower byte) ch.0 | R/W | 11111111$_B$ |
| 0FB0$_H$ to 0FBB$_H$ | — | (Disabled) | — | — |
| 0FBC$_H$ | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000$_B$ |
| 0FBD$_H$ | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000$_B$ |
| 0FBE$_H$ | PSSR0 | UART/SIO dedicated baud rate generator prescaler selecting register ch.0 | R/W | 00000000$_B$ |
| 0FBF$_H$ | BRSR0 | UART/SIO dedicated baud rate generator setting register ch.0 | R/W | 00000000$_B$ |
| 0FC0$_H$ to 0FC2$_H$ | — | (Disabled) | — | — |
| 0FC3$_H$ | AIDRL | A/D input disable register (lower byte) | R/W | 00000000$_B$ |
| 0FC4$_H$ | LCDCC | LCDC control register | R/W | 00010000$_B$ |
| 0FC5$_H$ | LCDCE1 | LCDC enable register 1 | R/W | 00110000$_B$ |
| 0FC6$_H$ | LCDCE2 | LCDC enable register 2 | R/W | 00000000$_B$ |
| 0FC7$_H$ | LCDCE3 | LCDC enable register 3 | R/W | 00000000$_B$ |
| 0FC8$_H$ | LCDCE4 | LCDC enable register 4 | R/W | 00000000$_B$ |
| 0FC9$_H$ | LCDCE5 | LCDC enable register 5 | R/W | 00000000$_B$ |
| 0FCA$_H$ | — | (Disabled) | — | — |
| 0FCB$_H$ | LCDCB1 | LCDC blinking setting register 1 | R/W | 00000000$_B$ |
| 0FCC$_H$ | LCDCB2 | LCDC blinking setting register 2 | R/W | 00000000$_B$ |
| 0FCD$_H$ to 0FDC$_H$ | LCDRAM | LCDC display RAM | R/W | 00000000$_B$ |
| 0FDD$_H$ to 0FE2$_H$ | — | (Disabled) | — | — |
| 0FE3$_H$ | WCDR | Watch counter data register | R/W | 00111111$_B$ |

*(Continued)*

### 3. DC Characteristics

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IH1}$ | P10, P67 | *1 | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | When selecting CMOS input level |
| | $V_{IH2}$ | P23, P24 | *1 | 0.7 $V_{CC}$ | — | $V_{SS}$ + 5.5 | V | |
| | $V_{IHA}$ | P00 to P07, P10 to P14, P20 to P22, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Port inputs if Automotive input levels are selected |
| | $V_{IHS1}$ | P00 to P07, P10 to P14, P20 to P22, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | *1 | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Hysteresis input |
| | $V_{IHS2}$ | P23, P24 | *1 | 0.8 $V_{CC}$ | — | $V_{SS}$ + 5.5 | V | |
| | $V_{IHM}$ | $\overline{RST}$, MOD | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{IL}$ | P10,P23, P24,P67 | *1 | $V_{SS}$ − 0.3 | — | 0.3 $V_{CC}$ | V | Hysteresis input (When selecting CMOS input level) |
| | $V_{ILA}$ | P00 to P07, P10 to P14, P20 to P24, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | — | $V_{SS}$ − 0.3 | — | 0.5 $V_{CC}$ | V | Port inputs if Automotive input levels are selected |
| | $V_{ILS}$ | P00 to P07, P10 to P14, P20 to P24, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | *1 | $V_{SS}$ − 0.3 | — | 0.2 $V_{CC}$ | V | Hysteresis input |
| | $V_{ILM}$ | $\overline{RST}$, MOD | — | $V_{SS}$ − 0.3 | — | 0.3 $V_{CC}$ | V | Hysteresis input |
| "H" level output voltage | $V_{OH}$ | All output pins | $I_{OH}$ = − 4.0 mA | $V_{CC}$ − 0.5 | — | — | V | |
| "L" level output voltage | $V_{OL}$ | $\overline{RST}$*2, All output pins | $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | |

*(Continued)*

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current*3 | $I_{CCL}$ | $V_{CC}$ (External clock operation) | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 16 kHz<br>Sub clock mode (divided by 2)<br>$T_A$ = + 25 °C | — | 45 | 100 | µA | |
| | $I_{CCLS}$ | | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 16 kHz<br>Sub sleep mode (divided by 2)<br>$T_A$ = + 25 °C | — | 10 | 81 | µA | |
| | $I_{CCT}$ | | $F_{CL}$ = 32 kHz<br>Watch mode<br>Main stop mode<br>$T_A$ = + 25 °C | — | 4.6 | 27.0 | µA | |
| | $I_{CCMPLL}$ | | $F_{CH}$ = 4 MHz<br>$F_{MP}$ = 10 MHz<br>Main PLL mode (multiplied by 2.5) | — | 9.3 | 12.5 | mA | Flash memory product |
| | | | | — | 7 | 9.5 | mA | Mask ROM product |
| | | | $F_{CH}$ = 6.4 MHz<br>$F_{MP}$ = 16 MHz<br>Main PLL mode (multiplied by 2.5) | — | 14.9 | 20.0 | mA | Flash memory product |
| | | | | — | 11.2 | 15.2 | mA | Mask ROM product |
| | $I_{CCSPLL}$ | | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 128 kHz<br>Sub PLL mode (multiplied by 4),<br>$T_A$ = + 25 °C | — | 160 | 400 | µA | |
| | $I_{CTS}$ | | $F_{CH}$ = 10 MHz<br>Time-base timer mode<br>$T_A$ = + 25 °C | — | 0.15 | 1.10 | mA | |
| | $I_{CCH}$ | | Sub stop mode<br>$T_A$ = + 25 °C | — | 5 | 20 | µA | |
| | $I_A$ | $AV_{CC}$ | $F_{CH}$ = 16 MHz<br>At operating of A/D conversion | — | 2.4 | 4.7 | mA | |
| | $I_{AH}$ | | $F_{CH}$ = 16 MHz<br>At stopping of A/D conversion<br>$T_A$ = + 25 °C | — | 1 | 5 | µA | |
| LCD internal division resistance | $R_{LCD}$ | — | Between V3 and $V_{SS}$ | — | 300 | — | kΩ | |
| COM0 to COM3 output impedance | $R_{VCOM}$ | COM0 to COM3 | V1 to V3 = 5.0 V | — | — | 5 | kΩ | |
| SEG00 to SEG31 output impedance | $R_{VSEG}$ | SEG00 to SEG31 | | — | — | 7 | kΩ | |

*(Continued)*

*(Continued)*

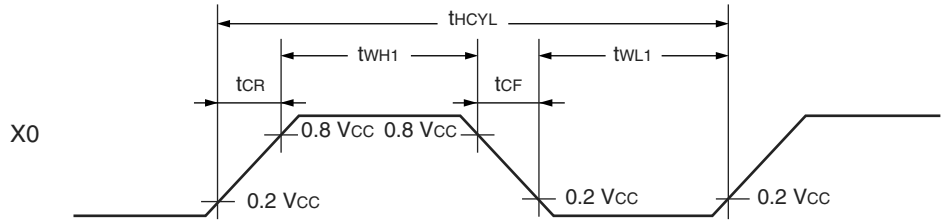
| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| LCD leak current | $I_{LCDL}$ | V0 to V3, COM0 to COM3 SEG00 to SEG31 | — | − 1 | — | + 1 | μA | |

*1 : The input level of P10, P23, P24 and P67 can be switched to either the “CMOS input level” or “hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR) .

*2 : Product without clock supervisor only

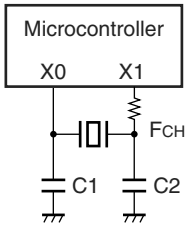
*3 :
- The power-supply current is determined by the external clock. When both low voltage detection option and clock supervisor option are selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit ($I_{LVD}$) and current consumption of built-in CR oscillator ($I_{CSV}$) to the specified value.
- Refer to “4. AC Characteristics (1) Clock Timing” for $F_{CH}$ and $F_{CL}$.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for $F_{MP}$ and $F_{MPL}$.

• Input wave form for using external clock (main clock)

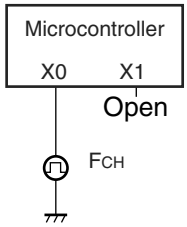



• Figure of Main Clock Input Port External Connection

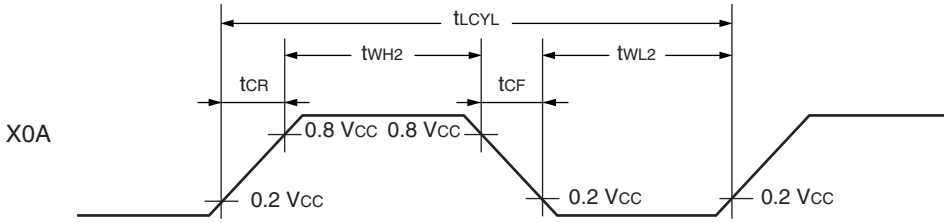
When using a crystal or ceramic oscillator




When using external clock

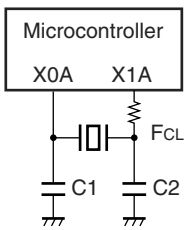



• Input wave form for using external clock (sub clock)

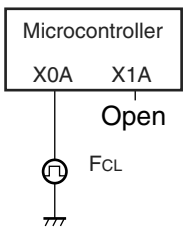



• Figure of Sub clock Input Port External Connection

When using a crystal or ceramic oscillator




When using external clock



### (3) External Reset

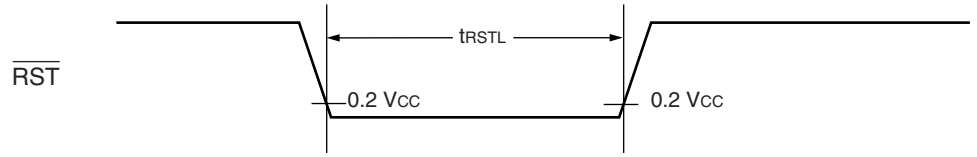
(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| $\overline{RST}$ "L" level pulse width | $t_{RSTL}$ | $\overline{RST}$ | — | 2 $t_{MCLK}$*1 | — | ns | At normal operating |
| | | | | Oscillation time of oscillator*2 + 100 | — | µs | At stop mode, sub clock mode, sub sleep mode, and watch mode |
| | | | | 100 | — | µs | At time-base timer mode |

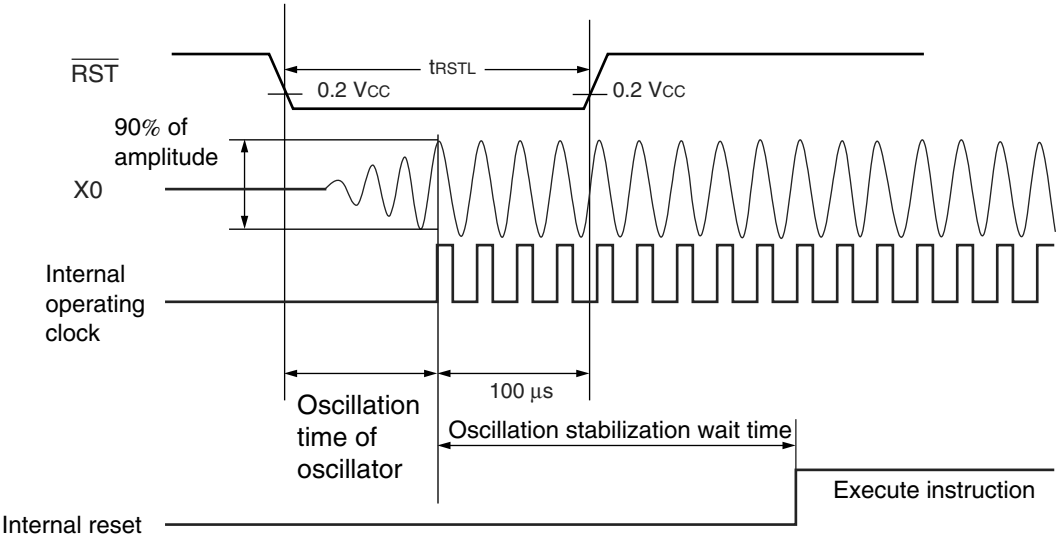
*1 : Refer to " (2) Source Clock/Machine Clock" for $t_{MCLK}$.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

• At normal operating




• At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on

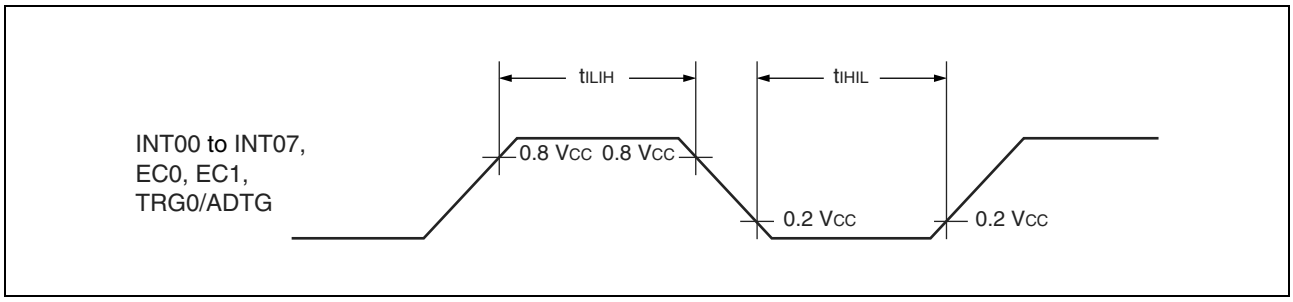


**(5) Peripheral Input Timing**

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Peripheral input "H" pulse width | $t_{ILIH}$ | INT00 to INT07, EC0, EC1, TRG0/ADTG | — | 2 $t_{MCLK}$* | — | ns |
| Peripheral input "L" pulse width | $t_{IHIL}$ | | | 2 $t_{MCLK}$* | — | ns |

* : Refer to " (2) Source Clock/Machine Clock" for $t_{MCLK}$.



**(8) I²C Timing**

($V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Standard-mode | | Fast-mode | | |
| | | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | SCL0 | R = 1.7 kΩ, C = 50 pF*1 | 0 | 100 | 0 | 400 | kHz |
| (Repeat) Start condition hold time SDA ↓ → SCL ↓ | $t_{HD;STA}$ | SCL0 SDA0 | | 4.0 | — | 0.6 | — | µs |
| SCL clock "L" width | $t_{LOW}$ | SCL0 | | 4.7 | — | 1.3 | — | µs |
| SCL clock "H" width | $t_{HIGH}$ | SCL0 | | 4.0 | — | 0.6 | — | µs |
| (Repeat) Start condition setup time SCL ↑ → SDA ↓ | $t_{SU;STA}$ | SCL0 SDA0 | | 4.7 | — | 0.6 | — | µs |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HD;DAT}$ | SCL0 SDA0 | | 0 | 3.45*2 | 0 | 0.9*3 | µs |
| Data setup time SDA ↓ ↑ → SCL ↑ | $t_{SU;DAT}$ | SCL0 SDA0 | | 0.25*4 | — | 0.1*4 | — | µs |
| Stop condition setup time SCL ↑ → SDA ↑ | $t_{SU;STO}$ | SCL0 SDA0 | | 4.0 | — | 0.6 | — | µs |
| Bus free time between stop condition and start condition | $t_{BUF}$ | SCL0 SDA0 | | 4.7 | — | 1.3 | — | µs |

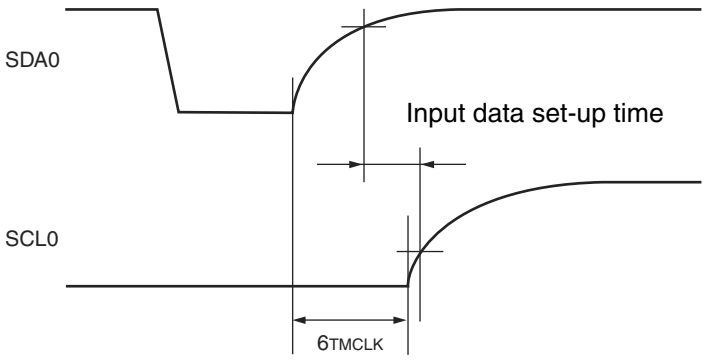
*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum $t_{HD;DAT}$ have only to be met if the device dose not stretch the "L" width ($t_{LOW}$) of the SCL signal.

*3 : A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must then be met.

*4 : Refer to " • Note of SDA and SCL set-up time".

• Note of SDA and SCL set-up time




The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

*(Continued)*

($V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value*2 | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Stop condition detection | $t_{SU;STO}$ | SCL0 SDA0 | R = 1.7 kΩ, C = 50 pF*1 | 2 $t_{MCLK}$ – 20 | — | ns | Undetected when 1 $t_{MCLK}$ is used at reception |
| Restart condition detection condition | $t_{SU;STA}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | Undetected when 1 $t_{MCLK}$ is used at reception |
| Bus free time | $t_{BUF}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | At reception |
| Data hold time | $t_{HD;DAT}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | At slave transmission mode |
| Data setup time | $t_{SU;DAT}$ | SCL0 SDA0 | | $t_{LOW}$ – 3 $t_{MCLK}$ – 20 | — | ns | At slave transmission mode |
| Data hold time | $t_{HD;DAT}$ | SCL0 SDA0 | | 0 | — | ns | At reception |
| Data setup time | $t_{SU;DAT}$ | SCL0 SDA0 | | $t_{MCLK}$ – 20 | — | ns | At reception |
| SDA↓→SCL↑ (at wakeup function) | $t_{WAKE-UP}$ | SCL0 SDA0 | | Oscillation stabilization wait time + 2 $t_{MCLK}$ – 20 | — | ns | |

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

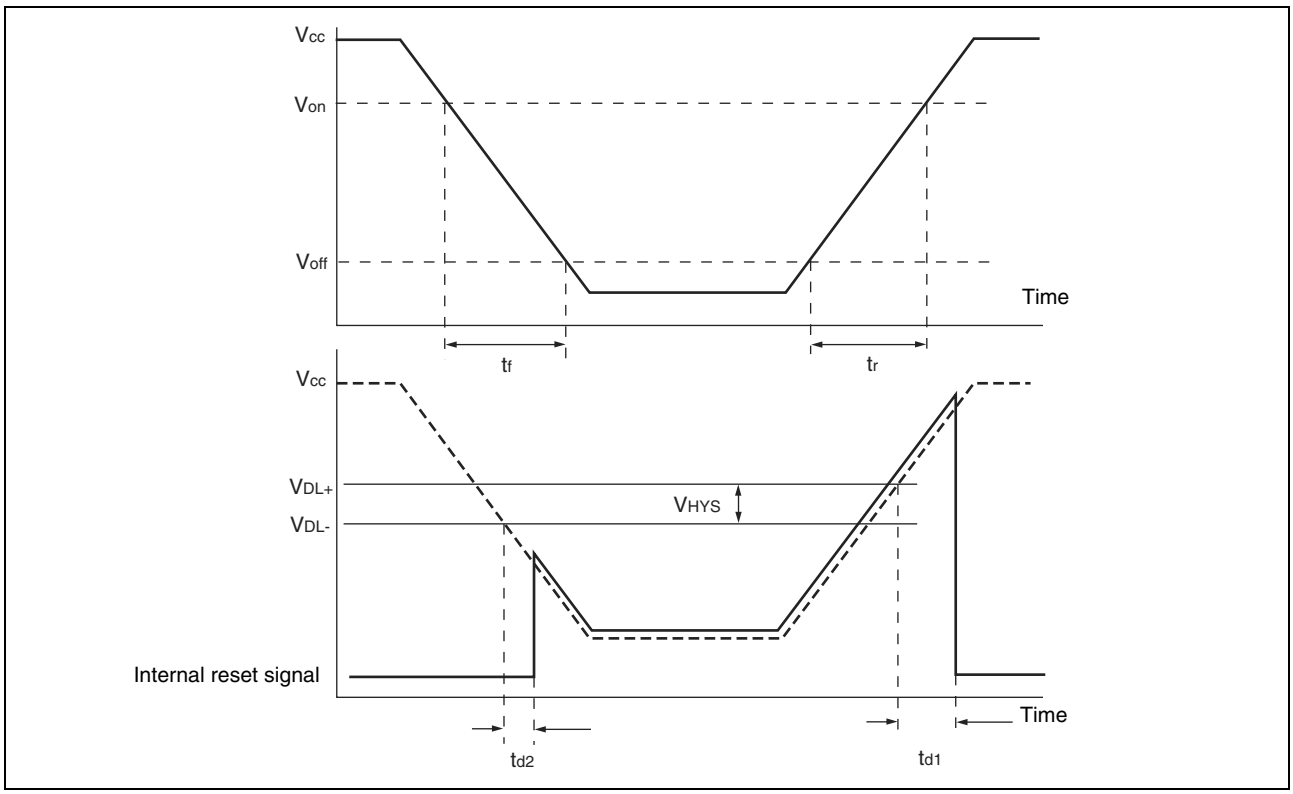
*2 : •Refer to " (2) Source Clock/Machine Clock" for $t_{MCLK}$.

- m is CS4 bit and CS3 bit (bit 4 and bit 3) of I²C clock control register (ICCR) .
- n is CS2 bit to CS0 bit (bit 2 to bit 0) of I²C clock control register (ICCR) .
- Actual timing of I²C is determined by m and n values set by the machine clock ($t_{MCLK}$) and CS4 to CS0 of ICCR0 register.
- Standard-mode :
  m and n can be set at the range : 0.9 MHz < $t_{MCLK}$ (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 0.9 MHz < $t_{MCLK}$ ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) : 0.9 MHz < $t_{MCLK}$ ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) : 0.9 MHz < $t_{MCLK}$ ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < $t_{MCLK}$ ≤ 10 MHz
- Fast-mode :
  m and n can be set at the range : 3.3 MHz < $t_{MCLK}$ (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 3.3 MHz < $t_{MCLK}$ ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < $t_{MCLK}$ ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < $t_{MCLK}$ ≤ 10 MHz

### (9) Low Voltage Detection

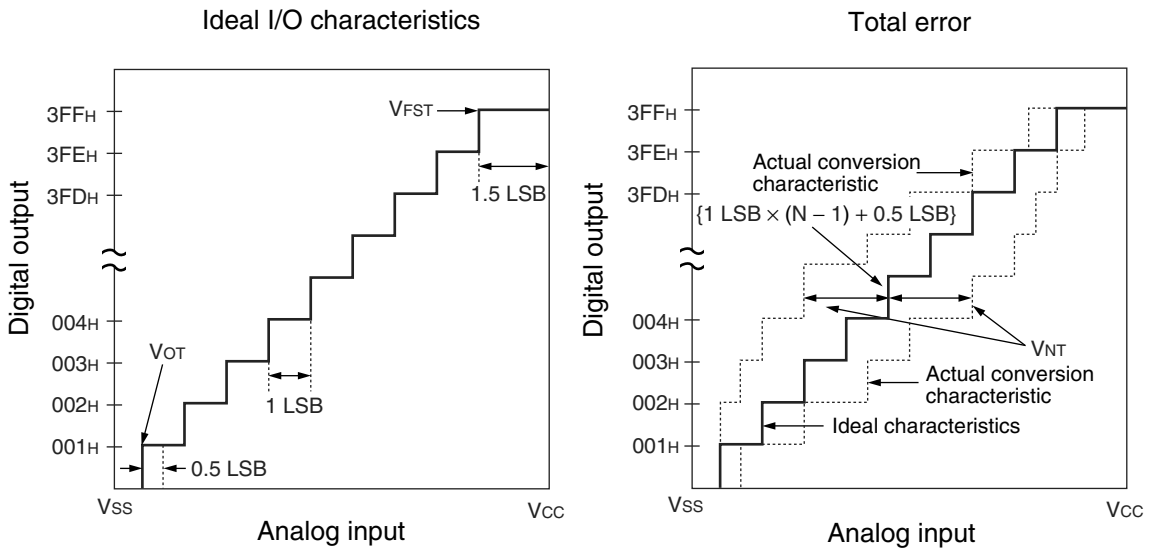
(Vss = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Release voltage | $V_{DL+}$ | — | 2.52 | 2.70 | 2.88 | V | At power-supply rise |
| Detection voltage | $V_{DL-}$ | | 2.42 | 2.60 | 2.78 | V | At power-supply fall |
| Hysteresis width | $V_{HYS}$ | | 70 | 100 | — | mV | |
| Power-supply start voltage | $V_{off}$ | | — | — | 2.3 | V | |
| Power-supply end voltage | $V_{on}$ | | 4.9 | — | — | V | |
| Power-supply voltage change time (at power supply rise) | $t_r$ | | 0.3 | — | — | µs | Slope of power supply that reset release signal generates |
| | | | — | 3000 | — | µs | Slope of power supply that reset release signal generates within rating ($V_{DL+}$) |
| Power-supply voltage change time (at power supply fall) | $t_f$ | | 300 | — | — | µs | Slope of power supply that reset detection signal generates |
| | | | — | 300 | — | µs | Slope of power supply that reset detection signal generates within rating ($V_{DL-}$) |
| Reset release delay time | $t_{d1}$ | | — | — | 400 | µs | |
| Reset detection delay time | $t_{d2}$ | | — | — | 30 | µs | |
| Current consumption | $I_{LVD}$ | | — | 38 | 50 | µA | Current consumption of low voltage detection circuit only |



**(3) Definition of A/D Converter Terms**

- Resolution
  The level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation between the value along a straight line connecting the zero transition point ("00 0000 0000" ← → "00 0000 0001") of a device and the full-scale transition point ("11 1111 1111" ← → "11 1111 1110") compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
  Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.



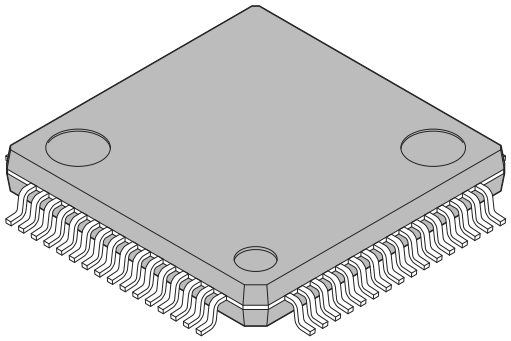

$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ \text{(V)}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

N : A/D converter digital output value
$V_{NT}$ : A voltage at which digital output transits from $(N - 1)_H$ to $N_H$

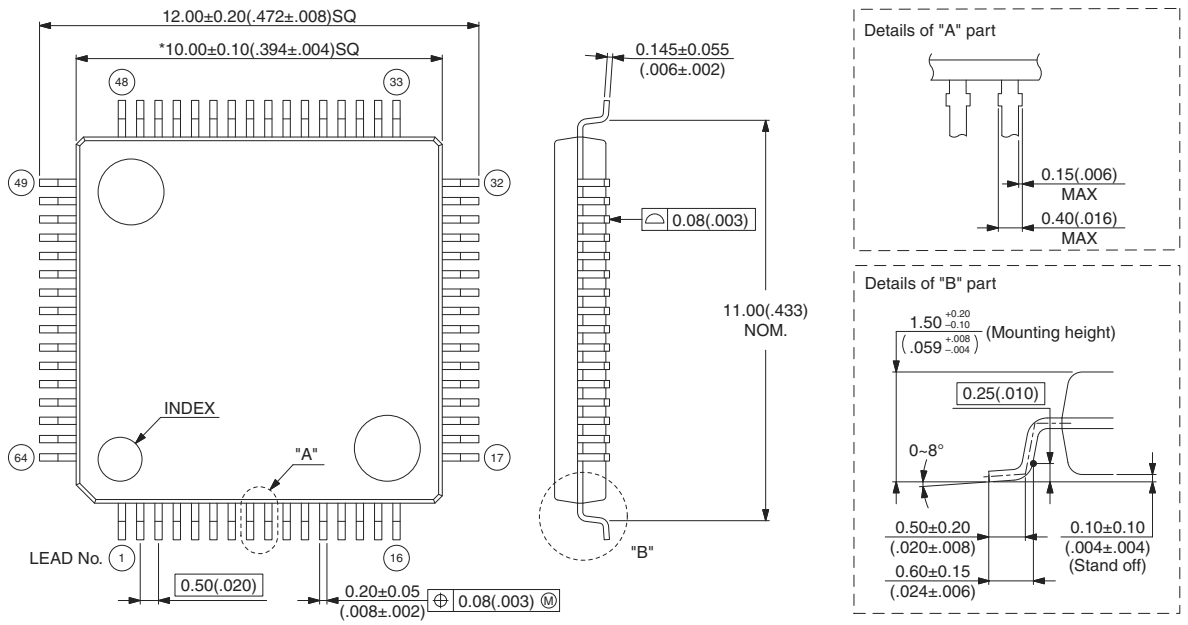
*(Continued)*

*(Continued)*

| 64-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 10.0 mm × 10.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Code (Reference) | P-LFQFP64-10×10-0.50 |
| | | |
| (FPT-64P-M24) | | |

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

# MEMO

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