**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-8FX |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, LINbus, SIO, UART/USART |
| Peripherals | LCD, LVD, POR, PWM, WDT |
| Number of I/O | 52 |
| Program Memory Size | 60KB (60K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/fujitsu/mb95f168japmc1-ge1 |

FUJITSU SEMICONDUCTOR
DATA SHEET

DS07–12624–4E

*8-bit Microcontrollers*

**CMOS**

# F²MC-8FX MB95160MA Series

## MB95168MA/F168MA/F168NA/F168JA/ MB95FV100D-103

### ■ DESCRIPTION

The MB95160MA series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

### ■ FEATURE

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock
  - Sub PLL clock

*(Continued)*

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/


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- Timer
  - 8/16-bit compound timer × 2 channels
    Can be used to interval timer, PWC timer, PWM timer and input capture.
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG × 1 channel
  - Time-base timer × 1 channel
  - Watch prescaler × 1 channel
- LIN-UART × 1 channel
  - LIN function, clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- UART/SIO × 1 channel
  - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- $I^2C$ × 1 channel
  Built-in wake-up function
- External interrupt × 8 channels
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter × 8 channels
  8-bit or 10-bit resolution can be selected.
- LCD controller (LCDC)
  - 32 SEG × 4 COM (Max 128 pixels)
  - With blinking function
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode
  - Time-base timer mode
- I/O port
  - The number of maximum ports : Max 52
  - Port configuration
    - General-purpose I/O ports (N-ch open drain) : 2 ports
    - General-purpose I/O ports (CMOS) : 50 ports
- Programmable input voltage levels of port
  Automotive input level / CMOS input level / hysteresis input level
- Flash memory security function (Flash memory product only)
  Protects the content of Flash memory

## ■ PRODUCT LINEUP

| Parameter \ Part number | | MB95168MA | MB95F168MA | MB95F168NA | MB95F168JA |
|---|---|---|---|---|---|
| Type | | Mask ROM product | Flash memory product | | |
| ROM capacity | | 60 Kbytes | | | |
| RAM capacity | | 2 Kbytes | | | |
| Reset output | | Yes/No selectable | Yes | | No |
| Option* | Clock system | Dual clock | | | |
| | Low voltage detection reset | Yes/No selectable | No | Yes | |
| | Clock supervisor | Yes/No selectable | No | | Yes |
| CPU functions | | Number of basic instructions : 136<br>Instruction bit length : 8 bits<br>Instruction length : 1 to 3 bytes<br>Data bit length : 1, 8, and 16 bits<br>Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz)<br>Interrupt processing time : 0.6 μs (at machine clock frequency 16.25 MHz) | | | |
| Peripheral functions | Ports (Max 52 ports) | General-purpose I/O port (N-ch open drain) : 2 ports<br>General-purpose I/O port (CMOS) : 50 ports<br>Programmable input voltage levels of port :<br>Automotive input level / CMOS input level / hysteresis input level | | | |
| | Time-base timer (1 channel) | Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz) | | | |
| | Watchdog timer | Reset generated cycle<br>At main oscillation clock 10 MHz : Min 105 ms<br>At sub oscillation clock 32.768 kHz (for dual clock product) : Min 250 ms | | | |
| | Wild register | Capable of replacing 3 bytes of ROM data | | | |
| | $I^2C$ (1 channel) | Master/slave sending and receiving<br>Bus error function and arbitration function<br>Detecting transmitting direction function<br>Start condition repeated generation and detection functions<br>Built-in wake-up function | | | |
| | UART/SIO (1 channel) | Data transfer capable in UART/SIO<br>Full duplex double buffer,<br>variable data length (5/6/7/8-bit), built-in baud rate generator<br>NRZ type transfer format, error detected function<br>LSB-first or MSB-first can be selected.<br>Clock synchronous (SIO) or clock asynchronous (UART) serial data transfer capable | | | |
| | LIN-UART (1 channel) | Dedicated reload timer allowing a wide range of communication speeds to be set.<br>Full duplex double buffer.<br>Capable of serial data transfer synchronous or asynchronous to clock signal.<br>LIN functions available as the LIN master or LIN slave. | | | |
| | 8/10-bit A/D converter (8 channels) | 8-bit or 10-bit resolution can be selected. | | | |

*(Continued)*

## ■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value. The maximum value is shown as follows.

| Oscillation stabilization wait time | Remarks |
|---|---|
| $(2^{14}-2)/F_{CH}$ | Approx. 4.10 ms (at main oscillation clock 4 MHz) |

## ■ PACKAGES AND CORRESPONDING PRODUCTS

| Package \ Part number | MB95168MA | MB95F168MA/ F168NA/F168JA | MB95FV100D-103 |
|---|---|---|---|
| FPT-64P-M23 | ○ | ○ | × |
| FPT-64P-M24 | ○ | ○ | × |
| BGA-224P-M08 | × | × | ○ |

○ : Available
× : Unavailable

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| Pin no. | Pin name | I/O circuit type*1 | Function |
|---|---|---|---|
| 55 | P67/SEG23/ SIN | N | General-purpose I/O port. The pin is shared with LCDC SEG output (SEG23) and LIN-UART data input (SIN) . |
| 56 | P07/INT07/ AN07/SEG24 | F | General-purpose I/O ports. The pins are shared with external interrupt input (INT00 to INT07), A/D analog input (AN00 to AN07) and LCDC SEG output (SEG31 to SEG24) . |
| 57 | P06/INT06/ AN06/SEG25 | | |
| 58 | P05/INT05/ AN05/SEG26 | | |
| 59 | P04/INT04/ AN04/SEG27 | | |
| 60 | P03/INT03/ AN03/SEG28 | | |
| 61 | P02/INT02/ AN02/SEG29 | | |
| 62 | P01/INT01/ AN01/SEG30 | | |
| 63 | P00/INT00/ AN00/SEG31 | | |
| 64 | $AV_{SS}$ | — | Power supply pin (GND) of A/D converter |

*1 : Refer to "■ I/O CIRCUIT TYPE" for details on the I/O circuit types.

*2 : When using P07 for segment output (SEG24) of LCDC, P95 can not be used as an output port. It can be used only as an input port.

• Mode Pin (MOD)

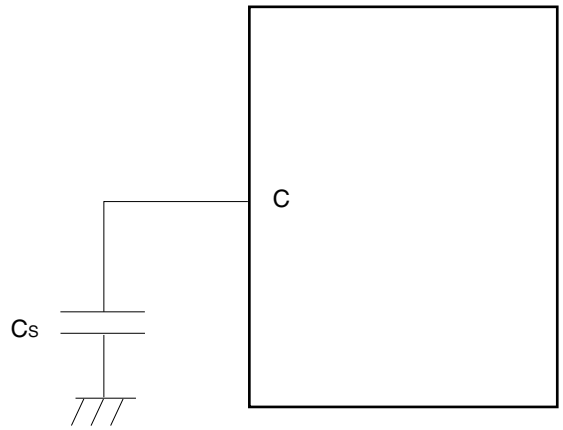
Connect the MOD pin directly to $V_{CC}$ or $V_{SS}$.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pin to $V_{CC}$ or $V_{SS}$ and to provide a low-impedance connection.

• C Pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of $V_{CC}$ pin must have a capacitance value higher than $C_S$. For connection of smoothing capacitor $C_S$, refer to the diagram below.

• C pin connection diagram




• Analog Power Supply

Always set the same potential to $AV_{CC}$ and $V_{CC}$ pins. When $V_{CC} > AV_{CC}$, the current may flow through the AN00 to AN07 pins.

• Treatment of Power Supply Pins on A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter is not in use.

Noise riding on the $AV_{CC}$ pin may cause accuracy degradation. So, connect approx. 0.1 μF ceramic capacitor as a bypass capacitor between $AV_{CC}$ and $AV_{SS}$ pins in the vicinity of this device.

## ■ I/O MAP

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0000H | PDR0 | Port 0 data register | R/W | 00000000B |
| 0001H | DDR0 | Port 0 direction register | R/W | 00000000B |
| 0002H | PDR1 | Port 1 data register | R/W | 00000000B |
| 0003H | DDR1 | Port 1 direction register | R/W | 00000000B |
| 0004H | — | (Disabled) | — | — |
| 0005H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111B |
| 0006H | PLLC | PLL control register | R/W | 00000000B |
| 0007H | SYCC | System clock control register | R/W | 1010X011B |
| 0008H | STBC | Standby control register | R/W | 00000000B |
| 0009H | RSRR | Reset factor register | R/W | XXXXXXXXB |
| 000AH | TBTC | Time-base timer control register | R/W | 00000000B |
| 000BH | WPCR | Watch prescaler control register | R/W | 00000000B |
| 000CH | WDTC | Watchdog timer control register | R/W | 00000000B |
| 000DH | — | (Disabled) | — | — |
| 000EH | PDR2 | Port 2 data register | R/W | 00000000B |
| 000FH | DDR2 | Port 2 direction register | R/W | 00000000B |
| 0010H to 0015H | — | (Disabled) | — | — |
| 0016H | PDR6 | Port 6 data register | R/W | 00000000B |
| 0017H | DDR6 | Port 6 direction register | R/W | 00000000B |
| 0018H to 001BH | — | (Disabled) | — | — |
| 001CH | PDR9 | Port 9 data register | R/W | 00000000B |
| 001DH | DDR9 | Port 9 direction register | R/W | 00000000B |
| 001EH | PDRA | Port A data register | R/W | 00000000B |
| 001FH | DDRA | Port A direction register | R/W | 00000000B |
| 0020H | PDRB | Port B data register | R/W | 00000000B |
| 0021H | DDRB | Port B direction register | R/W | 00000000B |
| 0022H | PDRC | Port C data register | R/W | 00000000B |
| 0023H | DDRC | Port C direction register | R/W | 00000000B |
| 0024H to 002CH | — | (Disabled) | — | — |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0059H | TDR0 | UART/SIO serial output data register ch.0 | R/W | 00000000B |
| 005AH | RDR0 | UART/SIO serial input data register ch.0 | R | 00000000B |
| 005BH to 005FH | — | (Disabled) | — | — |
| 0060H | IBCR00 | I²C bus control register 0 ch.0 | R/W | 00000000B |
| 0061H | IBCR10 | I²C bus control register 1 ch.0 | R/W | 00000000B |
| 0062H | IBSR0 | I²C bus status register ch.0 | R | 00000000B |
| 0063H | IDDR0 | I²C data register ch.0 | R/W | 00000000B |
| 0064H | IAAR0 | I²C address register ch.0 | R/W | 00000000B |
| 0065H | ICCR0 | I²C clock control register ch.0 | R/W | 00000000B |
| 0066H to 006BH | — | (Disabled) | — | — |
| 006CH | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000B |
| 006DH | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000B |
| 006EH | ADDH | 8/10-bit A/D converter data register (upper byte) | R/W | 00000000B |
| 006FH | ADDL | 8/10-bit A/D converter data register (lower byte) | R/W | 00000000B |
| 0070H | WCSR | Watch counter status register | R/W | 00000000B |
| 0071H | — | (Disabled) | — | — |
| 0072H | FSR | Flash memory status register | R/W | 000X0000B |
| 0073H | SWRE0 | Flash memory sector writing control register 0 | R/W | 00000000B |
| 0074H | SWRE1 | Flash memory sector writing control register 1 | R/W | 00000000B |
| 0075H | — | (Disabled) | — | — |
| 0076H | WREN | Wild register address compare enable register | R/W | 00000000B |
| 0077H | WROR | Wild register data test setting register | R/W | 00000000B |
| 0078H | — | Register bank pointer (RP) , Mirror of direct bank pointer (DP) | — | — |
| 0079H | ILR0 | Interrupt level setting register 0 | R/W | 11111111B |
| 007AH | ILR1 | Interrupt level setting register 1 | R/W | 11111111B |
| 007BH | ILR2 | Interrupt level setting register 2 | R/W | 11111111B |
| 007CH | ILR3 | Interrupt level setting register 3 | R/W | 11111111B |
| 007DH | ILR4 | Interrupt level setting register 4 | R/W | 11111111B |
| 007EH | ILR5 | Interrupt level setting register 5 | R/W | 11111111B |
| 007FH | — | (Disabled) | — | — |
| 0F80H | WRARH0 | Wild register address setting register (upper byte) ch.0 | R/W | 00000000B |

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*1 : The parameter is based on $V_{SS}$ = 0.0 V.

*2 : Apply equal potential to $AV_{CC}$ and $V_{CC}$. AVR should not exceed $AV_{CC}$ + 0.3 V.

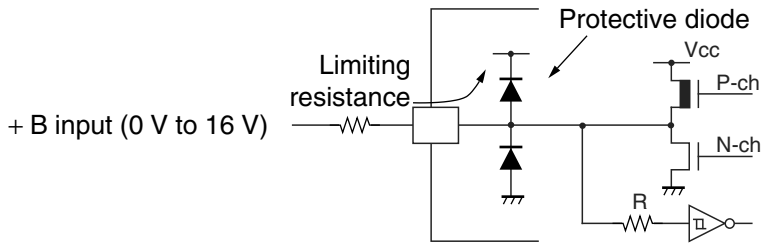
*3 : V0 to V3 should not exceed $V_{CC}$ + 0.3 V.

*4 : $V_I$ and Vo should not exceed $V_{CC}$ + 0.3 V. $V_I$ must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating.

*5 : Applicable to pins :
P00 to P07, P10 to P14, P20 to P22,P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7

- Use within recommended operating conditions.
- Use at DC voltage (current).
- + B signal is an input signal that exceeds $V_{CC}$ voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this affects other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

- Input/Output Equivalent circuits




WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

(Vss = 0.0 V)

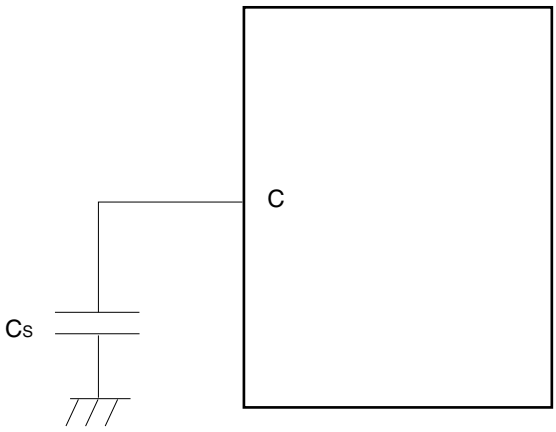
| Parameter | Symbol | Condi-tions | Value | | Unit | Remarks | |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | — | 2.42*1,*2 | 5.5*1 | V | In normal operating | Other than MB95FV100D-103 |
| | | | 2.3 | 5.5 | | Hold condition in STOP mode | |
| | | | 2.7 | 5.5 | | In normal operating | MB95FV100D-103 |
| | | | 2.3 | 5.5 | | Hold condition in STOP mode | |
| Power supply voltage for LCD | V0 to V3 | | $V_{SS}$ | $V_{CC}$ | V | The range of liquid crystal power supply (The optimal value depends on liquid crystal display elements used.) | |
| A/D converter reference input voltage | AVR | | 4.0 | $AV_{CC}$ | V | | |
| Smoothing capacitor | $C_S$ | | 0.1 | 1.0 | µF | *3 | |
| Operating temperature | $T_A$ | | − 40 | + 85 | °C | Other than MB95FV100D-103 | |
| | | | + 5 | +35 | °C | MB95FV100D-103 | |

*1 : The values vary with the operating frequency, machine clock or analog guarantee range.

*2 : When the low voltage detection reset is used, reset occurs while the low voltage is detected. For details on Low voltage detection, see "(9) Low Voltage Detection" in "4. AC Characteristics ".

*3 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of $V_{CC}$ pin must have a capacitor value higher than $C_S$. For connection of smoothing capacitor $C_S$, refer to the diagram below.

• C pin connection diagram




WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

### 3. DC Characteristics

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IH1}$ | P10, P67 | *1 | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | When selecting CMOS input level |
| | $V_{IH2}$ | P23, P24 | *1 | 0.7 $V_{CC}$ | — | $V_{SS}$ + 5.5 | V | |
| | $V_{IHA}$ | P00 to P07, P10 to P14, P20 to P22, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Port inputs if Automotive input levels are selected |
| | $V_{IHS1}$ | P00 to P07, P10 to P14, P20 to P22, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | *1 | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Hysteresis input |
| | $V_{IHS2}$ | P23, P24 | *1 | 0.8 $V_{CC}$ | — | $V_{SS}$ + 5.5 | V | |
| | $V_{IHM}$ | $\overline{RST}$, MOD | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{IL}$ | P10,P23, P24,P67 | *1 | $V_{SS}$ − 0.3 | — | 0.3 $V_{CC}$ | V | Hysteresis input (When selecting CMOS input level) |
| | $V_{ILA}$ | P00 to P07, P10 to P14, P20 to P24, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | — | $V_{SS}$ − 0.3 | — | 0.5 $V_{CC}$ | V | Port inputs if Automotive input levels are selected |
| | $V_{ILS}$ | P00 to P07, P10 to P14, P20 to P24, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7 | *1 | $V_{SS}$ − 0.3 | — | 0.2 $V_{CC}$ | V | Hysteresis input |
| | $V_{ILM}$ | $\overline{RST}$, MOD | — | $V_{SS}$ − 0.3 | — | 0.3 $V_{CC}$ | V | Hysteresis input |
| "H" level output voltage | $V_{OH}$ | All output pins | $I_{OH}$ = − 4.0 mA | $V_{CC}$ − 0.5 | — | — | V | |
| "L" level output voltage | $V_{OL}$ | $\overline{RST}$*2, All output pins | $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | |

*(Continued)*

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input leakage current (Hi-Z output leakage current) | $I_{LI}$ | Ports other than P23, P24 | 0.0 V < $V_I$ < $V_{CC}$ | − 5 | — | + 5 | µA | When the pull-up prohibition setting |
| Open drain output leakage current | $I_{LIOD}$ | P23, P24 | 0.0 V < $V_I$ < $V_{SS}$ + 5.5 V | — | — | 5 | µA | |
| Pull-up resistor | $R_{PULL}$ | P10 to P14, P20 to P22 | $V_I$ = 0.0 V | 25 | 50 | 100 | kΩ | When the pull-up permission setting |
| Pull-down resistor | $R_{MOD}$ | MOD | $V_I$ = $V_{CC}$ | 50 | 100 | 200 | kΩ | Mask ROM product only |
| Input capacitance | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVR, $V_{CC}$, $V_{SS}$ | f = 1 MHz | — | 5 | 15 | pF | |
| Power supply current*3 | $I_{CC}$ | $V_{CC}$ (External clock operation) | $F_{CH}$ = 20 MHz<br>$F_{MP}$ = 10 MHz<br>Main clock mode (divided by 2) | — | 9.5 | 12.5 | mA | Flash memory product (At other than Flash memory writing and erasing) |
| | | | | — | 30.0 | 35.0 | mA | Flash memory product (At Flash memory writing and erasing) |
| | | | | — | 7.2 | 9.5 | mA | Mask ROM product |
| | | | $F_{CH}$ = 32 MHz<br>$F_{MP}$ = 16 MHz<br>Main clock mode (divided by 2) | — | 15.2 | 20.0 | mA | Flash memory product (At other than Flash memory writing and erasing) |
| | | | | — | 35.7 | 42.5 | mA | Flash memory product (At Flash memory writing and erasing) |
| | | | | — | 11.6 | 15.2 | mA | Mask ROM product |
| | $I_{CCS}$ | | $F_{CH}$ = 20 MHz<br>$F_{MP}$ = 10 MHz<br>Main Sleep mode (divided by 2) | — | 4.5 | 7.5 | mA | |
| | | | $F_{CH}$ = 32 MHz<br>$F_{MP}$ = 16 MHz<br>Main Sleep mode (divided by 2) | — | 7.2 | 12.0 | mA | |

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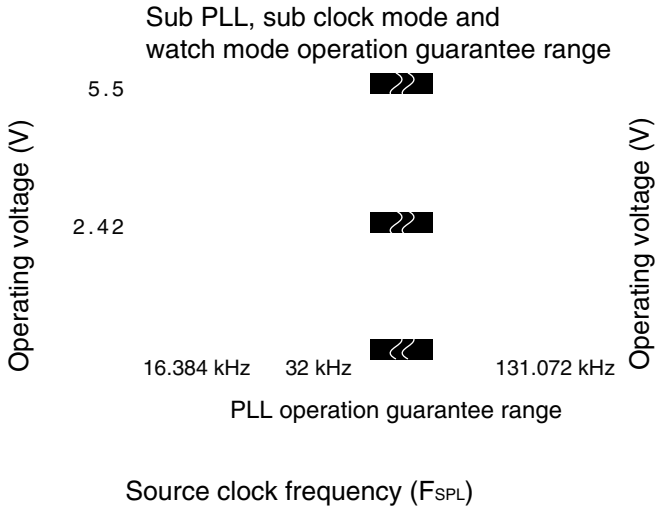
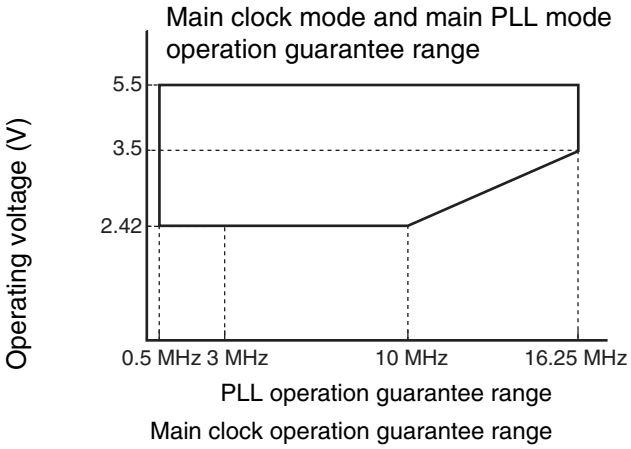
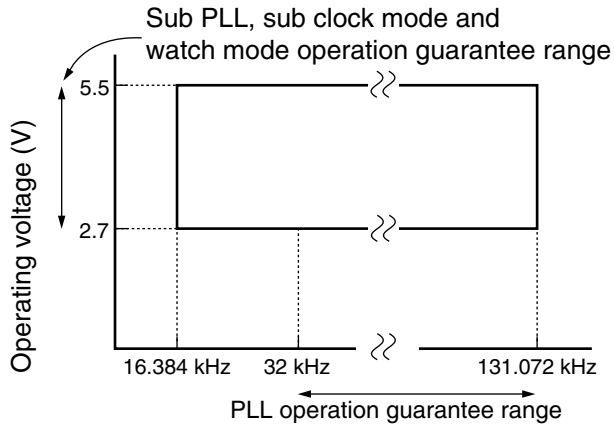
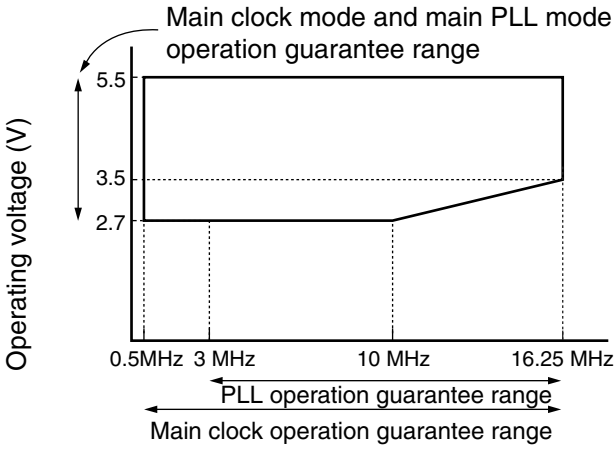
• Operating voltage - Operating frequency (When $T_A = -40$ °C to $+85$ °C)
  • MB95168MA/F168MA/F168NA/F168JA




• Operating voltage - Operating frequency (When $T_A = +5$ °C to $+35$ °C)
  • MB95FV100D-103



**(8) I²C Timing**

($V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Standard-mode | | Fast-mode | | |
| | | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | SCL0 | R = 1.7 kΩ, C = 50 pF*1 | 0 | 100 | 0 | 400 | kHz |
| (Repeat) Start condition hold time SDA ↓ → SCL ↓ | $t_{HD;STA}$ | SCL0 SDA0 | | 4.0 | — | 0.6 | — | µs |
| SCL clock "L" width | $t_{LOW}$ | SCL0 | | 4.7 | — | 1.3 | — | µs |
| SCL clock "H" width | $t_{HIGH}$ | SCL0 | | 4.0 | — | 0.6 | — | µs |
| (Repeat) Start condition setup time SCL ↑ → SDA ↓ | $t_{SU;STA}$ | SCL0 SDA0 | | 4.7 | — | 0.6 | — | µs |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HD;DAT}$ | SCL0 SDA0 | | 0 | 3.45*2 | 0 | 0.9*3 | µs |
| Data setup time SDA ↓ ↑ → SCL ↑ | $t_{SU;DAT}$ | SCL0 SDA0 | | 0.25*4 | — | 0.1*4 | — | µs |
| Stop condition setup time SCL ↑ → SDA ↑ | $t_{SU;STO}$ | SCL0 SDA0 | | 4.0 | — | 0.6 | — | µs |
| Bus free time between stop condition and start condition | $t_{BUF}$ | SCL0 SDA0 | | 4.7 | — | 1.3 | — | µs |

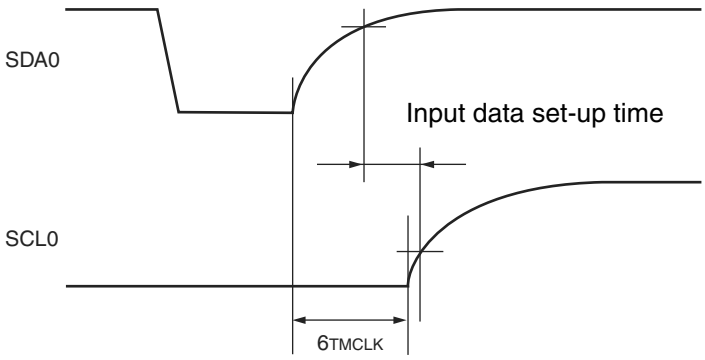
*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum $t_{HD;DAT}$ have only to be met if the device dose not stretch the "L" width ($t_{LOW}$) of the SCL signal.

*3 : A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must then be met.

*4 : Refer to " • Note of SDA and SCL set-up time".

• Note of SDA and SCL set-up time




The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

($V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value*2 | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCL clock "L" width | $t_{LOW}$ | SCL0 | R = 1.7 kΩ, C = 50 pF*1 | (2 + nm / 2) $t_{MCLK}$ – 20 | — | ns | Master mode |
| SCL clock "H" width | $t_{HIGH}$ | SCL0 | | (nm / 2) $t_{MCLK}$ – 20 | (nm / 2 ) $t_{MCLK}$ + 20 | ns | Master mode |
| Start condition hold time | $t_{HD;STA}$ | SCL0 SDA0 | | (–1 + nm / 2) $t_{MCLK}$ – 20 | (–1 + nm) $t_{MCLK}$ + 20 | ns | Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied. |
| Stop condition setup time | $t_{SU;STO}$ | SCL0 SDA0 | | (1 + nm / 2) $t_{MCLK}$ – 20 | (1 + nm / 2) $t_{MCLK}$ + 20 | ns | Master mode |
| Start condition setup time | $t_{SU;STA}$ | SCL0 SDA0 | | (1 + nm / 2) $t_{MCLK}$ – 20 | (1 + nm / 2) $t_{MCLK}$ + 20 | ns | Master mode |
| Bus free time between stop condition and start condition | $t_{BUF}$ | SCL0 SDA0 | | (2 nm + 4) $t_{MCLK}$ – 20 | — | ns | |
| Data hold time | $t_{HD;DAT}$ | SCL0 SDA0 | | 3 $t_{MCLK}$ – 20 | — | ns | Master mode |
| Data setup time | $t_{SU;DAT}$ | SCL0 SDA0 | | (–2 + nm / 2) $t_{MCLK}$ – 20 | (–1 + nm / 2) $t_{MCLK}$ + 20 | ns | Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied. |
| Setup time between clearing interrupt and SCL rising | $t_{SU;INT}$ | SCL0 | | (nm / 2) $t_{MCLK}$ – 20 | (1 + nm / 2) $t_{MCLK}$ + 20 | ns | Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓. |
| SCL clock "L" width | $t_{LOW}$ | SCL0 | | 4 $t_{MCLK}$ – 20 | — | ns | At reception |
| SCL clock "H" width | $t_{HIGH}$ | SCL0 | | 4 $t_{MCLK}$ – 20 | — | ns | At reception |
| Start condition detection | $t_{HD;STA}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | Undetected when 1 $t_{MCLK}$ is used at reception |

*(Continued)*

*(Continued)*

($V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to + 85 °C)

| Parameter | Symbol | Pin name | Conditions | Value*2 | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Stop condition detection | $t_{SU;STO}$ | SCL0 SDA0 | R = 1.7 kΩ, C = 50 pF*1 | 2 $t_{MCLK}$ – 20 | — | ns | Undetected when 1 $t_{MCLK}$ is used at reception |
| Restart condition detection condition | $t_{SU;STA}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | Undetected when 1 $t_{MCLK}$ is used at reception |
| Bus free time | $t_{BUF}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | At reception |
| Data hold time | $t_{HD;DAT}$ | SCL0 SDA0 | | 2 $t_{MCLK}$ – 20 | — | ns | At slave transmission mode |
| Data setup time | $t_{SU;DAT}$ | SCL0 SDA0 | | $t_{LOW}$ – 3 $t_{MCLK}$ – 20 | — | ns | At slave transmission mode |
| Data hold time | $t_{HD;DAT}$ | SCL0 SDA0 | | 0 | — | ns | At reception |
| Data setup time | $t_{SU;DAT}$ | SCL0 SDA0 | | $t_{MCLK}$ – 20 | — | ns | At reception |
| SDA↓→SCL↑ (at wakeup function) | $t_{WAKE-UP}$ | SCL0 SDA0 | | Oscillation stabilization wait time + 2 $t_{MCLK}$ – 20 | — | ns | |

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : •Refer to " (2) Source Clock/Machine Clock" for $t_{MCLK}$.

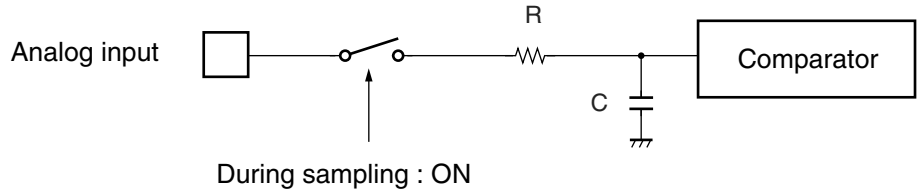
- m is CS4 bit and CS3 bit (bit 4 and bit 3) of I²C clock control register (ICCR) .
- n is CS2 bit to CS0 bit (bit 2 to bit 0) of I²C clock control register (ICCR) .
- Actual timing of I²C is determined by m and n values set by the machine clock ($t_{MCLK}$) and CS4 to CS0 of ICCR0 register.
- Standard-mode :
  m and n can be set at the range : 0.9 MHz < $t_{MCLK}$ (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 0.9 MHz < $t_{MCLK}$ ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) : 0.9 MHz < $t_{MCLK}$ ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) : 0.9 MHz < $t_{MCLK}$ ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < $t_{MCLK}$ ≤ 10 MHz
- Fast-mode :
  m and n can be set at the range : 3.3 MHz < $t_{MCLK}$ (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 3.3 MHz < $t_{MCLK}$ ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < $t_{MCLK}$ ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < $t_{MCLK}$ ≤ 10 MHz

### (2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

- Analog input equivalent circuit

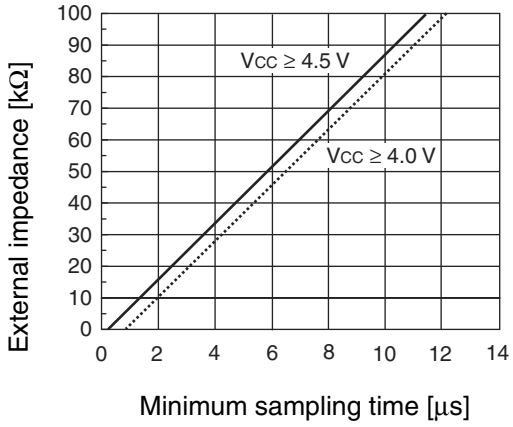



| | R | C |
|---|---|---|
| 4.5 V ≤ $V_{CC}$ ≤ 5.5 V | 2.0 kΩ (Max) | 16 pF (Max) |
| 4.0 V ≤ $V_{CC}$ < 4.5 V | 8.2 kΩ (Max) | 16 pF (Max) |

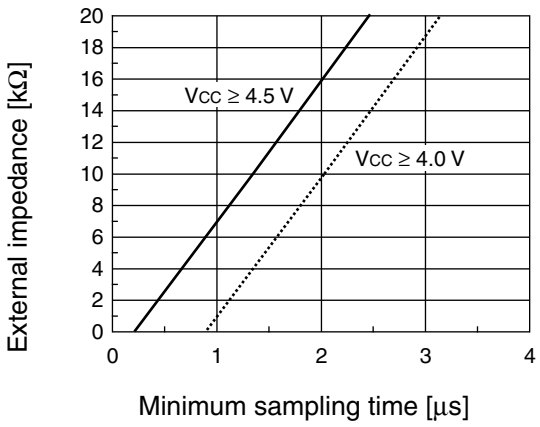
Note : The values are reference values.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)




(External impedance = 0 kΩ to 20 kΩ)



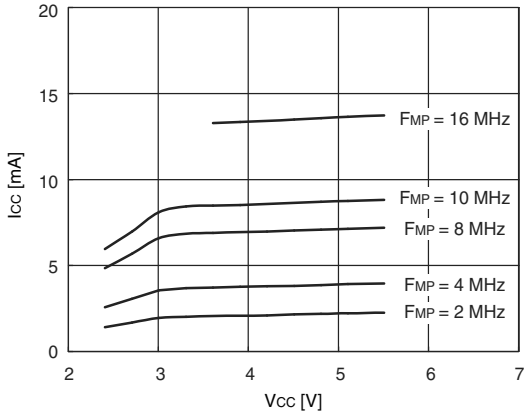

- **About errors**

As |$V_{CC}$ – $V_{SS}$| becomes smaller, values of relative errors grow larger.

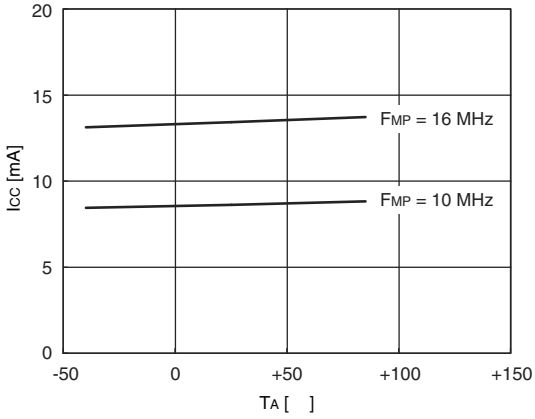
## ■ EXAMPLE CHARACTERISTICS

**• Power supply current temperature (MB95F168MA/F168NA/F168JA)**

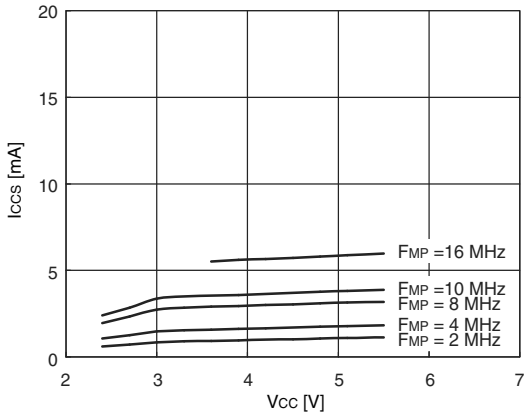
$I_{CC}$ – $V_{CC}$
$T_A$ = + 25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode, at external clock operating



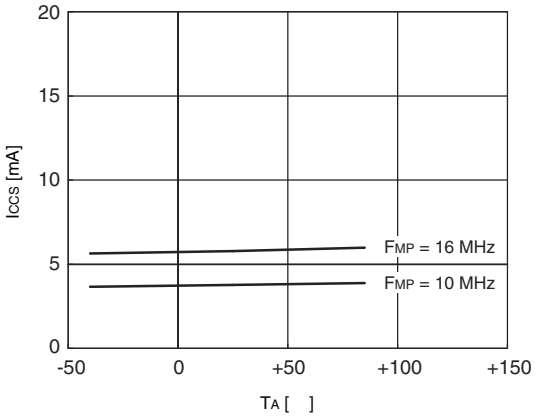

$I_{CC}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (divided by 2)
Main clock mode, at external clock operating



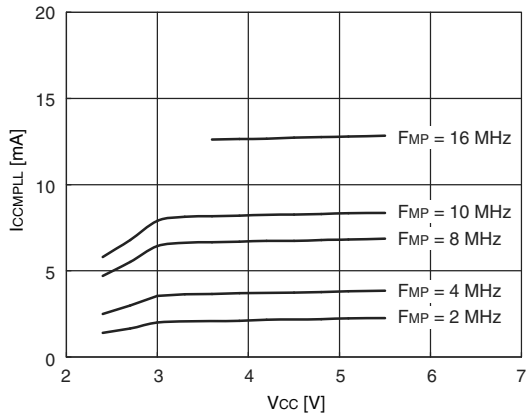

$I_{CCS}$ – $V_{CC}$
$T_A$ = + 25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode, at external clock operating



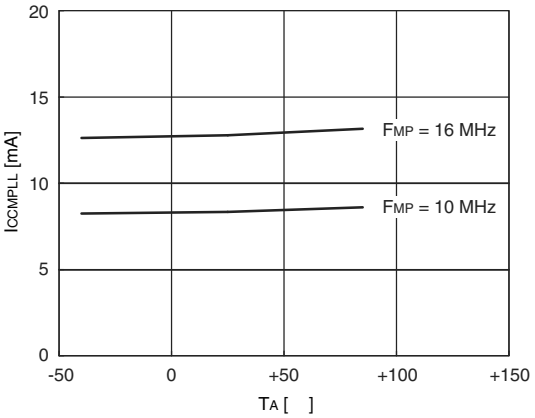

$I_{CCS}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (divided by 2)
Main sleep mode, at external clock operating




$I_{CCMPLL}$ – $V_{CC}$
$T_A$ = + 25 °C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz
(Main PLL multiplied by 2.5)
Main PLL mode, at external clock operating

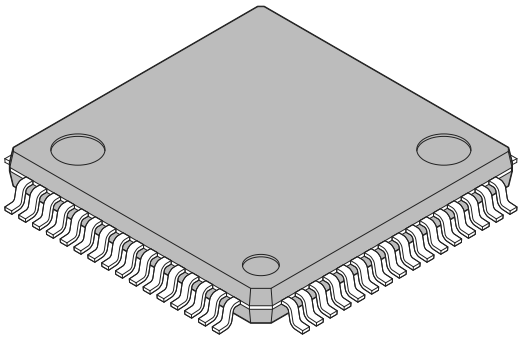



$I_{CCMPLL}$ – $T_A$
$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (Main PLL multiplied by 2.5)
Main PLL mode, at external clock operating



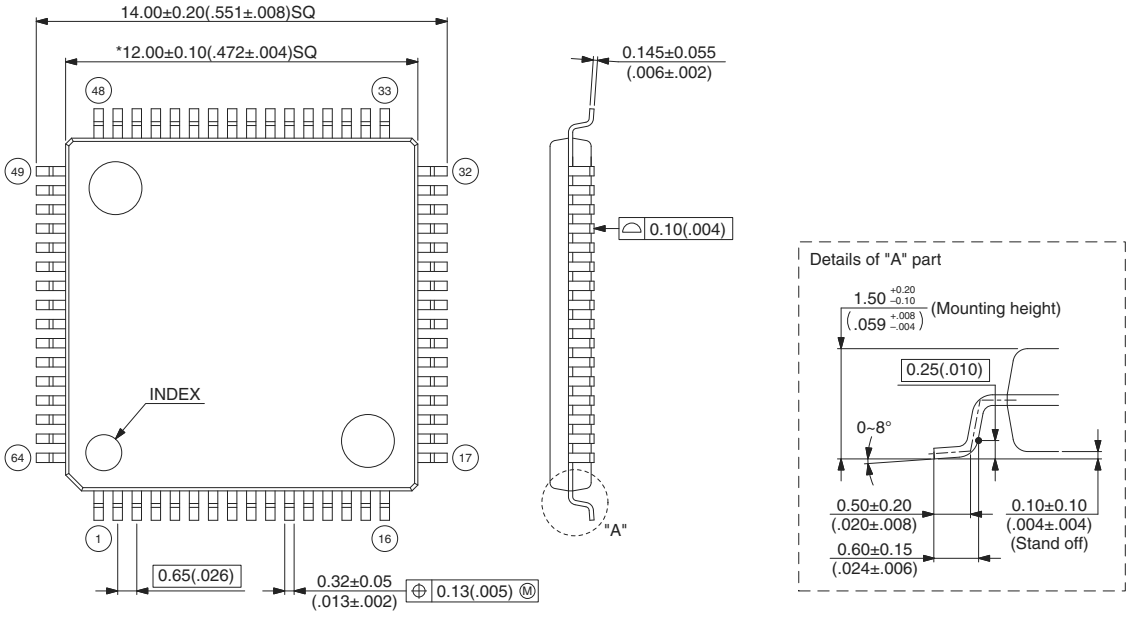

*(Continued)*

## ■ PACKAGE DIMENSIONS

| 64-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.65 mm |
| | Package width × package length | 12.0 × 12.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.47 g |
| (FPT-64P-M23) | Code (Reference) | P-LQFP64-12×12-0.65 |

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

## ■ MAJOR CHANGES IN THIS EDITION

| Page | Section | Change Results |
|---|---|---|
| 35 | ■ ELECTRICAL CHARACTERISTICS<br>3. DC Characteristics | Corrected note *1 below the table.<br>(The value is 2.88 V when the low voltage detection reset is used.<br>→ The input level of P10, P23, P24 and P67 can be switched to either the “CMOS input level” or “Hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR) .) |

The vertical lines marked in the left side of the page show the changes.