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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	83
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1810fbd144-551

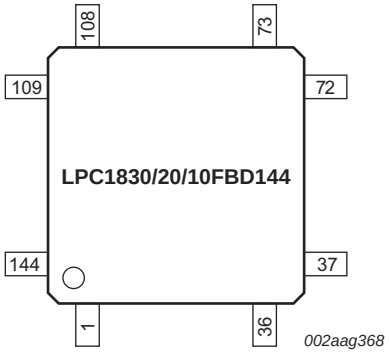


Fig 5. Pin configuration LQFP144 package

6.2 Pin description

On the LPC1850/30/20/10, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Not all functions listed in Table 3 are available on all packages. See Table 2 for availability of USB0, USB1, Ethernet, and LCD functions.

The parts contain two 10-bit ADCs (ADC0 and ADC1). The input channels of ADC0 and ADC1 on dedicated pins and multiplexed pins are combined in such a way that all channel 0 inputs (named ADC0_0 and ADC1_0) are tied together and connected to both, channel 0 on ADC0 and channel 0 on ADC1, channel 1 inputs (named ADC0_1 and ADC1_1) are tied together and connected to channel 1 on ADC0 and ADC1, and so forth. There are eight ADC channels total for the two ADCs.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_5	R5	N3	J4	48	[2]	N; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS0}}$ —** LOW active Chip Select 0 signal.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**SD_POW —** SD/MMC card power monitor output.
P1_6	T4	P3	K4	49	[2]	N; PU	I/O	**GPIO1[9] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_WE}}$ —** LOW active Write Enable signal.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CMD —** SD/MMC command signal.
P1_7	T5	N4	G4	50	[2]	N; PU	I/O	**GPIO1[0] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D0 —** External memory data line 0.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_20	M10	J10	K10	70	[2]	N; PU	I/O	**GPIO0[15] —** General purpose digital input/output pin.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
							I	**T0_CAP2 —** Capture input 2 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_0	T16	N14	G10	75	[2]	N; PU	-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0.
							I/O	**EMC_A13 —** External memory address line 13.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active high). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							I/O	**GPIO5[0] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input 0 of timer 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
P2_1	N15	M13	G7	81	[2]	N; PU	-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.
							I/O	**EMC_A12 —** External memory address line 12.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**GPIO5[1] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input 1 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P6_10	H15	G13	-	100	[2]	N; PU	I/O	**GPIO3[6] —** General purpose digital input/output pin.
							O	**$\overline{\text{MCABORT}}$ —** Motor control PWM, LOW-active fast abort.
							-	**R —** Function reserved.
							O	**EMC_DQMOUT1 —** Data mask 1 used with SDRAM and static devices.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_11	H12	F11	C9	101	[2]	N; PU	I/O	**GPIO3[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_CKEOUT0 —** SDRAM clock enable 0.
							-	**R —** Function reserved.
							O	**T2_MAT3 —** Match output 3 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_12	G15	F13	-	103	[2]	N; PU	I/O	**GPIO2[8] —** General purpose digital input/output pin.
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							-	**R —** Function reserved.
							O	**EMC_DQMOUT0 —** Data mask 0 used with SDRAM and static devices.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_0	B16	B14	-	110	[2]	N; PU	I/O	**GPIO3[8] —** General purpose digital input/output pin.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_LE —** Line end signal.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P7_1	C14	C13	-	113	[2]	N; PU	I/O	**GPIO3[9] —** General purpose digital input/output pin.
							O	**CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							O	**LCD_VD19 —** LCD data.
							O	**LCD_VD7 —** LCD data.
							-	**R —** Function reserved.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.
P7_2	A16	A14	-	115	[2]	N; PU	I/O	**GPIO3[10] —** General purpose digital input/output pin.
							I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
							I/O	**I2S0_TX_SDA —** I²S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**LCD_VD18 —** LCD data.
							O	**LCD_VD6 —** LCD data.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
P7_3	C13	C12	-	117	[2]	N; PU	I/O	**GPIO3[11] —** General purpose digital input/output pin.
							I	**CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1.
							-	**R —** Function reserved.
							O	**LCD_VD17 —** LCD data.
							O	**LCD_VD5 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P9_6	L11	M9	-	72	[2]	N; PU	I/O	**GPIO4[11] —** General purpose digital input/output pin.
							O	**MCOB1 —** Motor control PWM channel 1, output B.
							I	**USB1_PWR_FAULT —** USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.
PA_0	L12	L10	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S1_RX_MCLK —** I^2S1 receive master clock.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
PA_1	J14	H12	-	-	[3]	N; PU	I/O	**GPIO4[8] —** General purpose digital input/output pin.
							I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
							-	**R —** Function reserved.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_2	K15	J13	-	-	[3]	N; PU	I/O	**GPIO4[9] —** General purpose digital input/output pin.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PC_7	G5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
							-	**R —** Function reserved.
							I	**ENET_RXD3 —** Ethernet receive data 3 (MII interface).
							I/O	**GPIO6[6] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT0 —** Match output 0 of timer 3.
							I/O	**SD_DAT3 —** SD/MMC data bus line 3.
PC_8	N4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
							-	**R —** Function reserved.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).
							I/O	**GPIO6[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT1 —** Match output 1 of timer 3.
							I	**SD_CD —** SD/MMC card detect input.
PC_9	K2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY.
							-	**R —** Function reserved.
							I	**ENET_RX_ER —** Ethernet receive error (MII interface).
							I/O	**GPIO6[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output 2 of timer 3.
							O	**SD_POW —** SD/MMC power monitor output.
PC_10	M5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
							I	**U1_DSR —** Data Set Ready input for UART1.
							-	**R —** Function reserved.
							I/O	**GPIO6[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output 3 of timer 3.
							I/O	**SD_CMD —** SD/MMC command signal.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PF_6	E7	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							I/O	**GPIO7[20] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S1_TX_SDA —** I^2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							AI	**ADC1_3 —** ADC1 and ADC0, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_7	B7	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U3_BAUD —** Baud pin USART3.
							I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							I/O	**GPIO7[21] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							AI/O	**ADC1_7 —** ADC1 and ADC0, input channel 7 or band gap output. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_8	E6	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
							I	**CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0.
							O	**TRACEDATA[3] —** Trace data, bit 3.
							I/O	**GPIO7[22] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_2 —** ADC0 and ADC1, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
Debug pins								
DBGEN	L4	K4	A6	28	[2]	I; PU	I	JTAG interface control signal. Also used for boundary scan. To use the part in functional mode, connect this pin in one of the following ways: • Leave DBGEN open. The DBGEN pin is pulled up internally by a 50 kΩ resistor. • Tie DBGEN to VDDIO. • Pull DBGEN up to VDDIO with an external pull-up resistor.
TCK/SWDCLK	J5	G5	H2	27	[2]	I; F	I	Test Clock for JTAG interface (default) or Serial Wire (SW) clock.
$\overline{\text{TRST}}$	M4	L4	B4	29	[2]	I; PU	I	Test Reset for JTAG interface.
TMS/SWDIO	K6	K5	C4	30	[2]	I; PU	I	Test Mode Select for JTAG interface (default) or SW debug data input/output.
TDO/SWO	K5	J5	H3	31	[2]	O	O	Test Data Out for JTAG interface (default) or SW trace output.
TDI	J4	H4	G3	26	[2]	I; PU	I	Test Data In for JTAG interface.
USB0 pins								
USB0_DP	F2	E2	E1	18	[6]	-	I/O	USB0 bidirectional D+ line. Do not add an external series resistor.
USB0_DM	G2	F2	E2	20	[6]	-	I/O	USB0 bidirectional D− line. Do not add an external series resistor.
USB0_VBUS	F1	E1	E3	21	[6] [7]	-	I/O	VBUS pin (power on USB cable). This pin includes an internal pull-down resistor of 64 kΩ (typical) ± 16 kΩ.
USB0_ID	H2	G2	F1	22	[8]	-	I	Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH). For use with OTG, this pin has an internal pull-up resistor.
USB0_RREF	H1	G1	F3	24	[8]	-		12.0 kΩ (accuracy 1 %) on-board resistor to ground for current reference.
USB1 pins								
USB1_DP	F12	D11	E9	89	[9]	-	I/O	USB1 bidirectional D+ line. Add an external series resistor of 33 Ω +/- 2 %.
USB1_DM	G12	E11	E10	90	[9]	-	I/O	USB1 bidirectional D− line. Add an external series resistor of 33 Ω +/- 2 %.
I^2C-bus pins								
I2C0_SCL	L15	K13	D6	92	[10]	I; F	I/O	I^2C clock input/output. Open-drain output (for I^2C-bus compliance).
I2C0_SDA	L16	K14	E6	93	[10]	I; F	I/O	I^2C data input/output. Open-drain output (for I^2C-bus compliance).
Reset and wake-up pins								
$\overline{\text{RESET}}$	D9	C7	B6	128	[11]	I; IA	I	External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin does not have an internal pull-up.

- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.13.3 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M3 processor with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasing and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.13.3.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
- Supports DMA access.

7.13.4 SD/MMC card interface

The SD/MMC card interface supports the following modes:

- Secure Digital memory (SD version 3.0)
- Secure Digital I/O (SDIO version 2.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1)

- Smart card mode conforming to ISO7816 specification

7.14.3 SSP serial I/O controller

Remark: The LPC1850/30/20/10 contain two SSP controllers.

The SSP controller can operate on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full-duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.14.3.1 Features

- Maximum SSP speed in full-duplex mode of 25 Mbit/s; for transmit only 50 Mbit/s (master) and 15 Mbit/s (slave).
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- Eight-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.
- Connected to the GPDMA.

7.14.4 I^2C-bus interface

Remark: The LPC1850/30/20/10 contain two I^2C-bus interfaces.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.14.4.1 Features

- I^2C0 is a standard I^2C-compliant bus interface with open-drain pins. I^2C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I^2C1 uses standard I/O pins with bit rates of up to 400 kbit/s (Fast I^2C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)	on pin VDDREG		−0.5	3.6	V
$V_{DD(IO)}$	input/output supply voltage	on pin VDDIO		−0.5	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		−0.5	3.6	V
V_{BAT}	battery supply voltage	on pin VBAT		−0.5	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP		−0.5	3.6	V
V_I	input voltage	only valid when the $V_{DD(IO)} \geq 2.2$ V	[2]			
		5 V tolerant I/O pins		−0.5	5.5	V
		ADC/DAC pins and digital I/O pins configured for an analog function		−0.5	$V_{DDA(3V3)}$	V
		USB0 pins USB0_DP; USB0_DM;USB0_VBUS		−0.3	5.25	V
		USB0 pins USB0_ID; USB0_RREF		−0.3	3.6	V
		USB1 pins USB1_DP and USB1_DM		−0.3	5.25	V
I_{DD}	supply current	per supply pin	[3]	-	100	mA
I_{SS}	ground current	per ground pin	[3]	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[4]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	−2000	+2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

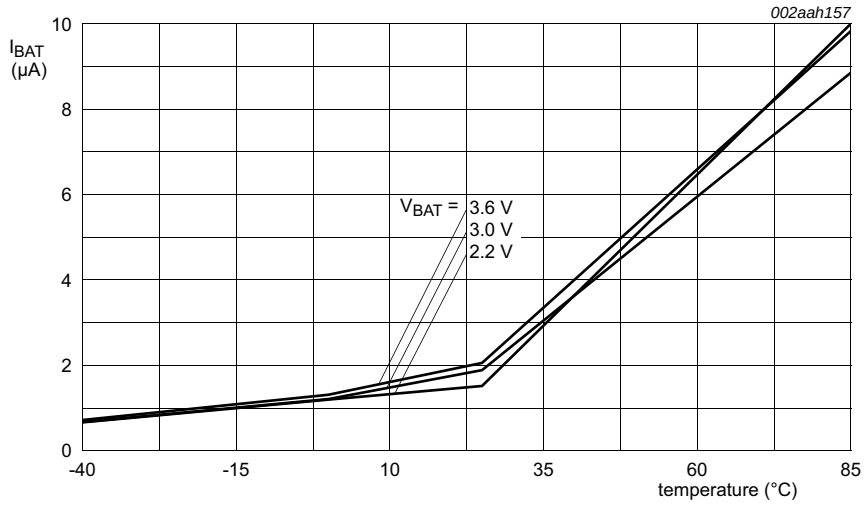
b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.



Conditions: $V_{DD(REG)(3V3)}$, $V_{DD(IO)}$ floating.

Fig 18. Typical battery supply versus temperature in Deep power-down mode

10.2 Peripheral power consumption

The typical power consumption at T = 25 °C for each individual peripheral is measured as follows:

1. Enable all branch clocks and measure the current $I_{DD(REG)(3V3)}$.
2. Disable the branch clock to the peripheral to be measured and keep all other branch clocks enabled.
3. Calculate the difference between measurement 1 and 2. The result is the peripheral power consumption.

Table 11. Peripheral power consumption

Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
I2C1	CLK_APB3_I2C1	0.01	0.02
I2C0	CLK_APB1_I2C0	0.02	0.01
DAC	CLK_APB3_DAC	0.01	0.02
ADC0	CLK_APB3_ADC0	0.05	0.05
ADC1	CLK_APB3_ADC1	0.04	0.04
CAN0	CLK_APB3_CAN0	0.17	0.17
CAN1	CLK_APB1_CAN1	0.17	0.17
MOTOCON	CLK_APB1_MOTOCON	0.05	0.05
I2S	CLK_APB1_I2S	0.11	0.11
SPIFI	CLK_SPIFI, CLK_M3_SPIFI	0.95	1.85
GPIO	CLK_M3_GPIO	0.66	1.31
LCD	CLK_M3_LCD	0.85	1.72

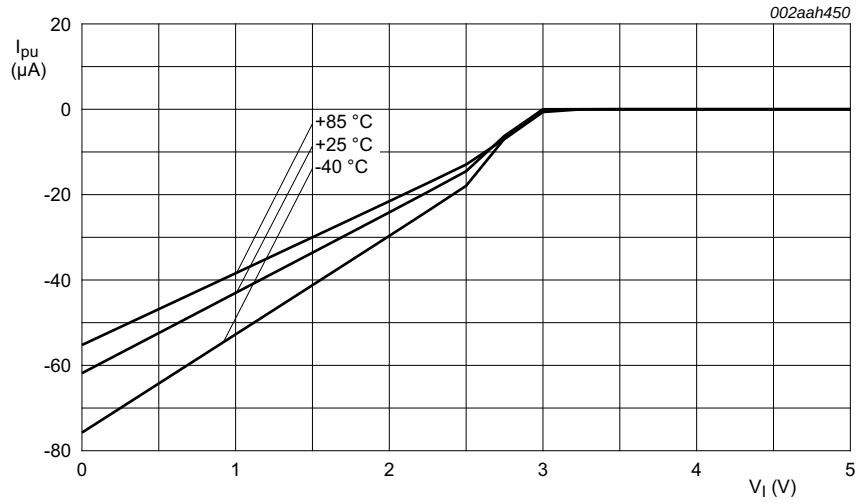
10.3 BOD characteristics

Table 12. BOD static characteristics[1]

T_{amb} = 25 °C; typical data.

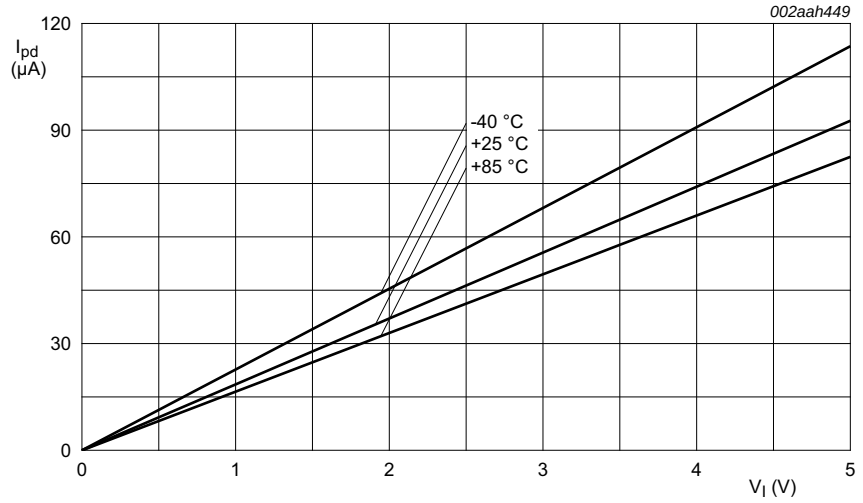
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0					
		assertion		-	2.75	-	V
		de-assertion		-	2.92	-	V
		interrupt level 1					
		assertion		-	2.85	-	V
		de-assertion		-	3.00	-	V
		interrupt level 2					
		assertion		-	2.95	-	V
		de-assertion		-	3.12	-	V
		interrupt level 3					
		assertion		-	3.05	-	V
		de-assertion		-	3.19	-	V
		reset level 0					
		assertion		-	1.70	-	V
		de-assertion		-	1.85	-	V
		reset level 1					
		assertion		-	1.80	-	V
		de-assertion		-	1.95	-	V
		reset level 2					
		assertion		-	1.90	-	V
		de-assertion		-	2.05	-	V
		reset level 3					
		assertion		-	2.00	-	V
		de-assertion		-	2.15	-	V

[1] Interrupt and reset levels are selected by writing to the BODLV1/2 bits in the control register CREGE0, see *the LPC18xx user manual*.



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated values.

Fig 23. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated values.

Fig 24. Typical pull-down current I_{pd} versus input voltage V_I

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

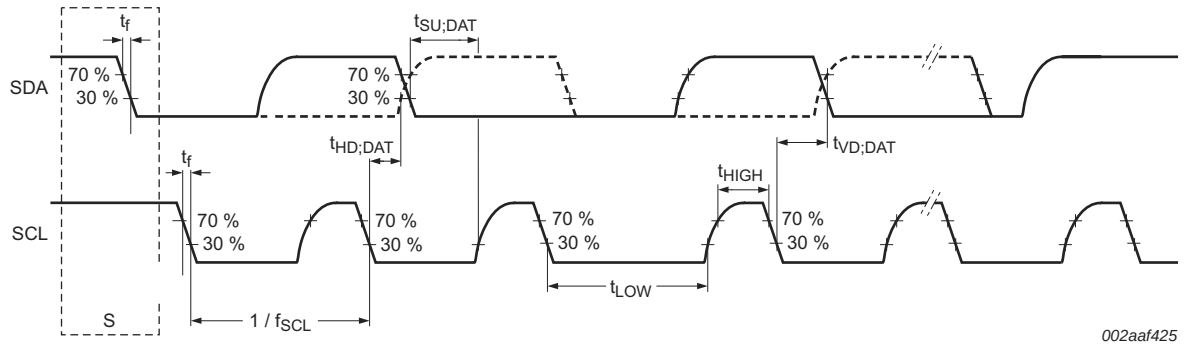


Fig 26. I^2C-bus pins clock timing

11.9 I^2S-bus interface

Table 21. Dynamic characteristics: I^2S-bus interface pins

T_{amb} = 25 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I^2S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I^2S-bus interface PCLK = BASE_APB1_CLK / 12. I^2S clock cycle time $T_{cy(clk)}$ = 79.2 ns; corresponds to the SCK signal in the *I^2S-bus specification*.

Table 23. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5T_{cy(clk)}$ + 0.2	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$ + 0.2	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		0.5 × $T_{cy(clk)}$ + 0.2	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$ + 0.2	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$ + 0.2	-	-	ns
		microwire frame format		0.5 × $T_{cy(clk)}$	-	-	ns
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.

Table 24. Dynamic characteristics: Static asynchronous external memory interface *…continued*

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted resulting in multiple memory accesses.

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 0	[2]	−0.9 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	PB = 0	[2] [5]	−1.9 + $T_{cy(clk)}$	-	−0.5 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 0	[2]	−2.5 + $T_{cy(clk)}$	-	1.4 + $T_{cy(clk)}$	ns
t_{CSHEOW}	$\overline{CS}$ HIGH to end of write time		[5]	−2.0	-	0	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1		−2.5	-	1.4	ns
t_{WEHANV}	WE HIGH to address invalid time	PB = 1		−0.9 + $T_{cy(clk)}$	-	2.4 + $T_{cy(clk)}$	ns

[1] Parameters specified for 40 % of $V_{DD(IO)}$ for rising edges and 60 % of $V_{DD(IO)}$ for falling edges.

[2] $T_{cy(clk)}$ = 1/CCLK (see LPC18xx User manual).

[3] End Of Read (EOR): longest of t_{CSHOEH}, t_{OEHANV}, $t_{CSHBLSH}$.

[4] Start Of Read (SOR): longest of t_{CSLAV}, t_{CSLOEL}, $t_{CSLBLSL}$.

[5] End Of Write (EOW): earliest of address not valid or $\overline{EMC\_BLSn}$ HIGH.

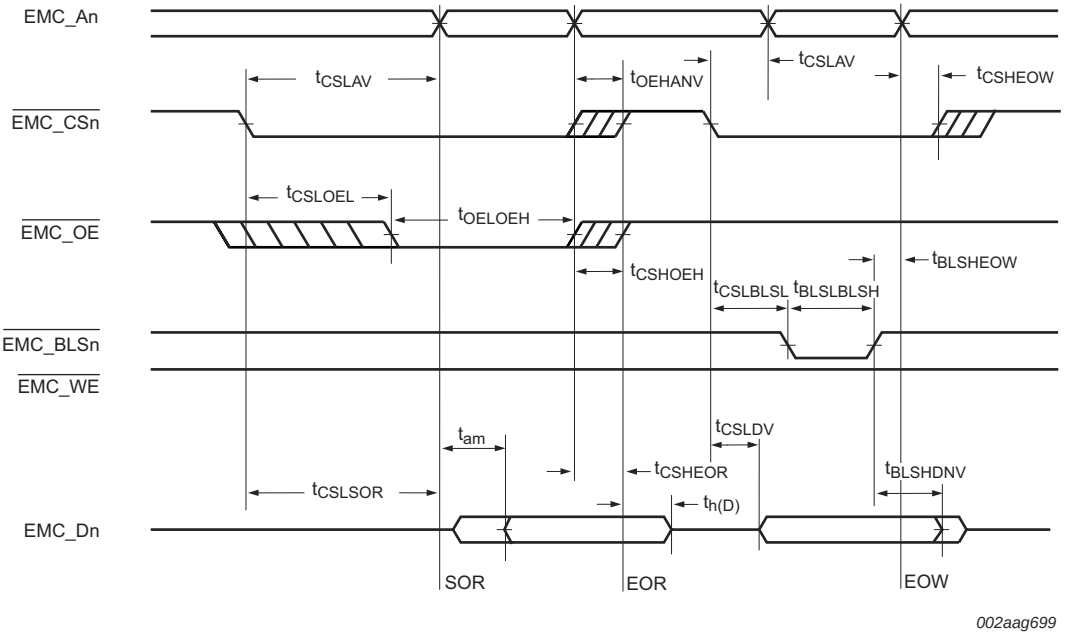


Fig 32. External static memory read/write access (PB = 0)

13. Application information

13.1 LCD panel signal usage

Table 35. LCD panel connections for STN single panel mode

External pin	4-bit mono STN single panel		8-bit mono STN single panel		Color STN single panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:8]	-	-	-	-	-	-
LCD_VD7	-	-	P8_4	UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	CDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 36. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:16]	-	-	-	-	-	-
LCD_VD15	-	-	PB_4	LD[7]	PB_4	LD[7]
LCD_VD14	-	-	PB_5	LD[6]	PB_5	LD[6]
LCD_VD13	-	-	PB_6	LD[5]	PB_6	LD[5]
LCD_VD12	-	-	P8_3	LD[4]	P8_3	LD[4]
LCD_VD11	P4_9	LD[3]	P4_9	LD[3]	P4_9	LD[3]
LCD_VD10	P4_10	LD[2]	P4_10	LD[2]	P4_10	LD[2]
LCD_VD9	P4_8	LD[1]	P4_8	LD[1]	P4_8	LD[1]
LCD_VD8	P7_5	LD[0]	P7_5	LD[0]	P7_5	LD[0]
LCD_VD7	-	-		UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]

Table 38. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	< 100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

Table 39. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{x2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

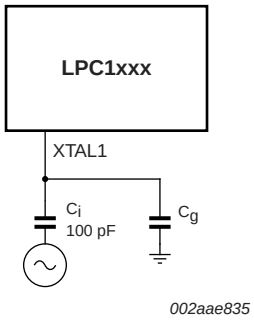


Fig 41. Slave mode operation of the on-chip oscillator

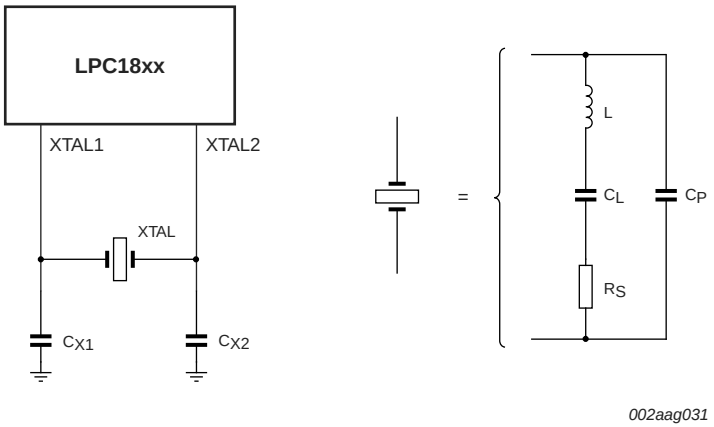


Fig 42. Oscillator modes with external crystal model used for C_{X1}/C_{X2} evaluation