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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	168K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1820fet100-551

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P2_8	J16	H14	C6	98	[2]	N; PU	-	**R —** Function reserved. Boot pin (see Table 5)
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							I/O	**EMC_A8 —** External memory address line 8.
							I/O	**GPIO5[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_9	H16	G14	B10	102	[2]	N; PU	I/O	**GPIO1[10] —** General purpose digital input/output pin. Boot pin (see Table 5).
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**EMC_A0 —** External memory address line 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_10	G16	F14	E8	104	[2]	N; PU	I/O	**GPIO0[14] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**EMC_A1 —** External memory address line 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_11	F16	E13	A9	105	[2]	N; PU	I/O	**GPIO1[11] —** General purpose digital input/output pin.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							I	**U2_RXD —** Receiver input for USART2.
							I/O	**EMC_A2 —** External memory address line 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.13.7 High-speed USB Host/Device interface with ULPI (USB1)

Remark: USB1 is available on parts LPC1850/30 (see Table 2).

The USB1 interface can operate as a full-speed USB host/device interface or can connect to an external ULPI PHY for High-speed operation.

7.13.7.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.13.8 LCD controller

Remark: The LCD controller is available on LPC1850 only.

The LCD controller provides all of the necessary control signals to interface directly to various color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 $\times$ 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512 byte color palette allows reducing bus utilization (that is, memory size of the displayed data) while still supporting many colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time required to operate the display.

7.13.8.1 Features

- AHB master interface to access frame buffer.

and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.15.3.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position-compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

7.15.4 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer compare function can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.15.4.1 Features

- 32-bit counter. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This mechanism allows for combinations not possible with a simple compare.

7.15.5 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.15.5.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

10. Static characteristics

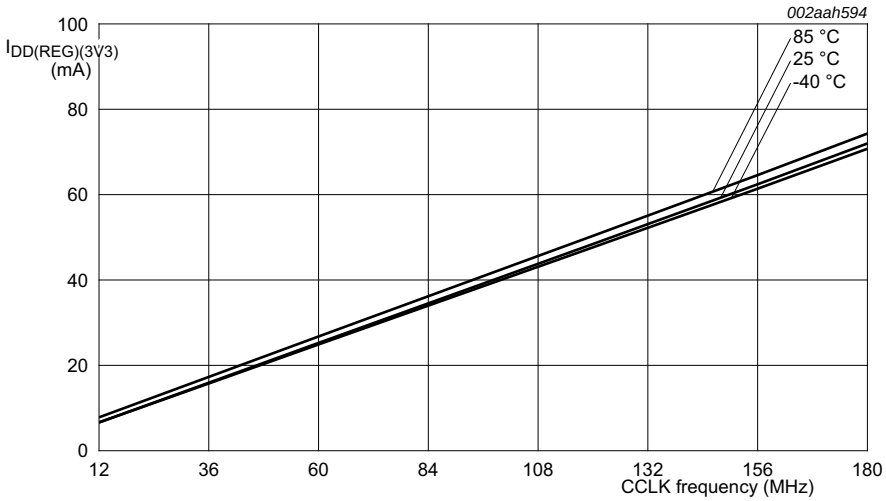
Table 10. Static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage			2.2	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.2	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.2	-	3.6	V
		on pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.2	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	6.6	-	mA
		CCLK = 60 MHz	[4]		25.3	-	mA
		CCLK = 120 MHz	[4]	-	48.4	-	mA
		CCLK = 180 MHz	[4]	-	72.0	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	after WFE/WFI instruction executed from RAM; all peripherals disabled					
		sleep mode	[4][5]	-	5.0	-	mA
		deep-sleep mode	[4]	-	30	-	µA
		power-down mode	[4]	-	15	-	µA
		deep power-down mode	[4][6]	-	0.03	-	µA
		deep power-down mode; VBAT floating	[4]	-	2	-	µA
I_{BAT}	battery supply current	active mode; V_{BAT} = 3.2 V; $V_{DD(REG)(3V3)}$ = 3.6 V.	[7]	-	0	-	nA
I_{BAT}	battery supply current	$V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} = 3.6 V	[9]			-	
		deep-sleep mode		-	2		µA
		power-down mode	[9]	-	2	-	µA
		deep power-down mode	[9]	-	2	-	µA

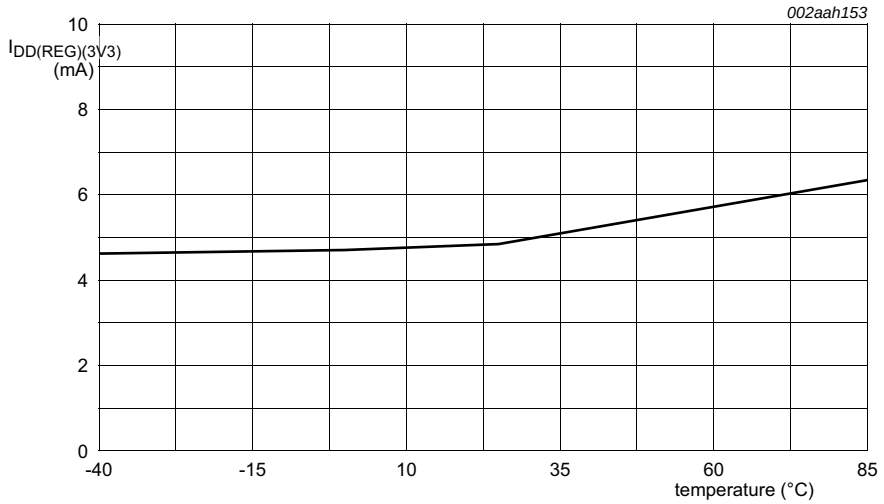
Table 10. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(IO)} \geq 2.2$ V		0	-	5.5	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	86	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	76	mA
I_{pd}	pull-down current	$V_I = V_{DD(IO)}$	[14] [15] [16]	-	62	-	µA
I_{pu}	pull-up current	V_I = 0 V	[14] [15] [16]	-	−62	-	µA
		$V_{DD(IO)} < V_I \leq 5$ V		-	0	-	µA
Open-drain I^2C0-bus pins							
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			0	0.14	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[13]	-	4.5	-	µA
		V_I = 5 V		-	-	10	µA



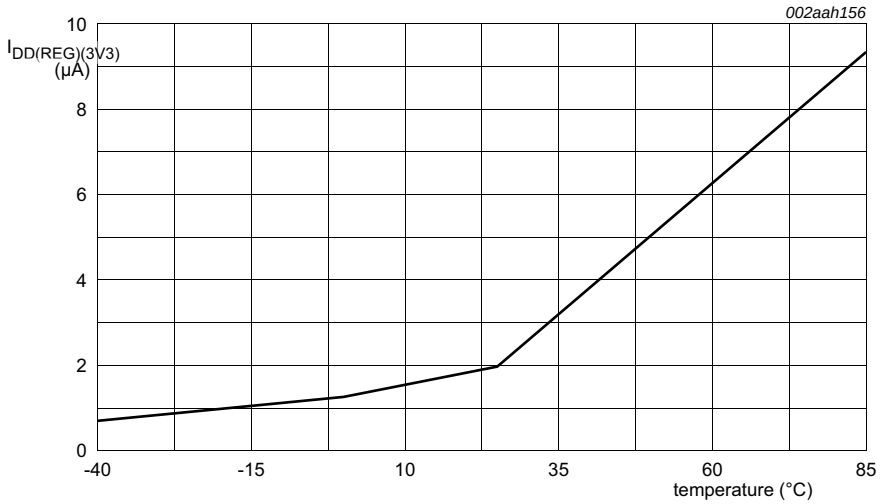
Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; Active mode entered executing code while(1){} from SRAM; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 12. Typical supply current versus frequency in Active mode



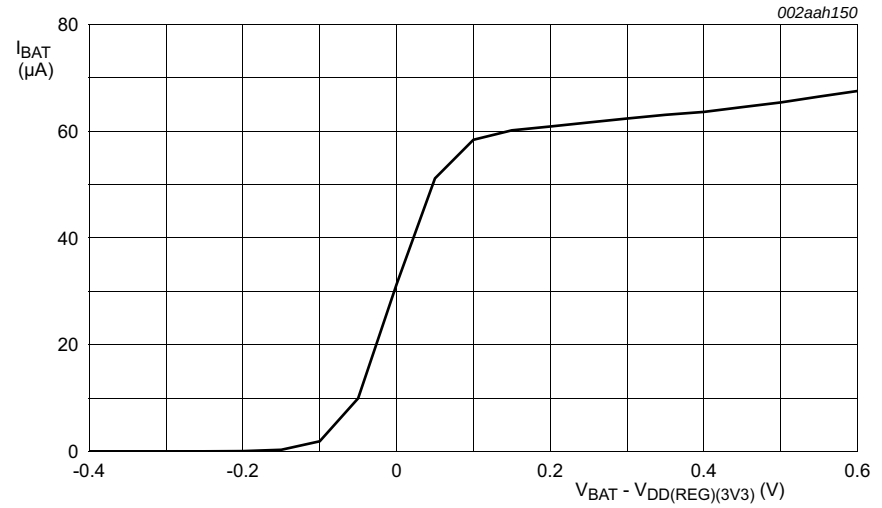
Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled; core clock CCLK = 12 MHz.

Fig 13. Typical supply current versus temperature in Sleep mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} floating; $V_{DD(IO)}$ = 3.3 V.

Fig 16. Typical supply current versus temperature in Deep power-down mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.0 V; CCLK = 12 MHz.

Fig 17. Typical battery supply current in Active mode

Table 11. Peripheral power consumption

Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
ETHERNET	CLK_M3_ETHERNET	1.05	2.09
UART0	CLK_M3_UART0, CLK_APB0_UART0	0.3	0.38
UART1	CLK_M3_UART1, CLK_APB0_UART1	0.27	0.48
UART2	CLK_M3_UART2, CLK_APB2_UART2	0.27	0.47
UART3	CLK_M3_USART3, CLK_APB2_UART3	0.29	0.49
TIMER0	CLK_M3_TIMER0	0.07	0.14
TIMER1	CLK_M3_TIMER1	0.07	0.14
TIMER2	CLK_M3_TIMER2	0.07	0.15
TIMER3	CLK_M3_TIMER3	0.06	0.11
SDIO	CLK_M3_SDIO, CLK_SDIO	0.79	1.37
SCTimer/PWM	CLK_M3_SCT	0.52	1.05
SSP0	CLK_M3_SSP0, CLK_APB0_SSP0	0.12	0.21
SSP1	CLK_M3_SSP1, CLK_APB2_SSP1	0.15	0.28
DMA	CLK_M3_DMA	1.88	3.71
WWDT	CLK_M3_WWDT	0.05	0.08
QEI	CLK_M3_QEI	0.33	0.68
USB0	CLK_M3_USB0, CLK_USB0	1.46	3.32
USB1	CLK_M3_USB1, CLK_USB1	2.83	5.03
RITIMER	CLK_M3_RITIMER	0.04	0.08
EMC	CLK_M3_EMC, CLK_M3_EMC_DIV	3.6	6.97
SCU	CLK_M3_SCU	0.09	0.23
CREG	CLK_M3_CREG	0.37	0.72

11. Dynamic characteristics

11.1 Wake-up times

Table 13. Dynamic characteristic: Wake-up from Deep-sleep, Power-down, and Deep power-down modes

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode	[2]	$3 \times T_{cy(clk)}$	$5 \times T_{cy(clk)}$	-	ns
		from Deep-sleep and Power-down mode		12	51	-	µs
		from Deep power-down mode		-	250	-	µs
		after reset		-	250	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{cy(clk)}$ = 1/CCLK with CCLK = CPU clock frequency.

11.2 External clock for oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.2 V (see Table 10). For connecting the oscillator to the XTAL pins, also see Section 13.2 and Section 13.4.

Table 14. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ over specified ranges.[1]

Symbol	Parameter	Min	Max	Unit
f_{osc}	oscillator frequency	1	25	MHz
$T_{cy(clk)}$	clock cycle time	40	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

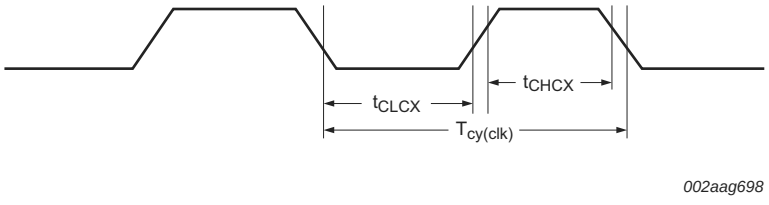


Fig 25. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

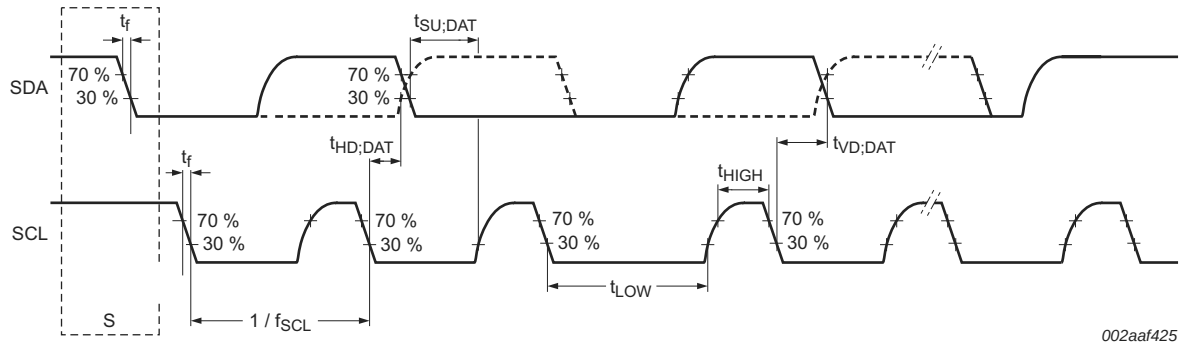


Fig 26. I^2C-bus pins clock timing

11.9 I^2S-bus interface

Table 21. Dynamic characteristics: I^2S-bus interface pins

T_{amb} = 25 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I^2S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I^2S-bus interface PCLK = BASE_APB1_CLK / 12. I^2S clock cycle time $T_{cy(clk)}$ = 79.2 ns; corresponds to the SCK signal in the *I^2S-bus specification*.

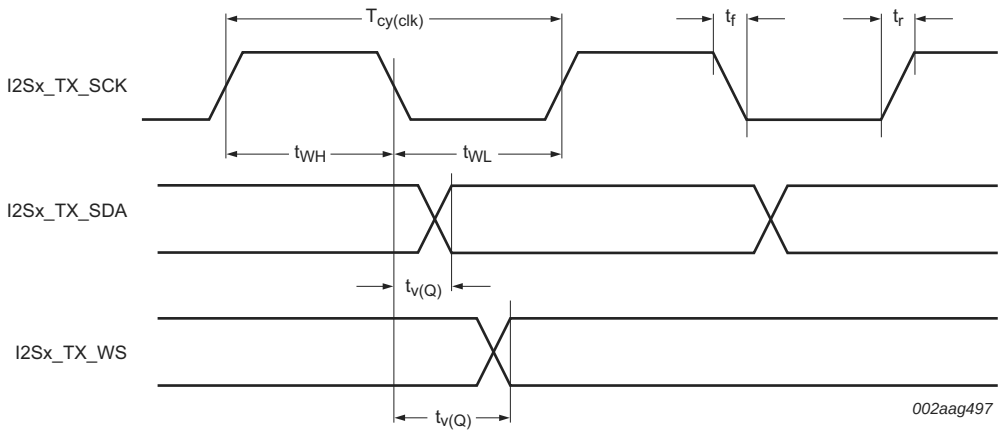


Fig 27. I²S-bus timing (transmit)

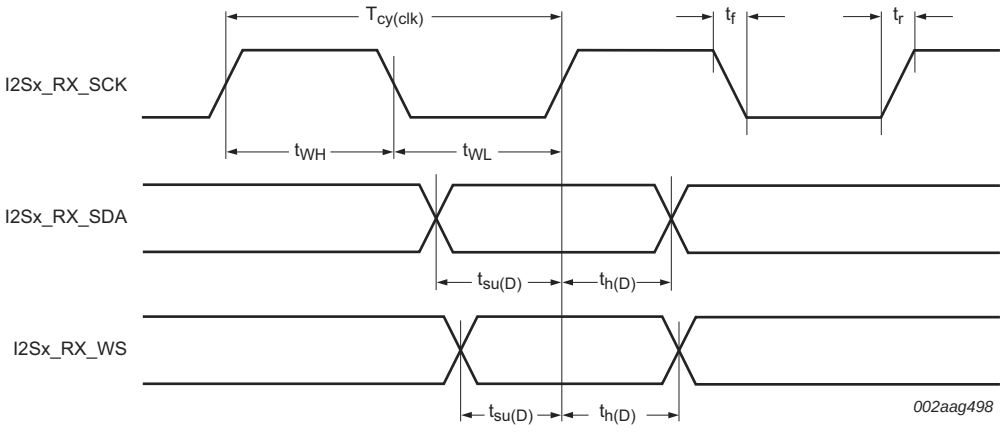


Fig 28. I²S-bus timing (receive)

11.10 USART interface

Table 22. USART dynamic characteristics

T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Min	Max	Unit
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	26.6	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	0	8.8	ns
USART slave (in synchronous mode)				
$t_{su(D)}$	data input set-up time	1.2	-	ns
$t_{h(D)}$	data input hold time	0.4	-	ns
$t_{v(Q)}$	data output valid time	5.5	24	ns

11.11 SSP interface

Table 23. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SSP master							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	$1/(25.5 \times 10^6)$	-	-	s
		when only transmitting		$1/(51 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		13.6	-	-	ns
t_{DH}	data hold time	in SPI mode		−3.8	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	6.0	ns
$t_{h(Q)}$	data output hold time	in SPI mode		−1.1	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)} + 3.2$	-	$T_{cy(clk)} + 6.1$	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)} + 3.2$	-	$0.5 \times T_{cy(clk)} + 6.1$	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)} + 3.2$	-	$T_{cy(clk)} + 6.1$	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)} + 3.2$	-	$0.5 \times T_{cy(clk)} + 6.1$	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)} + 3.2$	-	$0.5 \times T_{cy(clk)} + 6.1$	ns
		microwire frame format		$T_{cy(clk)} + 3.2$	-	$T_{cy(clk)} + 6.1$	ns
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$	-	-	ns
		microwire frame format		$0.5 \times T_{cy(clk)}$	-	-	ns

12. ADC/DAC electrical characteristics

Table 33. ADC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance			-	-	2	pF
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1][2]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[3]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[4]	-	±0.15	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.15	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[5]	-	±0.3	-	%
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.35	-	%
E_T	absolute error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[6]	-	±3	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±4	-	LSB
R_{vsi}	voltage source interface resistance	see Figure 40		-	-	$1/(7 \times f_{clk(ADC)} \times C_{ia})$	kΩ
R_i	input resistance		[7][8]	-	-	1.2	MΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	4.5	MHz
f_s	sampling frequency	10-bit resolution; 11 clock cycles		-	-	400	kSamples/s
		2-bit resolution; 3 clock cycles				1.5	MSamples/s

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 39.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 39.

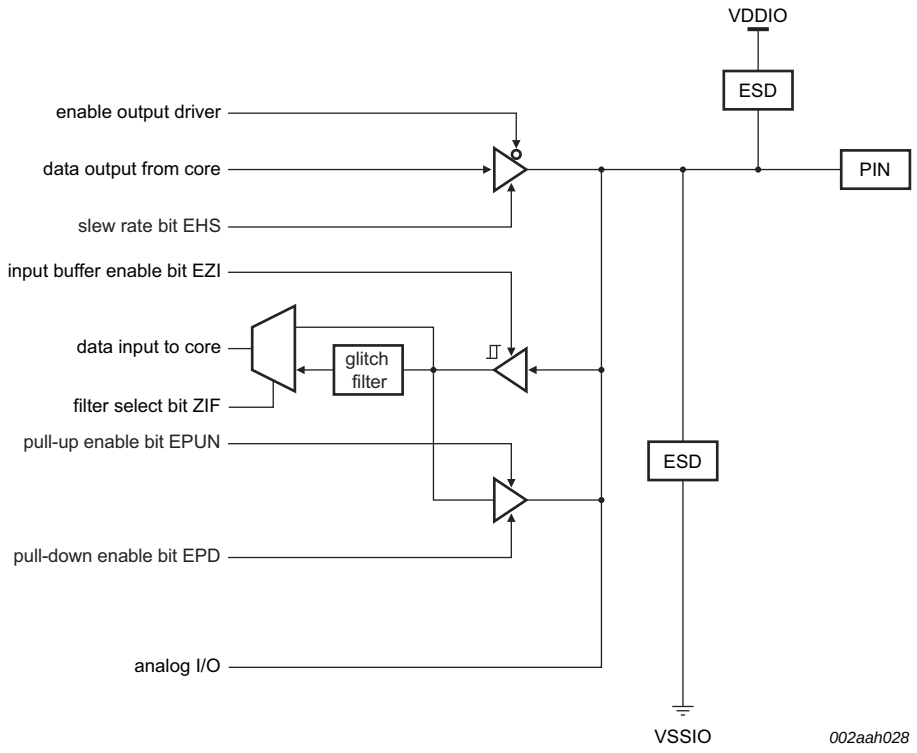
[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 39.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 39.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 39.

[7] T_{amb} = 25 °C.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 2\ k\Omega + 1 / (f_s \times C_{ia})$.



The glitch filter rejects pulses of typical 12 ns width.

Fig 44. Standard I/O pin configuration with analog input

13.6 Reset pin configuration

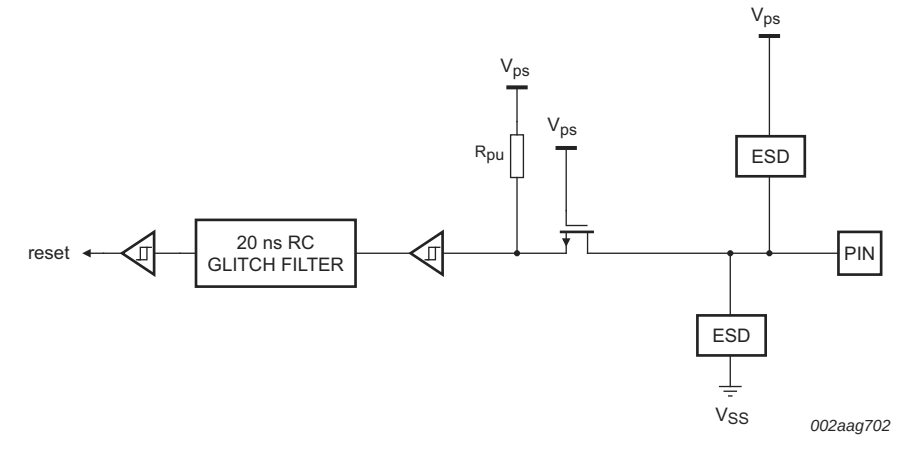


Fig 45. Reset pin configuration

13.7 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 46) or bus-powered device (see Figure 47).

On the LPC1850/30/20/10, USBn_VBUS pins are 5 V tolerant only when VDDIO is applied and at operating voltage level. Therefore, if the USBn_VBUS function is connected to the USB connector and the device is self-powered, the USBn_VBUS pins must be protected for situations when VDDIO = 0 V.

If VDDIO is always at operating level while VBUS = 5 V, the USBn_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where VDDIO can be 0 V and VBUS is directly applied to the USBn_VBUS pins, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USBn_VBUS pins in this case.

One method is to use a voltage divider to connect the USBn_VBUS pins to VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than 0.7VDDIO to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

VDDIO = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

For bus-powered devices, a regulator powered by USB can provide 3.3 V to VDDIO whenever bus power is present and ensure that power to the USBn_VBUS pins is always present when the 5 V VBUS signal is applied. See Figure 47.

Remark: Applying 5 V to the USBn_VBUS pins for a short time while the regulator ramps up might compromise the long-term reliability of the part but does not affect its function.

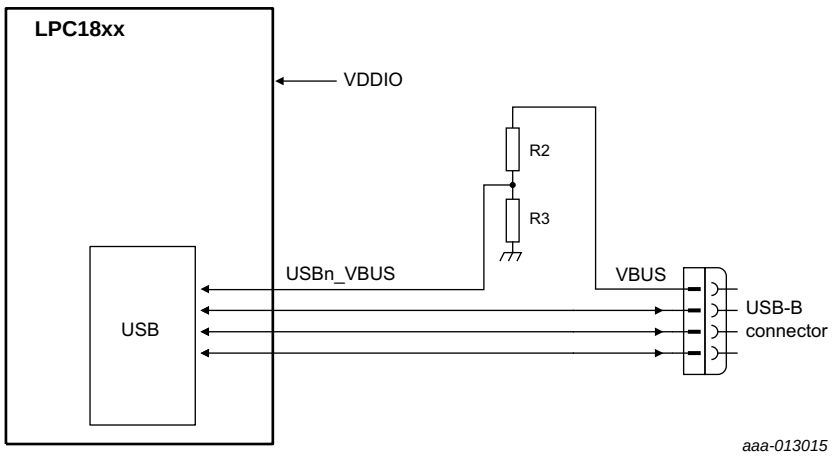
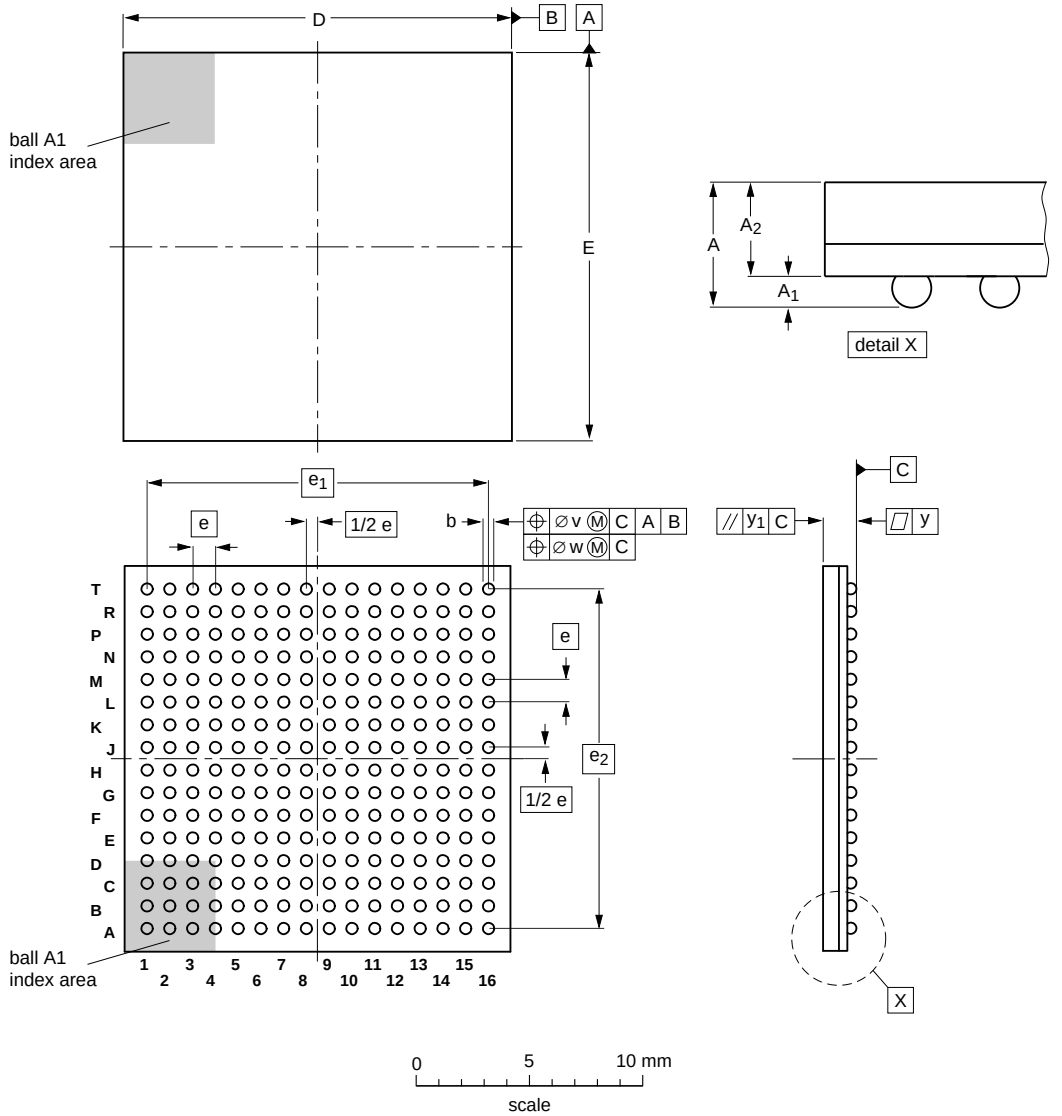


Fig 46. USB interface on a self-powered device where USBn_VBUS = 5 V

14. Package outline

LBGA256: plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm **SOT740-2**



DIMENSIONS (mm are the original dimensions)

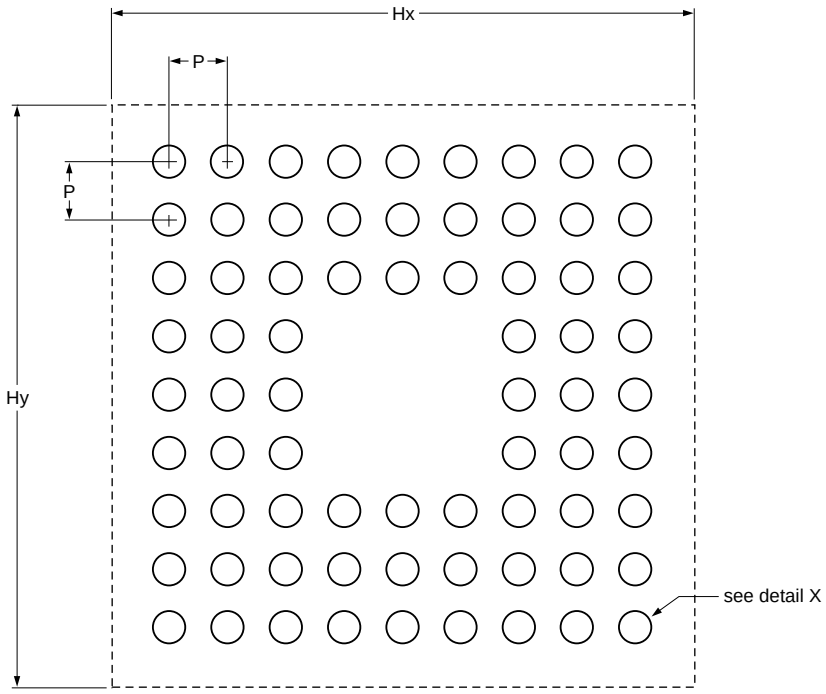
UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.55	0.45 0.35	1.1 0.9	0.55 0.45	17.2 16.8	17.2 16.8	1	15	15	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT740-2	- - -	MO-192	- - -			~~05-06-16~~ 05-08-04

Fig 49. Package outline of the LBGA256 package

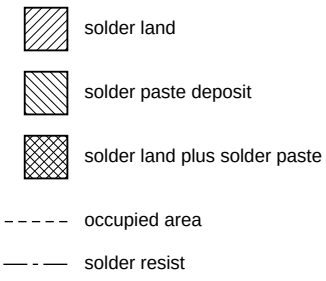
15. Soldering

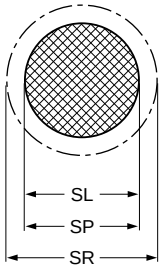
Footprint information for reflow soldering of LBGA256 package **SOT740-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
1.00	0.450	0.450	0.600	17.500	17.500

sot740-2_fr

Fig 53. Reflow soldering of the LBGA256 package

Table 40. Abbreviations *...continued*

Acronym	Description
USART	Universal Synchronous Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface

17. References

[1] LPC18xx User manual UM10430: http://www.nxp.com/documents/user_manual/UM10430.pdf

[2] LPC18X0 Errata sheet: http://www.nxp.com/documents/errata_sheet/ES_LPC18X0.pdf

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Document status[1][2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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