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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	83
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1830fbd144-551

- Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
- Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- Four general-purpose timer/counters with capture and match capabilities.
- One motor control PWM for three-phase motor control.
- One Quadrature Encoder Interface (QEI).
- Repetitive Interrupt timer (RI timer).
- Windowed watchdog timer.
- Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
- Alarm timer; can be battery powered.

- Analog peripherals:
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight input channels per ADC.
- Unique ID for each device.
- Power:
  - Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
  - Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.
  - Brownout detect with four separate thresholds for interrupt and forced reset.
  - Power-On Reset (POR).
- Available as 144-pin LQFP packages and as 256-pin, 180-pin, and 100-pin BGA packages.

3. Applications

- Industrial
- Consumer
- White goods
- RFID readers
- e-Metering

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1850FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1850FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC1830FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1830FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC1830FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1830FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1820FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1820FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1810FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1810FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

4.1 Ordering options

Table 2. Ordering options

Type number	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	ADC channels	Motor control PWM	QEI	GPIO	Package
LPC1850FET256	200 kB	yes	yes	yes	yes/yes	8	yes	yes	164	LBGA256
LPC1850FET180	200 kB	yes	yes	yes	yes/yes	8	yes	yes	118	TFBGA180
LPC1830FET256	200 kB	no	yes	yes	yes/yes	8	yes	yes	164	LBGA256
LPC1830FET180	200 kB	no	yes	yes	yes/yes	8	yes	yes	118	TFBGA180
LPC1830FET100	200 kB	no	yes	yes	yes/no	4	no	no	49	TFBGA100
LPC1830FBD144	200 kB	no	yes	yes	yes/no	8	yes	no	83	LQFP144
LPC1820FET100	168 kB	no	no	yes	no	4	no	no	49	TFBGA100
LPC1820FBD144	168 kB	no	no	yes	no	8	yes	no	83	LQFP144
LPC1810FET100	136 kB	no	no	no	no	4	no	no	49	TFBGA100
LPC1810FBD144	136 kB	no	no	no	no	8	yes	no	83	LQFP144

6. Pinning information

6.1 Pinning

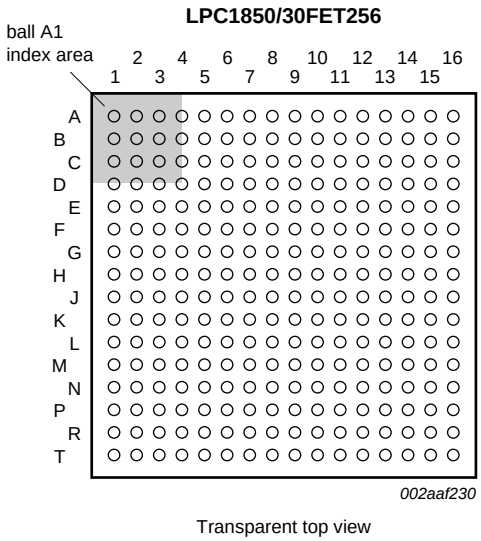


Fig 2. Pin configuration LBGA256 package

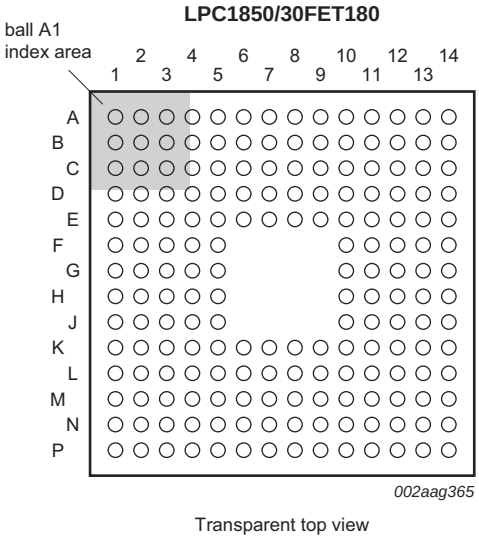


Fig 3. Pin configuration TFBGA180 package

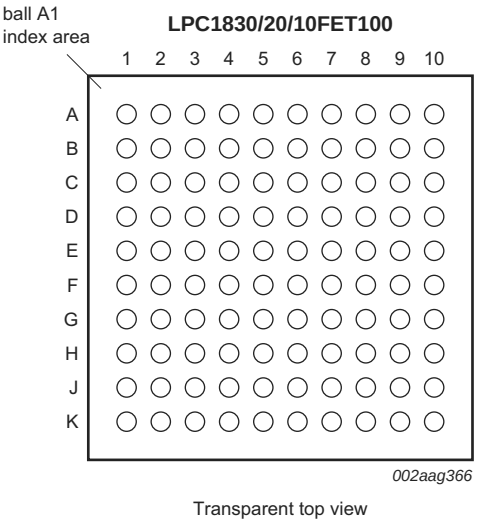


Fig 4. Pin configuration TFBGA100 package

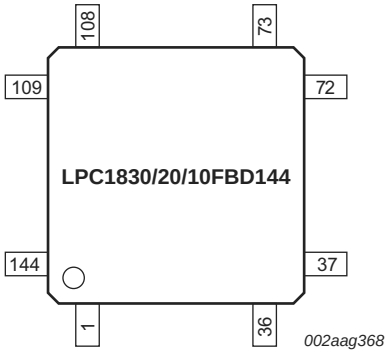


Fig 5. Pin configuration LQFP144 package

6.2 Pin description

On the LPC1850/30/20/10, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Not all functions listed in Table 3 are available on all packages. See Table 2 for availability of USB0, USB1, Ethernet, and LCD functions.

The parts contain two 10-bit ADCs (ADC0 and ADC1). The input channels of ADC0 and ADC1 on dedicated pins and multiplexed pins are combined in such a way that all channel 0 inputs (named ADC0_0 and ADC1_0) are tied together and connected to both, channel 0 on ADC0 and channel 0 on ADC1, channel 1 inputs (named ADC0_1 and ADC1_1) are tied together and connected to channel 1 on ADC0 and ADC1, and so forth. There are eight ADC channels total for the two ADCs.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_5	R5	N3	J4	48	[2]	N; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS0}}$ —** LOW active Chip Select 0 signal.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**SD_POW —** SD/MMC card power monitor output.
P1_6	T4	P3	K4	49	[2]	N; PU	I/O	**GPIO1[9] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_WE}}$ —** LOW active Write Enable signal.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CMD —** SD/MMC command signal.
P1_7	T5	N4	G4	50	[2]	N; PU	I/O	**GPIO1[0] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D0 —** External memory data line 0.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_12	R9	P7	K7	56	[2]	N; PU	I/O	**GPIO1[5] —** General purpose digital input/output pin.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D5 —** External memory data line 5.
							I	**T0_CAP1 —** Capture input 1 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT3 —** SD/MMC data bus line 3.
P1_13	R10	L8	H8	60	[2]	N; PU	I/O	**GPIO1[6] —** General purpose digital input/output pin.
							O	**U1_TXD —** Transmitter output for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D6 —** External memory data line 6.
							I	**T0_CAP0 —** Capture input 0 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**SD_CD —** SD/MMC card detect input.
P1_14	R11	K7	J8	61	[2]	N; PU	I/O	**GPIO1[7] —** General purpose digital input/output pin.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D7 —** External memory data line 7.
							O	**T0_MAT2 —** Match output 2 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P1_15	T12	P11	K8	62	[2]	N; PU	I/O	**GPIO0[2] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
							O	**T0_MAT1 —** Match output 1 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_20	M10	J10	K10	70	[2]	N; PU	I/O	**GPIO0[15] —** General purpose digital input/output pin.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
							I	**T0_CAP2 —** Capture input 2 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_0	T16	N14	G10	75	[2]	N; PU	-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0.
							I/O	**EMC_A13 —** External memory address line 13.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active high). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							I/O	**GPIO5[0] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input 0 of timer 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
P2_1	N15	M13	G7	81	[2]	N; PU	-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.
							I/O	**EMC_A12 —** External memory address line 12.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**GPIO5[1] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input 1 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P3_1	G11	D10	F7	114	[2]	N; PU	I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I	**CAN0_RD —** CAN receiver input.
							O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
							I/O	**GPIO5[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD15 —** LCD data.
							-	**R —** Function reserved.
P3_2	F11	D9	G6	116	[2]	OL; PU	I/O	**I2S0_TX_SDA —** I²S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S0_RX_SDA —** I²S receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**CAN0_TD —** CAN transmitter output.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							I/O	**GPIO5[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
P3_3	B14	B13	A7	118	[4]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							O	**SPIFI_SCK —** Serial clock for SPIFI.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I²S transmit master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I²S-bus specification.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P7_4	C8	C6	-	132	[5]	N; PU	I/O	**GPIO3[12] —** General purpose digital input/output pin.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD16 —** LCD data.
							O	**LCD_VD4 —** LCD data.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_4 —** ADC0 and ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_5	A7	A7	-	133	[5]	N; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD8 —** LCD data.
							O	**LCD_VD23 —** LCD data.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	F5	-	134	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
							O	**CTOUT_11 —** SCTimer/PWM output 1. Match output 3 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P8_3	J3	H3	-	-	[2]	N; PU	I/O	**GPIO4[3] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
							-	**R —** Function reserved.
							O	**LCD_VD12 —** LCD data.
							O	**LCD_VD19 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT3 —** Match output 3 of timer 0.
P8_4	J2	H2	-	-	[2]	N; PU	I/O	**GPIO4[4] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
							-	**R —** Function reserved.
							O	**LCD_VD7 —** LCD data.
							O	**LCD_VD16 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**T0_CAP0 —** Capture input 0 of timer 0.
P8_5	J1	H1	-	-	[2]	N; PU	I/O	**GPIO4[5] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
							-	**R —** Function reserved.
							O	**LCD_VD6 —** LCD data.
							O	**LCD_VD8 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**T0_CAP1 —** Capture input 1 of timer 0.
P8_6	K3	J3	-	-	[2]	N; PU	I/O	**GPIO4[6] —** General purpose digital input/output pin.
							I	**USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY.
							-	**R —** Function reserved.
							O	**LCD_VD5 —** LCD data.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**T0_CAP2 —** Capture input 2 of timer 0.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PE_11	D16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							O	**U1_TXD —** Transmitter output for UART1.
							I/O	**EMC_D30 —** External memory data line 30.
							I/O	**GPIO7[11] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_12	D15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2.
							I	**U1_RXD —** Receiver input for UART1.
							I/O	**EMC_D31 —** External memory data line 31.
							I/O	**GPIO7[12] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_13	G14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
							O	**EMC_DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
							I/O	**GPIO7[13] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_14	C15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_DYCS3}}$ —** SDRAM chip select 3.
							I/O	**GPIO7[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PE_15	E13	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
							O	**EMC_CKEOUT3 —** SDRAM clock enable 3.
							I/O	**GPIO7[15] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PF_0	D12	-	-	-	[2]	OL; PU	I/O	**SSP0_SCK —** Serial clock for SSP0.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S1_TX_MCLK —** I^2S1 transmit master clock.
PF_1	E11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							-	**R —** Function reserved.
							I/O	**GPIO7[16] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PF_2	D11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**U3_TXD —** Transmitter output for USART3.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							I/O	**GPIO7[17] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

- MultiMedia Cards (MMC version 4.4)

7.13.5 External Memory Controller (EMC)

The LPC1850/30/20/10 EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and NOR flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

7.13.5.1 Features

- Dynamic memory interface support including single data rate SDRAM. SDRAM maximum frequency of up to 120 MHz.
- Asynchronous static memory device support including RAM, ROM, and NOR flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines-wide static memory support. On parts LPC1820/10 only 8/16 data lines are available.
- 16-bit and 32-bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow auto-refresh through a chip reset if desired.
- SDRAM clock can run at full or half the Cortex-M4 core frequency.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.13.6 High-speed USB Host/Device/OTG interface (USB0)

Remark: USB0 is available on parts LPC1850/30/20 (see Table 2).

The USB OTG module allows the part to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode.

7.13.6.1 Features

- On-chip UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.

7.17.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Alarm interrupt can be generated for a specific date/time.

7.17.2 Alarm timer

The alarm timer is a 16-bit timer and counts down at 1 kHz from a preset value generating alarms in intervals of up to 1 min. The counter triggers a status bit when it reaches 0x00 and asserts an interrupt if enabled.

The alarm timer is part of the RTC power domain and can be battery powered.

7.18 System control

7.18.1 Configuration registers (CREG)

The following settings are controlled in the configuration register block:

- BOD trip settings
- Oscillator output
- DMA-to-peripheral muxing
- Ethernet mode
- Memory mapping
- Timer/USART inputs
- Enabling the USB controllers

In addition, the CREG block contains the part identification and part configuration information.

7.18.2 System Control Unit (SCU)

The system control unit determines the function and electrical mode of the digital pins. By default function 0 is selected for all pins with pull-up enabled. For pins that support a digital and analog function, the ADC function select registers in the SCU enable the analog function.

A separate set of analog I/Os for the ADCs and the DAC as well as most USB pins are located on separate pads and are not controlled through the SCU.

In addition, the clock delay register for the SDRAM EMC_CLK pins and the registers that select the pin interrupts are located in the SCU.

The LPC1850/30/20/10 can wake up from Deep-sleep, Power-down, and Deep power-down modes via the WAKEUP[3:0] pins and interrupts generated by battery powered blocks in the RTC power domain.

7.19 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points.

11.6 GPCLKIN

Table 18. Dynamic characteristic: GPCLKIN
T_{amb} = 25 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Min	Typ	Max	Unit
GP_CLKIN	input frequency	-	-	25	MHz

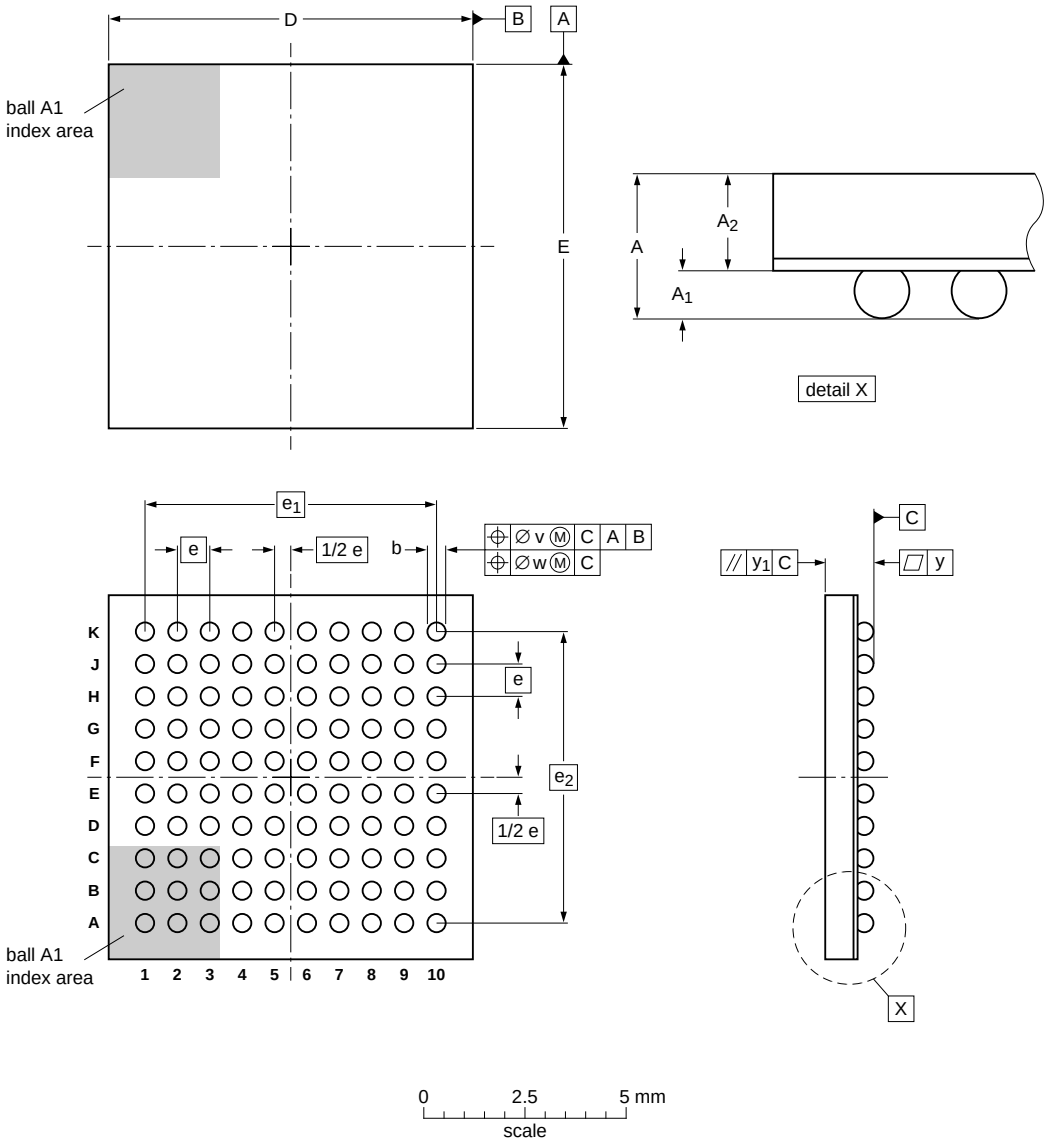
11.7 I/O pins

Table 19. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	1.0	-	2.5	ns
t_f	fall time	pin configured as output; EHS = 1	[2][3]	0.9	-	2.5	ns
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.3	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high drive strength							
t_r	rise time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.3	-	7.9	ns
t_f	fall time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.7	-	8.7	ns
t_r	rise time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.7	ns
t_f	fall time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.5	ns
t_r	rise time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.9	-	4.9	ns
t_f	fall time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.5	-	3.9	ns
t_r	rise time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.8	-	4.7	ns
t_f	fall time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.4	-	3.4	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high-speed							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	350	-	670	ps
t_f	fall time	pin configured as output; EHS = 1	[2][3]	450	-	730	ps
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.0	-	1.9	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.0	-	2.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

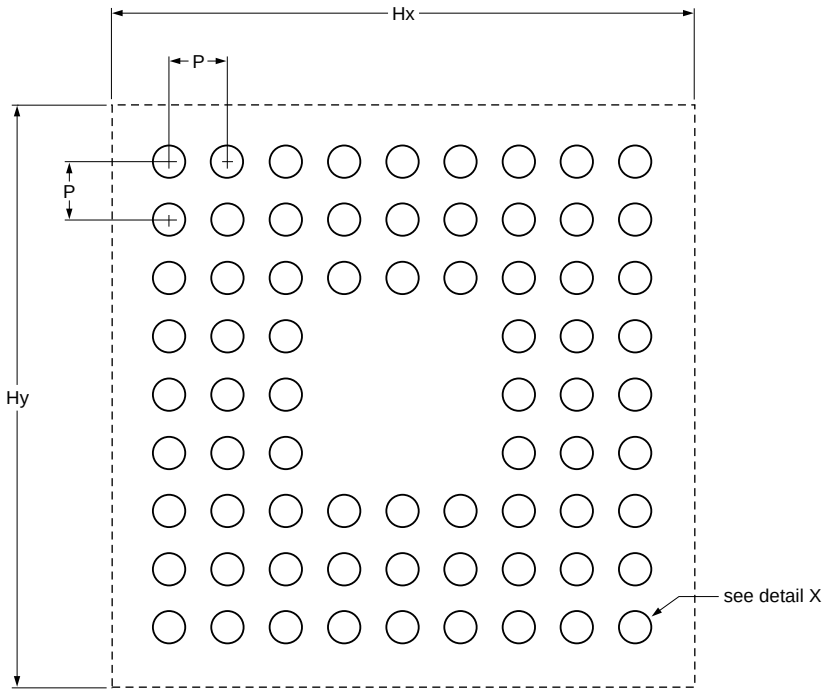
UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 51. Package outline of the TFBGA100 package

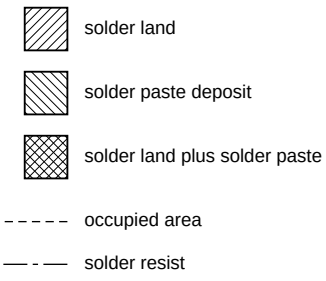
15. Soldering

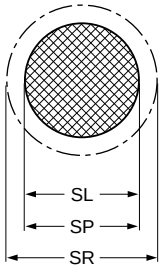
Footprint information for reflow soldering of LBGA256 package **SOT740-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

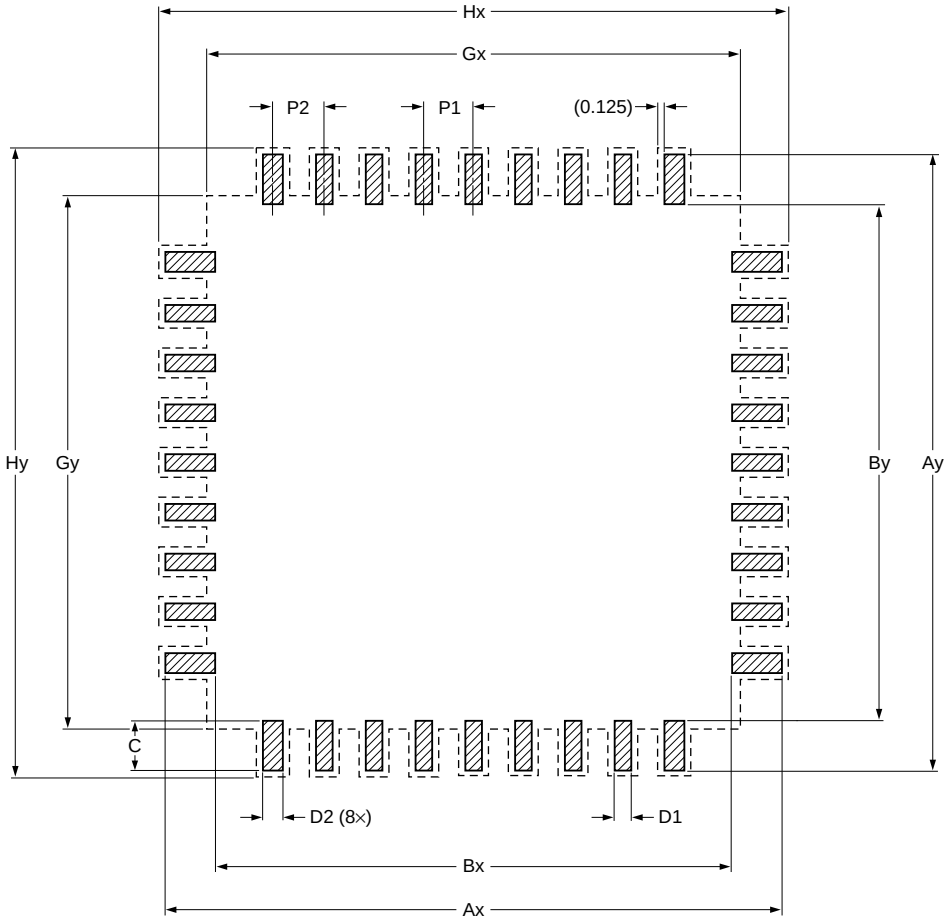
DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
1.00	0.450	0.450	0.600	17.500	17.500

sot740-2_fr

Fig 53. Reflow soldering of the LBGA256 package

Footprint information for reflow soldering of LQFP144 package **SOT486-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot486-1_fr

Fig 55. Reflow soldering of the LQFP144 package

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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