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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	83
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1830fbd144k

6. Pinning information

6.1 Pinning

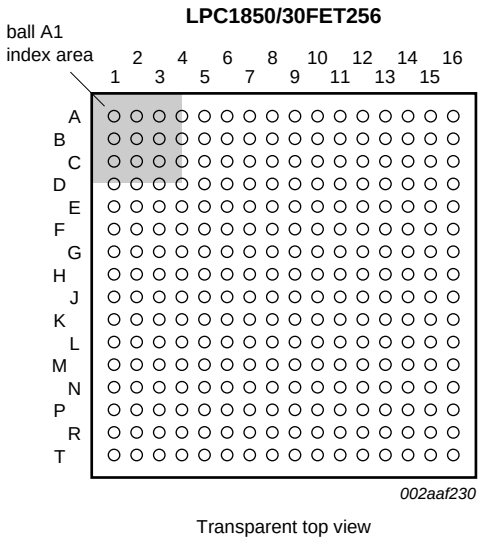

Fig 2. Pin configuration LBGA256 package

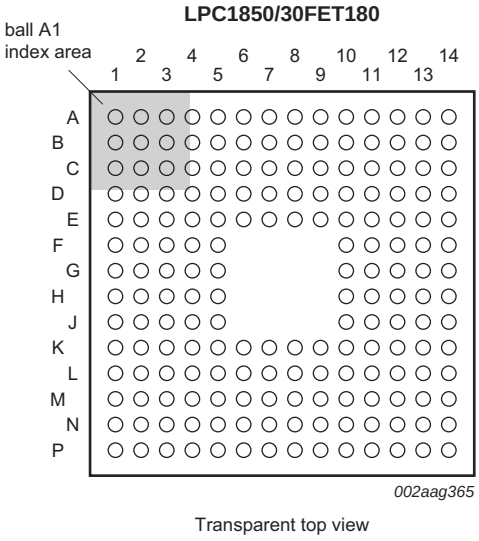

Fig 3. Pin configuration TFBGA180 package

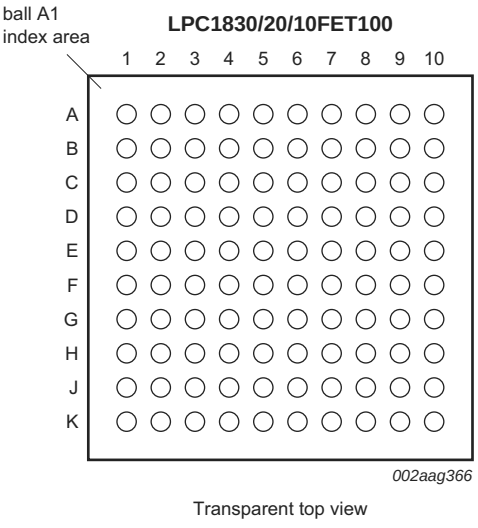

Fig 4. Pin configuration TFBGA100 package

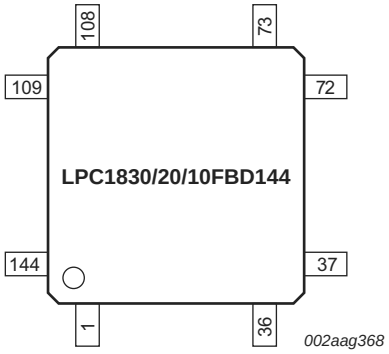

Fig 5. Pin configuration LQFP144 package

6.2 Pin description

On the LPC1850/30/20/10, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Not all functions listed in Table 3 are available on all packages. See Table 2 for availability of USB0, USB1, Ethernet, and LCD functions.

The parts contain two 10-bit ADCs (ADC0 and ADC1). The input channels of ADC0 and ADC1 on dedicated pins and multiplexed pins are combined in such a way that all channel 0 inputs (named ADC0_0 and ADC1_0) are tied together and connected to both, channel 0 on ADC0 and channel 0 on ADC1, channel 1 inputs (named ADC0_1 and ADC1_1) are tied together and connected to channel 1 on ADC0 and ADC1, and so forth. There are eight ADC channels total for the two ADCs.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

7.6 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

- WWDT, BOD interrupts
- C_CAN0/1 and QEI interrupts
- Ethernet, USB0, USB1 signals
- Selected outputs of combined timers (SCTimer/PWM and timer0/1/3)

Remark: Any interrupt can wake up the ARM Cortex-M3 from sleep mode if enabled in the NVIC.

7.7 Global Input Multiplexer Array (GIMA)

The GIMA routes internal and external signals to event-driven peripheral targets like the SCTimer/PWM, timers, event router, or the ADCs.

7.7.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

7.8 On-chip static RAM

The LPC1850/30/20/10 support up to 200 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

Table 5. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
USART0	LOW	LOW	LOW	LOW	Boot from device connected to USART0 using pins P2_0 and P2_1.
SPIFI	LOW	LOW	LOW	HIGH	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1].
EMC 8-bit	LOW	LOW	HIGH	LOW	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	LOW	LOW	HIGH	HIGH	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	LOW	HIGH	LOW	LOW	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	LOW	HIGH	LOW	HIGH	Boot from USB0
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP0)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	HIGH	LOW	LOW	LOW	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using the SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

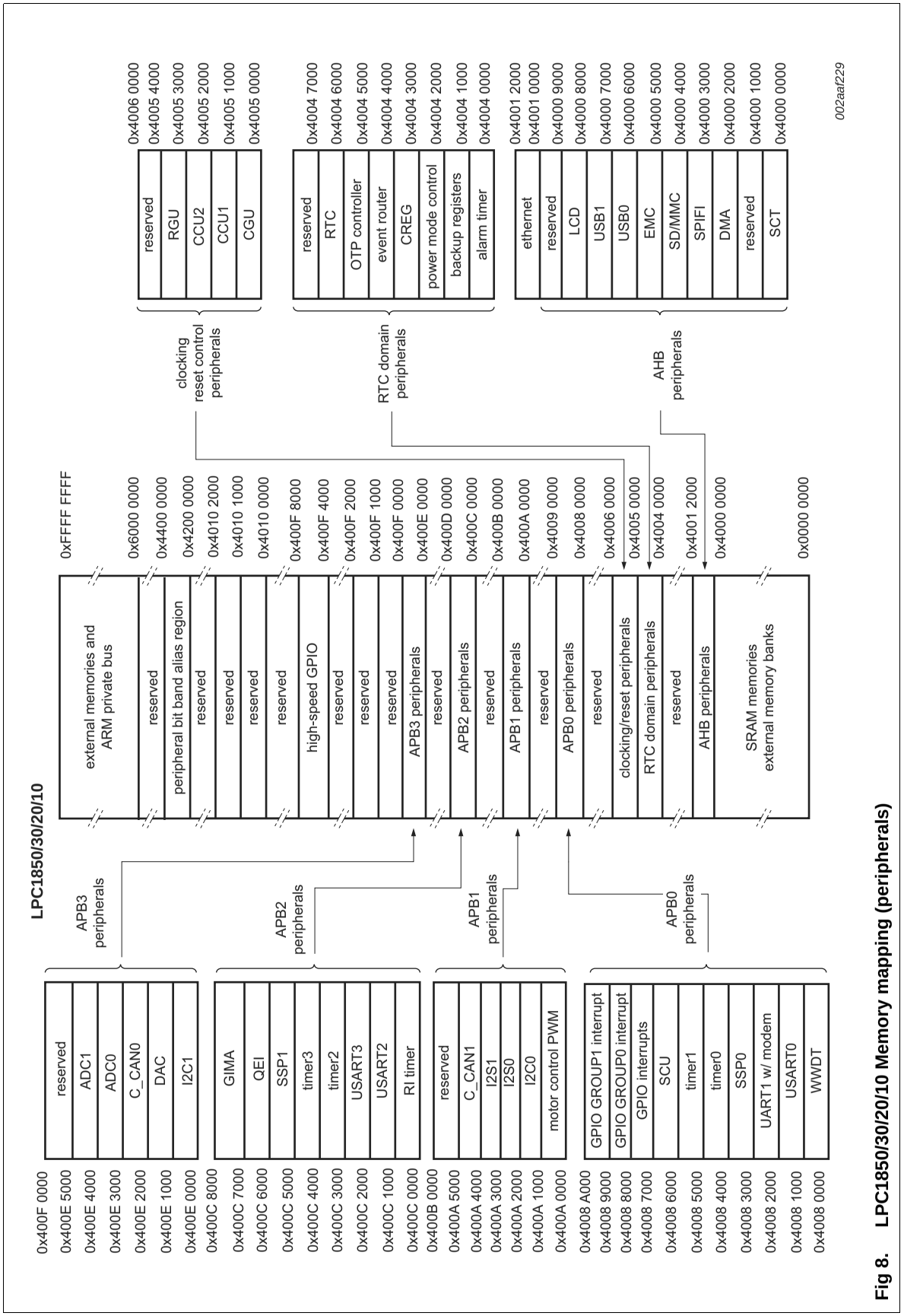

Fig 8. LPC1850/30/20/10 Memory mapping (peripherals)

- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.13.3 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M3 processor with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasing and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.13.3.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
- Supports DMA access.

7.13.4 SD/MMC card interface

The SD/MMC card interface supports the following modes:

- Secure Digital memory (SD version 3.0)
- Secure Digital I/O (SDIO version 2.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1)

7.17.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Alarm interrupt can be generated for a specific date/time.

7.17.2 Alarm timer

The alarm timer is a 16-bit timer and counts down at 1 kHz from a preset value generating alarms in intervals of up to 1 min. The counter triggers a status bit when it reaches 0x00 and asserts an interrupt if enabled.

The alarm timer is part of the RTC power domain and can be battery powered.

7.18 System control

7.18.1 Configuration registers (CREG)

The following settings are controlled in the configuration register block:

- BOD trip settings
- Oscillator output
- DMA-to-peripheral muxing
- Ethernet mode
- Memory mapping
- Timer/USART inputs
- Enabling the USB controllers

In addition, the CREG block contains the part identification and part configuration information.

7.18.2 System Control Unit (SCU)

The system control unit determines the function and electrical mode of the digital pins. By default function 0 is selected for all pins with pull-up enabled. For pins that support a digital and analog function, the ADC function select registers in the SCU enable the analog function.

A separate set of analog I/Os for the ADCs and the DAC as well as most USB pins are located on separate pads and are not controlled through the SCU.

In addition, the clock delay register for the SDRAM EMC_CLK pins and the registers that select the pin interrupts are located in the SCU.

Table 10. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I/O pins - high drive strength: standard drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	32	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	32	mA
I/O pins - high drive strength: medium drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	65	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	63	mA
I/O pins - high drive strength: high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−14	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		14	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	113	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	110	mA
I/O pins - high drive strength: ultra-high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−20	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		20	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	165	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	156	mA
I/O pins - high-speed							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	$V_I = 0$ V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		$V_I = 5$ V		-	-	20	nA

11.3 Crystal oscillator

Table 15. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ over specified ranges; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1 MHz to 20 MHz)[5]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3][4]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps
High-frequency mode (20 MHz to 25 MHz)[6]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3][4]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] PLL-induced jitter is not included.

[5] Select HF = 0 in the XTAL_OSC_CTRL register.

[6] Select HF = 1 in the XTAL_OSC_CTRL register.

11.4 IRC oscillator

Table 16. Dynamic characteristic: IRC oscillator

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-		11.82	12.0	12.18	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.5 RTC oscillator

Table 17. Dynamic characteristic: RTC oscillator

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V or 2.2 V ≤ V_{BAT} ≤ 3.6 V[1]*; typical $C_{RTCX1/2}$ = 20 pF; also see Section 13.3*

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
$f_{i(RTC)}$	RTC input frequency	-		-	32.768	-	kHz
$I_{DD(RTC)}$	RTC supply current				280	800	nA

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.6 GPCLKIN

Table 18. Dynamic characteristic: GPCLKIN
T_{amb} = 25 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Min	Typ	Max	Unit
GP_CLKIN	input frequency	-	-	25	MHz

11.7 I/O pins

Table 19. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	1.0	-	2.5	ns
t_f	fall time	pin configured as output; EHS = 1	[2][3]	0.9	-	2.5	ns
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.3	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high drive strength							
t_r	rise time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.3	-	7.9	ns
t_f	fall time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.7	-	8.7	ns
t_r	rise time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.7	ns
t_f	fall time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.5	ns
t_r	rise time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.9	-	4.9	ns
t_f	fall time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.5	-	3.9	ns
t_r	rise time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.8	-	4.7	ns
t_f	fall time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.4	-	3.4	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high-speed							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	350	-	670	ps
t_f	fall time	pin configured as output; EHS = 1	[2][3]	450	-	730	ps
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.0	-	1.9	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.0	-	2.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the system control block in the SFSP registers using the EHS bit. See the LPC18xx user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

[5] The drive modes are configured in the system control block in the SFSP registers using the EHD bit. See the *LPC18xx user manual*.

11.8 I²C-bus

Table 20. Dynamic characteristic: I²C-bus pins

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[3][4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[2][3][7]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[8][9]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.

[2] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

Table 23. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	$0.5 \times T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	$0.5 \times T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns
SSP slave							
PCLK	Peripheral clock frequency			-	-	180	MHz
$T_{cy(clk)}$	clock cycle time		[2]	$1/(11 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		1.15	-	-	ns
t_{DH}	data hold time	in SPI mode		0.5	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	[4 × (1/PCLK)] + 3	ns
$t_{h(Q)}$	data output hold time	in SPI mode		5.1	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)} + 2.2$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)} + 2.2$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)} + 2.2$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)} + 2.2$	-	-	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)} + 2.2$	-	-	ns
		microwire frame format		$T_{cy(clk)} + 2.2$	-	-	ns

Table 23. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5T_{cy(clk)}$ + 0.2	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$ + 0.2	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		0.5 × $T_{cy(clk)}$ + 0.2	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$ + 0.2	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$ + 0.2	-	-	ns
		microwire frame format		0.5 × $T_{cy(clk)}$	-	-	ns
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.

11.15 SD/MMC

Table 30. Dynamic characteristics: SD/MMC

T_{amb} = −40 °C to 85 °C, 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V, C_L = 20 pF. SAMPLE_DELAY = 0x9, DRV_DELAY = 0xD in the SDDELAY register sampled at 90 % and 10 % of the signal level, EHS = 1 for SD_CLK pin, EHS = 1 for SD_DATn and SD_CMD pins. Simulated values.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode		52	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs	3.9	-	ns
		on pins SD_CMD as inputs	5.2	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs	0.4	-	ns
		on pins SD_CMD as inputs	0		ns
$t_{d(QV)}$	data output valid delay time	on pins SD_DATn as outputs	-	15.3	ns
		on pins SD_CMD as outputs	-	16	ns
$t_{h(Q)}$	data output hold time	on pins SD_DATn as outputs	4	-	ns
		on pins SD_CMD as outputs	4	-	ns

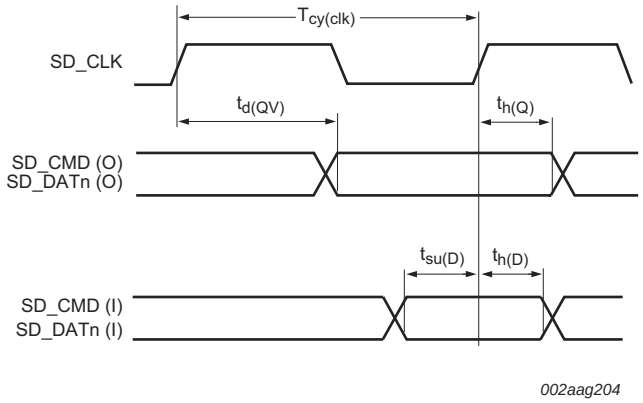

Fig 37. SD/MMC timing

11.16 LCD

Table 31. Dynamic characteristics: LCD

T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	-	MHz
$t_{d(QV)}$	data output valid delay time			-	17	ns
$t_{h(Q)}$	data output hold time		8.5	-		ns

13. Application information

13.1 LCD panel signal usage

Table 35. LCD panel connections for STN single panel mode

External pin	4-bit mono STN single panel		8-bit mono STN single panel		Color STN single panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:8]	-	-	-	-	-	-
LCD_VD7	-	-	P8_4	UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	CDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 36. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:16]	-	-	-	-	-	-
LCD_VD15	-	-	PB_4	LD[7]	PB_4	LD[7]
LCD_VD14	-	-	PB_5	LD[6]	PB_5	LD[6]
LCD_VD13	-	-	PB_6	LD[5]	PB_6	LD[5]
LCD_VD12	-	-	P8_3	LD[4]	P8_3	LD[4]
LCD_VD11	P4_9	LD[3]	P4_9	LD[3]	P4_9	LD[3]
LCD_VD10	P4_10	LD[2]	P4_10	LD[2]	P4_10	LD[2]
LCD_VD9	P4_8	LD[1]	P4_8	LD[1]	P4_8	LD[1]
LCD_VD8	P7_5	LD[0]	P7_5	LD[0]	P7_5	LD[0]
LCD_VD7	-	-		UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]

Table 38. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	< 100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

Table 39. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{x2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

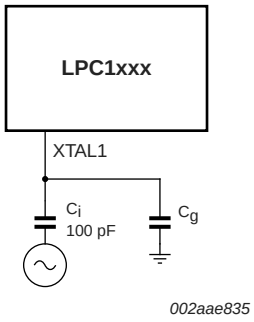

Fig 41. Slave mode operation of the on-chip oscillator

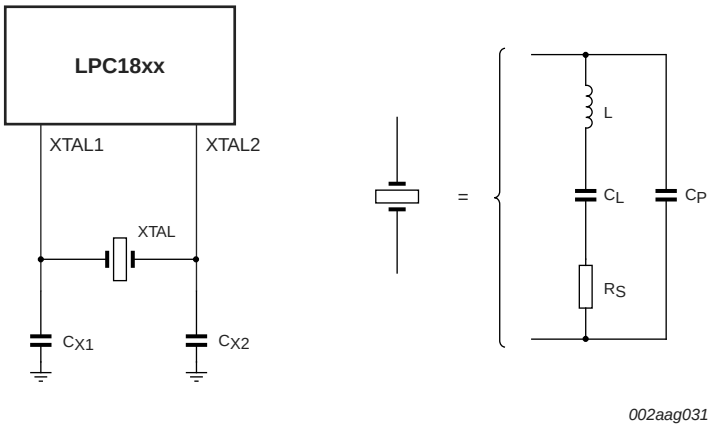

Fig 42. Oscillator modes with external crystal model used for C_{X1}/C_{X2} evaluation

16. Abbreviations

Table 40. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	BrownOut Detection
BGA	Ball Grid Array
CAN	Controller Area Network
CMAC	Cipher-based Message Authentication Code
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
GPIO	General-Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LQFP	Low Quad Flat Package
MAC	Media Access Control
MCU	MicroController Unit
MIIM	Media Independent Interface Management
n.c.	not connected
OTG	On-The-Go
PHY	PHYsical layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface

18. Revision history

Table 41. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1850_30_20_10 v.6.7	20160314	Product data sheet	-	LPC1850_30_20_10 v.6.6
	• Updated Table 25 “Dynamic characteristics: Dynamic external memory interface”: Read cycle parameters $t_{h(D)}$ min value is 2.2 ns and max value is “-”.			
LPC1850_30_20_10 v.6.6	20151116	Product data sheet	2015110031	LPC1850_30_20_10 v.6.5
Modifications:	**Updated SSP slave and SSP master values in Table 23 “Dynamic characteristics: SSP pins in SPI mode”. Updated footnote 2 to: $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.** • **removed $t_{v(Q)}$, data output valid time in SPI mode, minimum value of 3 ´ (1/PCLK) from SSP slave mode.** • **added units to t_d, delay time, for SSP slave and master mode.** **Added GPCLKIN section and table. See Section 11.6 “GPCLKIN” and Table 18 “Dynamic characteristic: GPCLKIN”.**			
LPC1850_30_20_10 v.6.5	20150430	Product data sheet	-	LPC1850_30_20_10 v.6.4
Modifications:	• For WAKEUP pin description: Changed external pull-up to internal pull-up. See Table 3 “Pin description”. • Table note 2 corrected in Table 10. • Updated USART dynamic characteristics table. See Table 22. • Added SSP slave timing data. See Table 22. • Added USART timing diagram. See Figure 29. • Updated SD/MMC dynamic characteristics table. See Table 30. • Updated SPIFI dynamic characteristics table. See Table 32. • Updated Dynamic characteristics: USB0 and USB1 pins (full-speed). See Table 27. • Updated Table 2: Motor control PWM instead of PWM. • Added a remark to Table 27.			
LPC1850_30_20_10 v.6.4	20140818	Product data sheet	201408013F01	LPC1850_30_20_10 v.6.3

Table 41. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• IEEE standard 802.3 compliance added to Section 11.13. Covers Ethernet dynamic characteristics of ENET_MDIO and ENET_MDC signals. • Parameter C_I corrected for high-drive pins (changed from 2 pF to 5.2 pF). See Table 10. • Table 18 “Dynamic characteristic: I/O pins[1]” added. • IRC accuracy changed from 1 % to 1.5 % over the full temperature range. See Table 16 “Dynamic characteristic: IRC oscillator”. • Description of internal pull-up resistor configuration added for $\overline{\text{RESET}}$, WAKEUPn, and ALARM pins. See Table 3. • Description of DEBUG pin updated. • Input range for PLL1 corrected: 1 MHz to 25 MHz. See Section 7.18.7 “System PLL1”. • Section 13.7 “Suggested USB interface solutions” added. • Reset state of the RTC alarm pin RTC_ALARM added. See Table 3. • Signal polarity corrected for signals EMC_CKEOUT and EMC_DQMOUT. Both signals are active HIGH. • SPIFI output timing parameters in Table 31 corrected to apply to Mode 0: – $t_{v(Q)}$ changed to 3.2 ns. – $t_{h(Q)}$ changed to 0.2 ns, • Parameter t_{CSLWEL} with condition PB = 1 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 23 “Dynamic characteristics: Static asynchronous external memory interface”. • Parameter $t_{CSLBLSL}$ with condition PB = 0 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 23 “Dynamic characteristics: Static asynchronous external memory interface”. • SSP master mode timing diagram updated with SSEL timing parameters. See Figure 29 “SSP master timing in SPI mode”. • Parameters t_{lead}, t_{lag}, and t_d added in Table 22 “Dynamic characteristics: SSP pins in SPI mode”.			

Table 41. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1850_30_20_10 v.6.3	20131210	Product data sheet	-	LPC1850_30_20_10 v.6.2
Modifications:	• Maximum value for $V_{i(RMS)}$ added in Section 13.3 “RTC oscillator”. • V_O for RTC_ALARM pin added in Table 10. • RTC_ALARM and WAKEUPn pins added to Table 10.			
LPC1850_30_20_10 v.6.2	20131014	Product data sheet	-	LPC1850_30_20_10 v.6.1
Modifications:	• Parameter I_{LH} (High-level leakage current) for condition V_I = 5 V changed to 20 nA (max). See Table 10. • Parameter $V_{DDA(3V3)}$ added for pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3 in Table 10. • Corrected max voltage on pins USB0_DP, USB0_DM, USB0_VBUS, USB1_DP, and USB1_DM in Table 6 and Table 10 to be consistent with USB specifications. • Description of $\overline{\text{RESET}}$ pin updated in Table 3. • Table note 8 added in Table 10. • Timing parameters in Table 28 “Dynamic characteristics: SD/MMC” corrected. • Band gap characteristics removed. • Part LPC1850FBD208 removed. • OTP memory size available for general-purpose use corrected.			
LPC1850_30_20_10 v.6.1	20130207	Product data sheet	-	LPC1850_30_20_10 v.6
Modifications:	• Table 13 “Band gap characteristics” and Figure 20 “Band gap voltage for different temperatures and process conditions” added. • Table 10, added Table note 2: “Dynamic characteristics for peripherals are provided for $V_{DD(REG)(3V3)} \geq 2.7$ V. • Description of ADC pins on digital/analog input pins changed. Each input to the ADC is connected to ADC0 and ADC1. See Table 3. • Use of C_CAN peripheral restricted in Section 2. • ADC channels limited to a total of 8 channels shared between ADC0 and ADC1. • Minimum value for parameter V_{IL} changed to 0 V in Table 10 “Static characteristics”. • Power consumption in active mode corrected. See parameter $I_{DD(REG)(3V3)}$ in Table 10 and graphs Figure 11, Figure 12, and Figure 13. • Parameter name $I_{DD(ADC)}$ changed to I_{DDA} in Table 10. • Added note to limit data in Table 23 “Dynamic characteristics: Static asynchronous external memory interface” to single memory accesses. • Value of parameter $I_{DD(REG)(3V3)}$ in deep power-down increased to 0.03 µA in Table 10. • Value of parameter $I_{DD(IO)}$ in deep power-down increased to 0.05 µA in Table 10.			