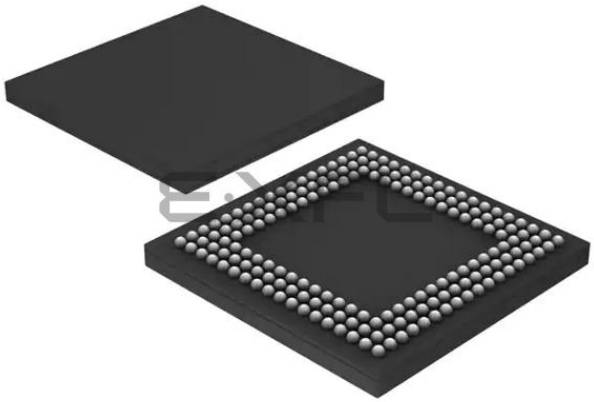

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	118
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1850fet180-551

4. Ordering information

Table 1. Ordering information

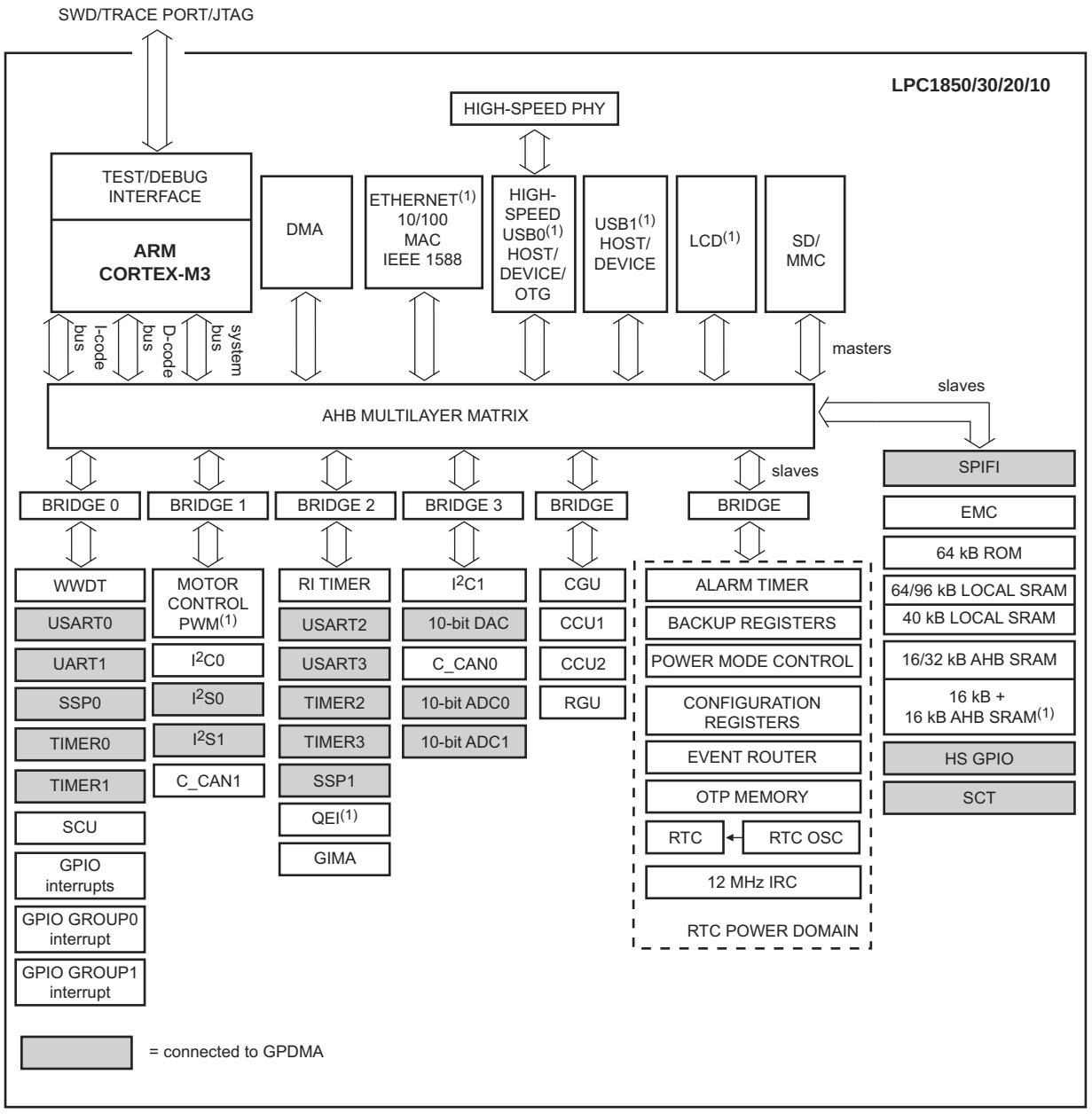
Type number	Package		
	Name	Description	Version
LPC1850FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1850FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC1830FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1830FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC1830FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1830FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1820FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1820FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1810FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1810FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

4.1 Ordering options

Table 2. Ordering options

Type number	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	ADC channels	Motor control PWM	QEI	GPIO	Package
LPC1850FET256	200 kB	yes	yes	yes	yes/yes	8	yes	yes	164	LBGA256
LPC1850FET180	200 kB	yes	yes	yes	yes/yes	8	yes	yes	118	TFBGA180
LPC1830FET256	200 kB	no	yes	yes	yes/yes	8	yes	yes	164	LBGA256
LPC1830FET180	200 kB	no	yes	yes	yes/yes	8	yes	yes	118	TFBGA180
LPC1830FET100	200 kB	no	yes	yes	yes/no	4	no	no	49	TFBGA100
LPC1830FBD144	200 kB	no	yes	yes	yes/no	8	yes	no	83	LQFP144
LPC1820FET100	168 kB	no	no	yes	no	4	no	no	49	TFBGA100
LPC1820FBD144	168 kB	no	no	yes	no	8	yes	no	83	LQFP144
LPC1810FET100	136 kB	no	no	no	no	4	no	no	49	TFBGA100
LPC1810FBD144	136 kB	no	no	no	no	8	yes	no	83	LQFP144

5. Block diagram



(1) Not available on all parts (see Table 2).

Fig 1. LPC1850/30/20/10 block diagram

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P2_5	K14	J12	D10	91	[3]	N; PU	-	**R —** Function reserved.
							I	**CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0.
							I	**USB1_VBUS —** Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
							I	**ADCTRIG1 —** ADC trigger input 1.
							I/O	**GPIO5[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output 2 of timer 3.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
P2_6	K16	J14	G9	95	[2]	N; PU	-	**R —** Function reserved.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							I/O	**EMC_A10 —** External memory address line 10.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**GPIO5[6] —** General purpose digital input/output pin.
							I	**CTIN_7 —** SCTimer/PWM input 7.
							I	**T3_CAP3 —** Capture input 3 of timer 3.
							-	**R —** Function reserved.
P2_7	H14	G12	C10	96	[2]	N; PU	I/O	**GPIO0[7] —** General purpose digital input/output pin. ISP entry pin. If this pin is pulled LOW at reset, the part enters ISP mode using USART0.
							O	**CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							I/O	**EMC_A9 —** External memory address line 9.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output 3 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PC_3	F5	-	-	-	[5]	N; PU	I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
							-	**R —** Function reserved.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**GPIO6[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.
							AI	**ADC1_0 —** ADC1 and ADC0, input channel shared with DAC output. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PC_4	F4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
							-	**R —** Function reserved.
								ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
							I/O	**GPIO6[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input 1 of timer 3.
							I/O	**SD_DAT0 —** SD/MMC data bus line 0.
PC_5	G4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
							-	**R —** Function reserved.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**GPIO6[4] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP2 —** Capture input 2 of timer 3.
							I/O	**SD_DAT1 —** SD/MMC data bus line 1.
PC_6	H6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
							-	**R —** Function reserved.
							I	**ENET_RXD2 —** Ethernet receive data 2 (MII interface).
							I/O	**GPIO6[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP3 —** Capture input 3 of timer 3.
							I/O	**SD_DAT2 —** SD/MMC data bus line 2.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PD_8	P8	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							I/O	**EMC_D22 —** External memory data line 22.
							-	**R —** Function reserved.
							I/O	**GPIO6[22] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_9	T11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D23 —** External memory data line 23.
							-	**R —** Function reserved.
							I/O	**GPIO6[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_10	P11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_1 —** SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							O	**$\overline{\text{EMC\_BLS3}}$ —** LOW active Byte Lane select signal 3.
							-	**R —** Function reserved.
							I/O	**GPIO6[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_11	N9	M7	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS3}}$ —** LOW active Chip Select 3 signal.
							-	**R —** Function reserved.
							I/O	**GPIO6[25] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PD_16	R14	P12	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A16 —** External memory address line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[30] —** General purpose digital input/output pin.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
PE_0	P14	N12	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A18 —** External memory address line 18.
							I/O	**GPIO7[0] —** General purpose digital input/output pin.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_1	N14	M12	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A19 —** External memory address line 19.
							I/O	**GPIO7[1] —** General purpose digital input/output pin.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_2	M14	L12	-	-	[2]	N; PU	I	**ADCTRIG0 —** ADC trigger input 0.
							I	**CAN0_RD —** CAN receiver input.
							-	**R —** Function reserved.
							I/O	**EMC_A20 —** External memory address line 20.
							I/O	**GPIO7[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PF_9	D6	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							O	**CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**GPIO7[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC1_2 —** ADC1 and ADC0, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_10	A3	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**SD_WP —** SD/MMC card write protect input.
							-	**R —** Function reserved.
							AI	**ADC0_5 —** ADC0 and ADC1, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_11	A2	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[25] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							-	**R —** Function reserved.
							AI	**ADC1_5 —** ADC1 and ADC0, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
Debug pins								
DBGEN	L4	K4	A6	28	[2]	I; PU	I	JTAG interface control signal. Also used for boundary scan. To use the part in functional mode, connect this pin in one of the following ways: • Leave DBGEN open. The DBGEN pin is pulled up internally by a 50 kΩ resistor. • Tie DBGEN to VDDIO. • Pull DBGEN up to VDDIO with an external pull-up resistor.
TCK/SWDCLK	J5	G5	H2	27	[2]	I; F	I	Test Clock for JTAG interface (default) or Serial Wire (SW) clock.
$\overline{\text{TRST}}$	M4	L4	B4	29	[2]	I; PU	I	Test Reset for JTAG interface.
TMS/SWDIO	K6	K5	C4	30	[2]	I; PU	I	Test Mode Select for JTAG interface (default) or SW debug data input/output.
TDO/SWO	K5	J5	H3	31	[2]	O	O	Test Data Out for JTAG interface (default) or SW trace output.
TDI	J4	H4	G3	26	[2]	I; PU	I	Test Data In for JTAG interface.
USB0 pins								
USB0_DP	F2	E2	E1	18	[6]	-	I/O	USB0 bidirectional D+ line. Do not add an external series resistor.
USB0_DM	G2	F2	E2	20	[6]	-	I/O	USB0 bidirectional D− line. Do not add an external series resistor.
USB0_VBUS	F1	E1	E3	21	[6] [7]	-	I/O	VBUS pin (power on USB cable). This pin includes an internal pull-down resistor of 64 kΩ (typical) ± 16 kΩ.
USB0_ID	H2	G2	F1	22	[8]	-	I	Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH). For use with OTG, this pin has an internal pull-up resistor.
USB0_RREF	H1	G1	F3	24	[8]	-		12.0 kΩ (accuracy 1 %) on-board resistor to ground for current reference.
USB1 pins								
USB1_DP	F12	D11	E9	89	[9]	-	I/O	USB1 bidirectional D+ line. Add an external series resistor of 33 Ω +/- 2 %.
USB1_DM	G12	E11	E10	90	[9]	-	I/O	USB1 bidirectional D− line. Add an external series resistor of 33 Ω +/- 2 %.
I^2C-bus pins								
I2C0_SCL	L15	K13	D6	92	[10]	I; F	I/O	I^2C clock input/output. Open-drain output (for I^2C-bus compliance).
I2C0_SDA	L16	K14	E6	93	[10]	I; F	I/O	I^2C data input/output. Open-drain output (for I^2C-bus compliance).
Reset and wake-up pins								
$\overline{\text{RESET}}$	D9	C7	B6	128	[11]	I; IA	I	External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin does not have an internal pull-up.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC1850/30/20/10 use a multi-layer AHB matrix to connect the ARM Cortex-M3 buses and other bus masters to peripherals. Flexible connections allow different bus masters to access peripherals that are on different slave ports of the matrix simultaneously.

7.2 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and low-power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware division, hardware single-cycle multiply, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

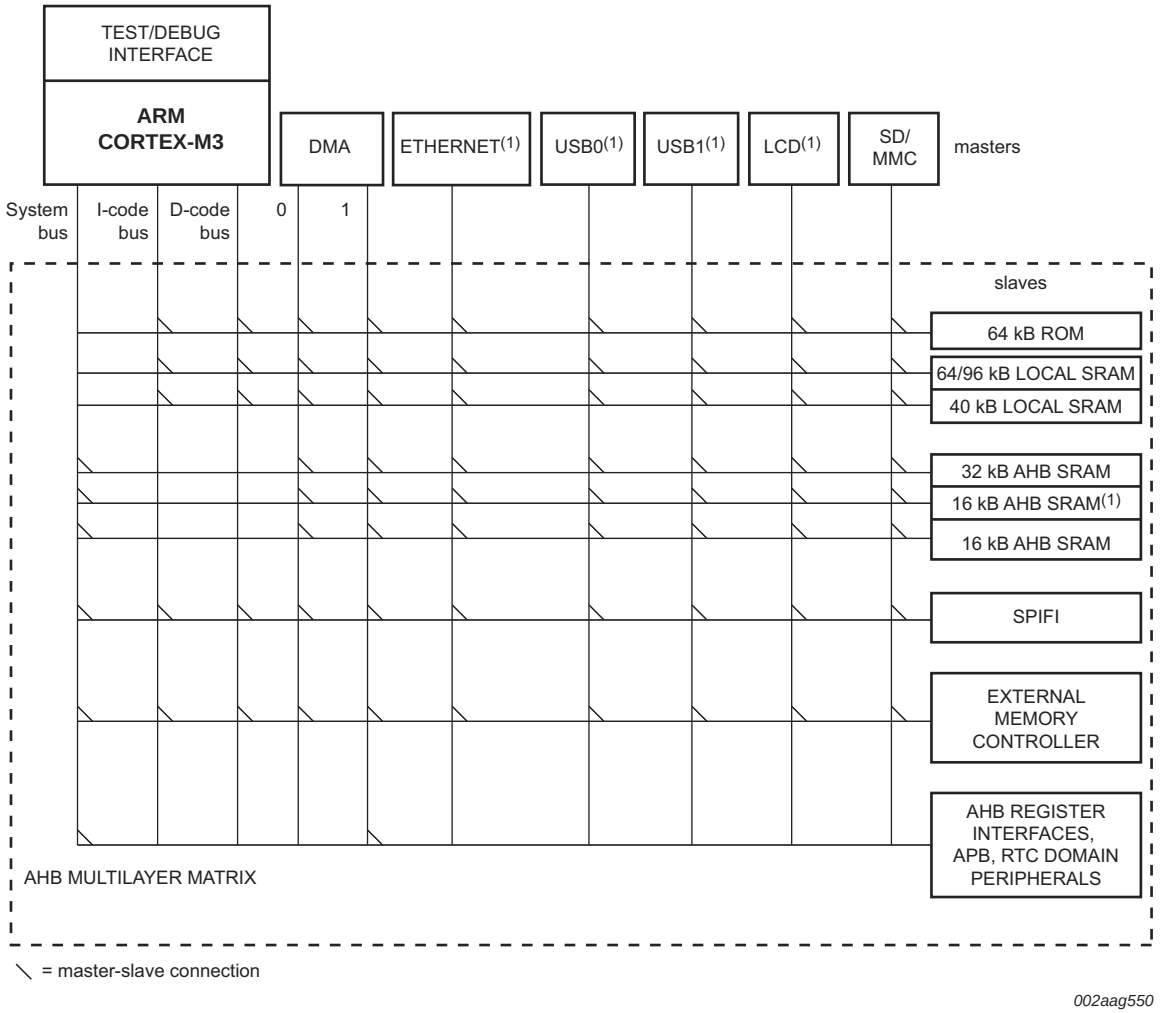
Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the Cortex-M3 Technical Reference Manual.

7.3 System Tick timer (SysTick)

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

7.4 AHB multilayer matrix



(1) Not available on all parts (see Table 2).

Fig 6. AHB multilayer matrix master and slave connections

7.5 Nested Vectored Interrupt Controller (NVIC)

The NVIC is part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC1850/30/20/10, the NVIC supports 53 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.14 Digital serial peripherals

7.14.1 UART

The LPC1850/30/20/10 contain one UART with standard transmit and receive data lines. UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.14.1.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- DMA support.

7.14.2 USART

Remark: The LPC1850/30/20/10 contain three USARTs. In addition to standard transmit and receive data lines, the USARTs support a synchronous mode and a smart card mode.

The USARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.14.2.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit/EIA-485 mode.
- USART3 includes an IrDA mode to support infrared communication.
- All USARTs have DMA support.
- Support for synchronous mode at a data bit rate of up to 8 Mbit/s.

and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.15.3.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position-compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

7.15.4 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer compare function can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.15.4.1 Features

- 32-bit counter. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This mechanism allows for combinations not possible with a simple compare.

7.15.5 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.15.5.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

7.18.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals.

7.18.9 Power control

The LPC1850/30/20/10 feature several independent power domains to control power to the core and the peripherals (see Figure 9). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.

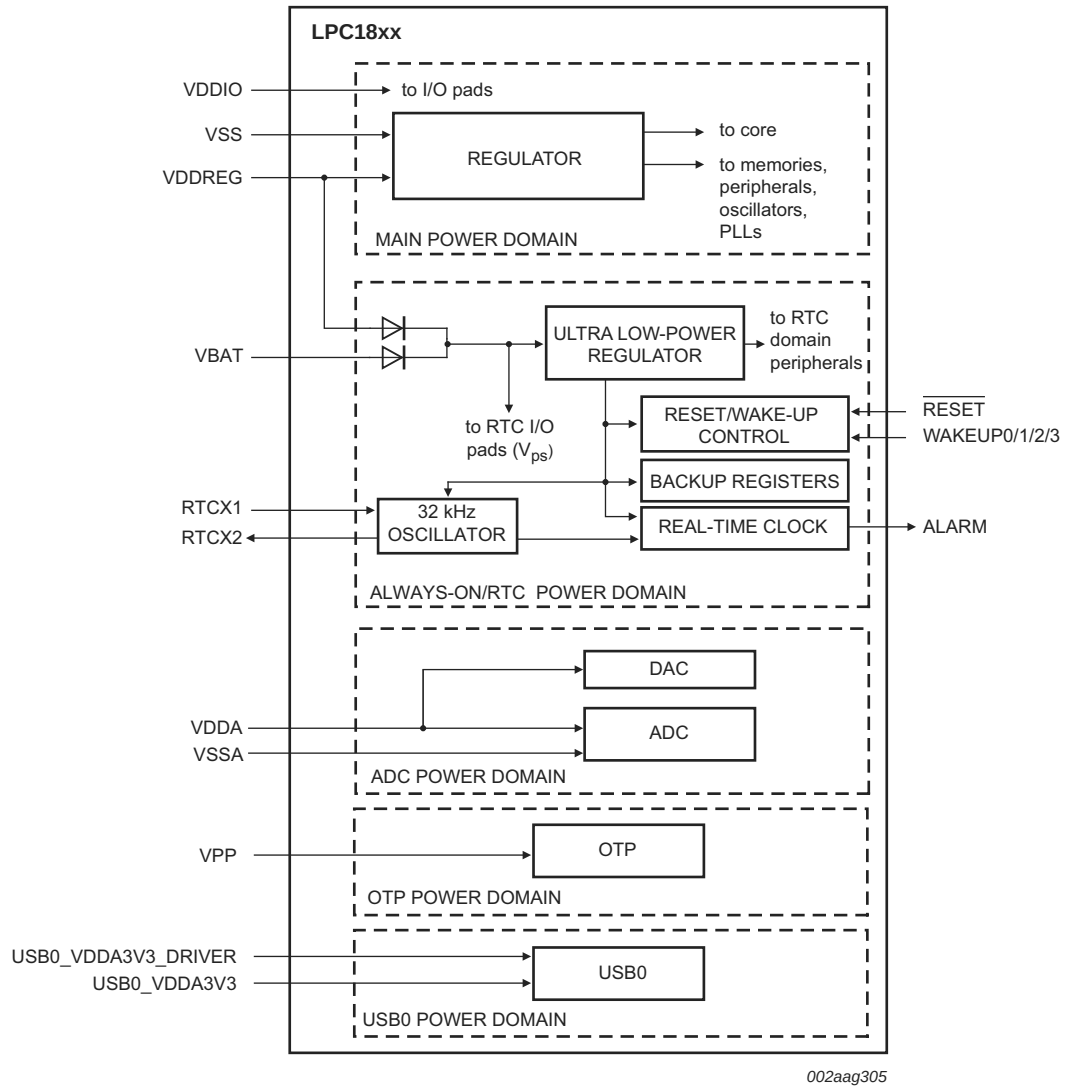


Fig 9. LPC1850/30/20/10 power domains

The LPC1850/30/20/10 support four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.

10.3 BOD characteristics

Table 12. BOD static characteristics[1]

T_{amb} = 25 °C; typical data.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0					
		assertion		-	2.75	-	V
		de-assertion		-	2.92	-	V
		interrupt level 1					
		assertion		-	2.85	-	V
		de-assertion		-	3.00	-	V
		interrupt level 2					
		assertion		-	2.95	-	V
		de-assertion		-	3.12	-	V
		interrupt level 3					
		assertion		-	3.05	-	V
		de-assertion		-	3.19	-	V
		reset level 0					
		assertion		-	1.70	-	V
		de-assertion		-	1.85	-	V
		reset level 1					
		assertion		-	1.80	-	V
		de-assertion		-	1.95	-	V
		reset level 2					
		assertion		-	1.90	-	V
		de-assertion		-	2.05	-	V
		reset level 3					
		assertion		-	2.00	-	V
		de-assertion		-	2.15	-	V

[1] Interrupt and reset levels are selected by writing to the BODLV1/2 bits in the control register CREGE0, see *the LPC18xx user manual*.

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

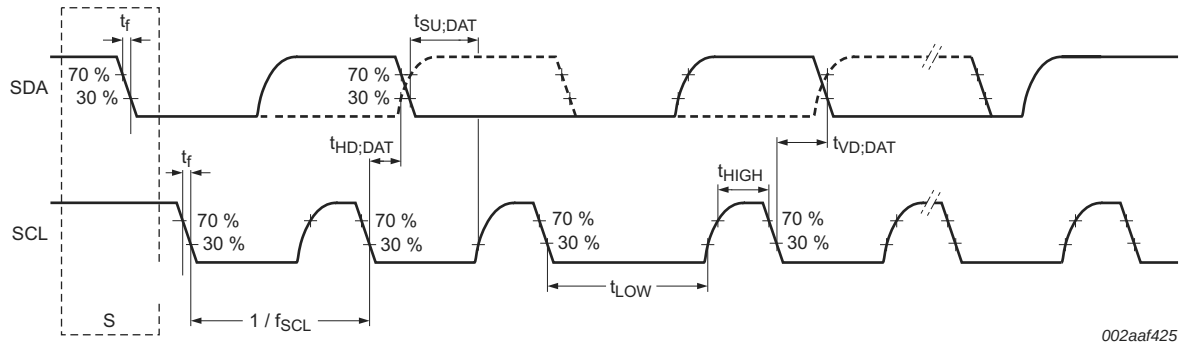


Fig 26. I^2C-bus pins clock timing

11.9 I^2S-bus interface

Table 21. Dynamic characteristics: I^2S-bus interface pins

T_{amb} = 25 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I^2S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I^2S-bus interface PCLK = BASE_APB1_CLK / 12. I^2S clock cycle time $T_{cy(clk)}$ = 79.2 ns; corresponds to the SCK signal in the *I^2S-bus specification*.

12. ADC/DAC electrical characteristics

Table 33. ADC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance			-	-	2	pF
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1][2]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[3]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[4]	-	±0.15	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.15	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[5]	-	±0.3	-	%
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.35	-	%
E_T	absolute error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[6]	-	±3	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±4	-	LSB
R_{vsi}	voltage source interface resistance	see Figure 40		-	-	$1/(7 \times f_{clk(ADC)} \times C_{ia})$	kΩ
R_i	input resistance		[7][8]	-	-	1.2	MΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	4.5	MHz
f_s	sampling frequency	10-bit resolution; 11 clock cycles		-	-	400	kSamples/s
		2-bit resolution; 3 clock cycles				1.5	MSamples/s

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 39.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 39.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 39.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 39.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 39.

[7] T_{amb} = 25 °C.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 2\ k\Omega + 1 / (f_s \times C_{ia})$.

13. Application information

13.1 LCD panel signal usage

Table 35. LCD panel connections for STN single panel mode

External pin	4-bit mono STN single panel		8-bit mono STN single panel		Color STN single panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:8]	-	-	-	-	-	-
LCD_VD7	-	-	P8_4	UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	CDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 36. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:16]	-	-	-	-	-	-
LCD_VD15	-	-	PB_4	LD[7]	PB_4	LD[7]
LCD_VD14	-	-	PB_5	LD[6]	PB_5	LD[6]
LCD_VD13	-	-	PB_6	LD[5]	PB_6	LD[5]
LCD_VD12	-	-	P8_3	LD[4]	P8_3	LD[4]
LCD_VD11	P4_9	LD[3]	P4_9	LD[3]	P4_9	LD[3]
LCD_VD10	P4_10	LD[2]	P4_10	LD[2]	P4_10	LD[2]
LCD_VD9	P4_8	LD[1]	P4_8	LD[1]	P4_8	LD[1]
LCD_VD8	P7_5	LD[0]	P7_5	LD[0]	P7_5	LD[0]
LCD_VD7	-	-		UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]

Table 37. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD0	-	-	-	-	-	-	P4_1	RED0
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB /LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

13.2 Crystal oscillator

The crystal oscillator is controlled by the XTAL_OSC_CTRL register in the CGU (see *LPC18xx user manual*).

The crystal oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL.

The oscillator can operate in one of two modes: slave mode and oscillation mode.

- In slave mode, couple the input clock signal with a capacitor of 100 pF (C_C in Figure 41), with an amplitude of at least 200 mV (RMS). The XTAL2 pin in this configuration can be left unconnected.
- External components and models used in oscillation mode are shown in Figure 42, and in Table 38 and Table 39. Since the feedback resistance is integrated on chip, only a crystal and the capacitances CX1 and CX2 need to be connected externally in case of fundamental mode oscillation (L, CL and RS represent the fundamental frequency). Capacitance C_P in Figure 42 represents the parallel package capacitance and must not be larger than 7 pF. Parameters FC, CL, RS and CP are supplied by the crystal manufacturer.

Table 38. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
2 MHz	< 200 Ω	33 pF, 33 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
4 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
8 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF

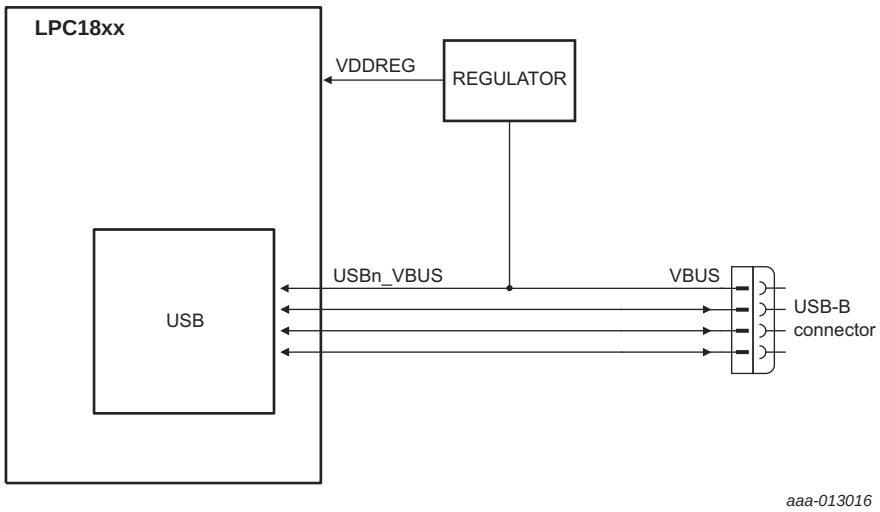


Fig 47. USB interface on a bus-powered device

Remark: If the VBUS function of the USB1 interface is not connected, configure the pin function for GPIO using the function control bits in the SYSCON block.

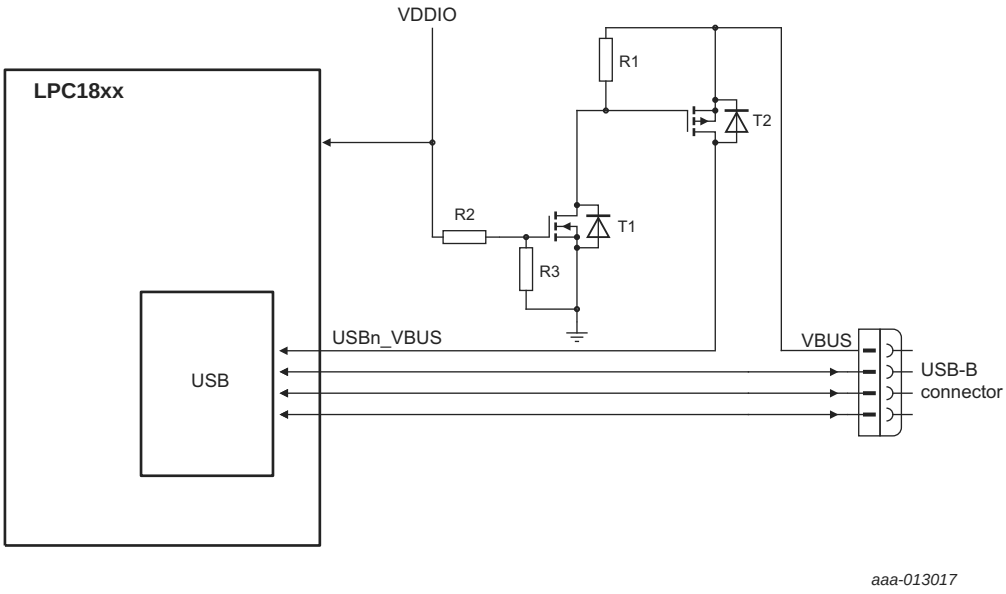


Fig 48. USB interface if the USB operates in OTG mode

Remark: In OTG mode, it is important to be able to detect the VBUS level and to charge and discharge VBUS. This requires adding active devices that disconnect the link when VDDIO is not present.

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