Silicon Labs - EFM32WG360F128G-A-CSP81 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	65
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-UFBGA, CSPBGA
Supplier Device Package	81-CSP (4.35x4.27)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg360f128g-a-csp81

available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

2.1.27 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32WG360 to keep track of time and retain data, even if the main power source should drain out.

2.1.28 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.29 General Purpose Input/Output (GPIO)

In the EFM32WG360, there are 65 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32WG360 is a subset of the feature set described in the EFM32WG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M4	Full configuration	NA
DBG	Full configuration	

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		65	76	µA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		64	75	µA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		65	77	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		65	76	µA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		66	78	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		67	79	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		68	82	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		68	81	µA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		70	83	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		74	87	µA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		76	89	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		106	120	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		112	129	µA/ MHz
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C		0.95[1]	1.7[1]	µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		3.0[1]	4.0[1]	µA
I_{EM3}	EM3 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.65	1.3	µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		2.65	4.0	µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02	0.055	µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.44	0.9	µA

[1]Using backup RTC.

Figure 3.5. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz

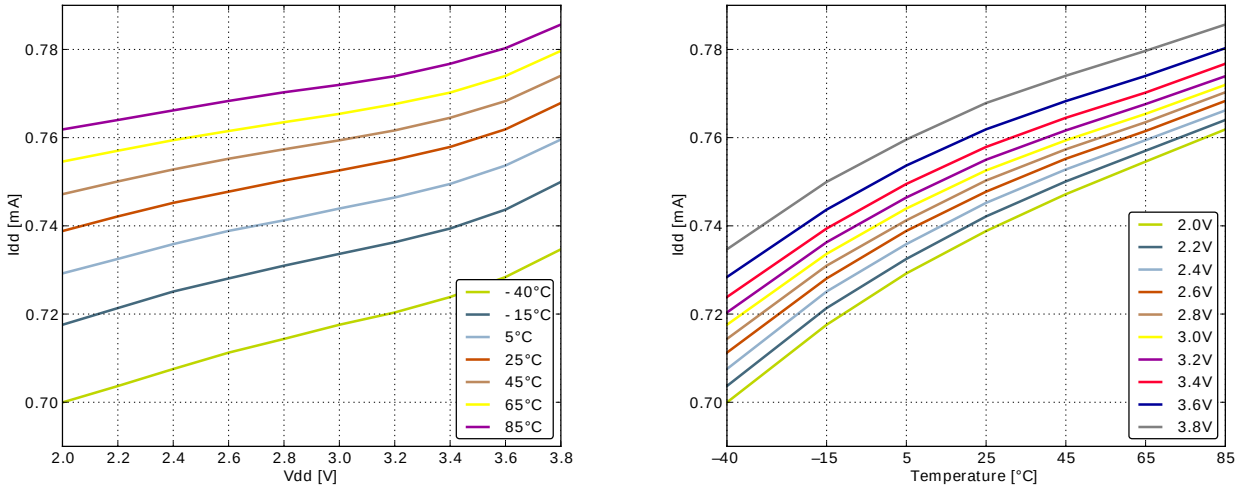


Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz

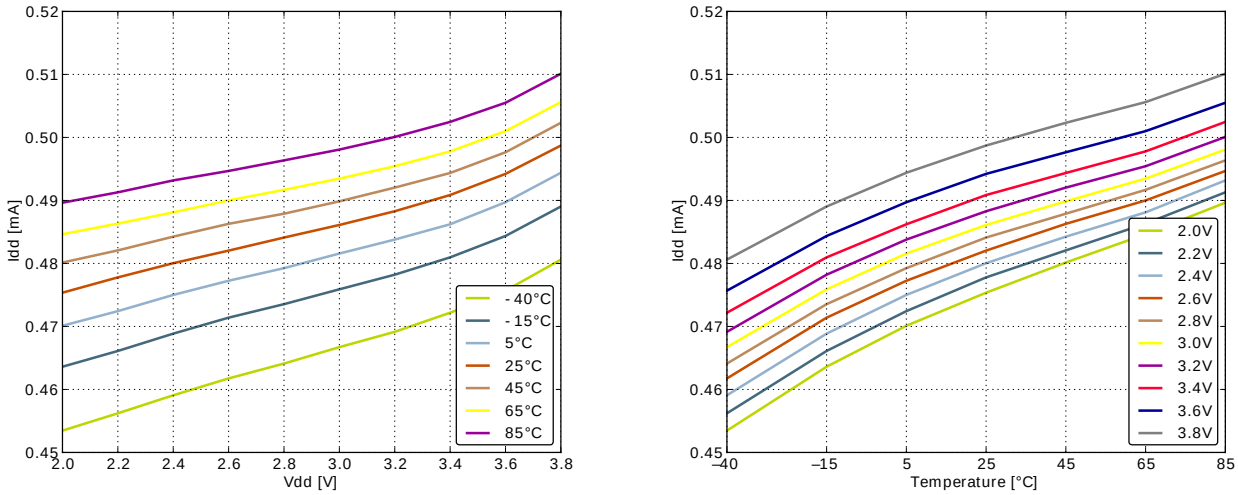
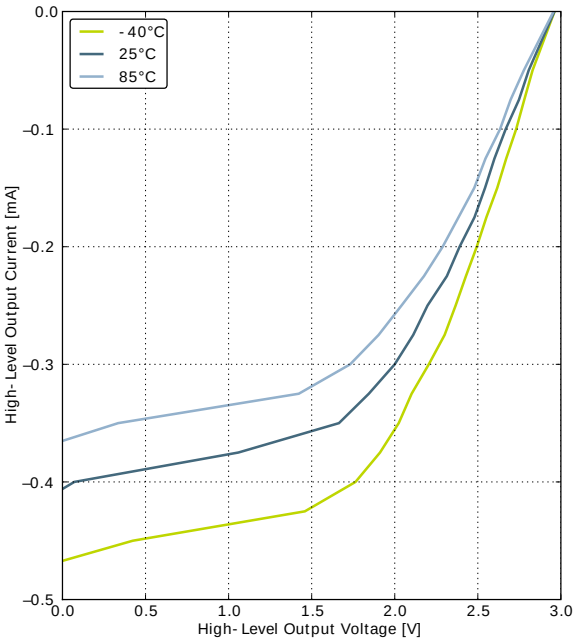
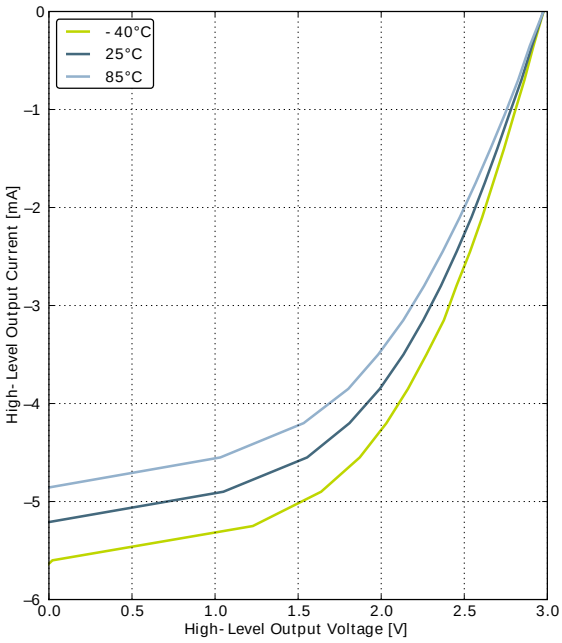


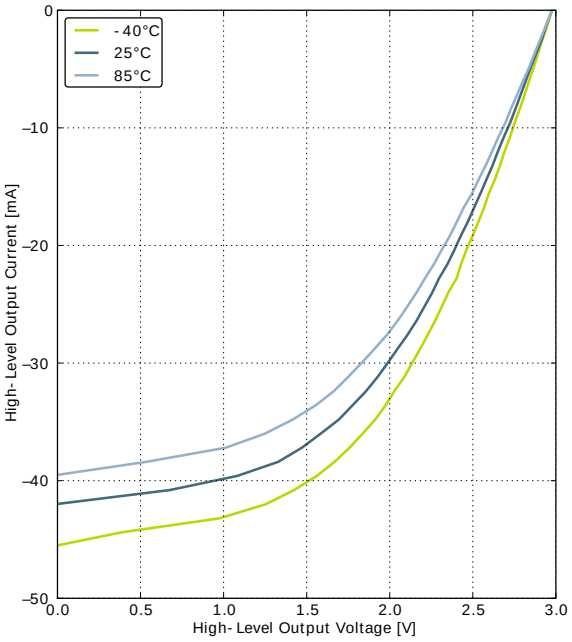
Figure 3.14. Typical High-Level Output Current, 3V Supply Voltage



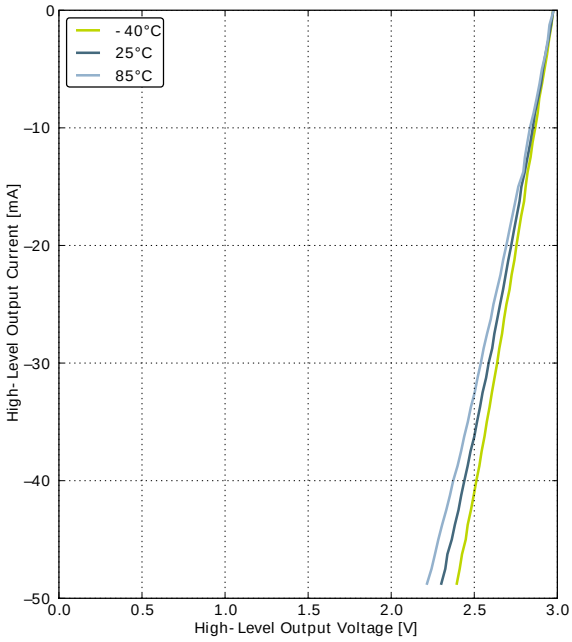
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

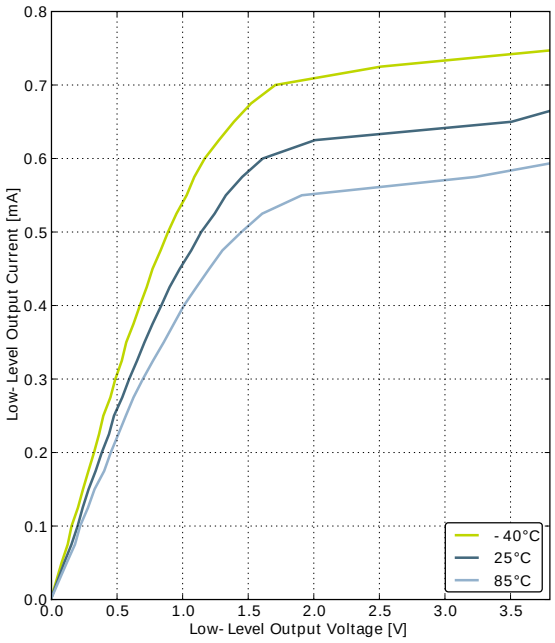


GPIO_Px_CTRL DRIVEMODE = STANDARD

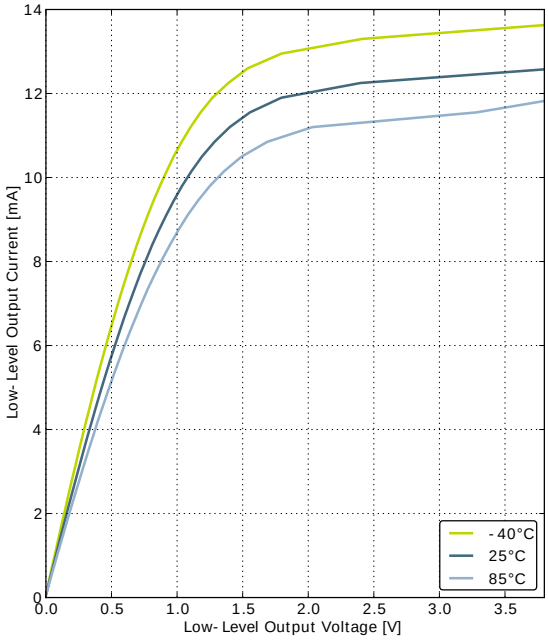


GPIO_Px_CTRL DRIVEMODE = HIGH

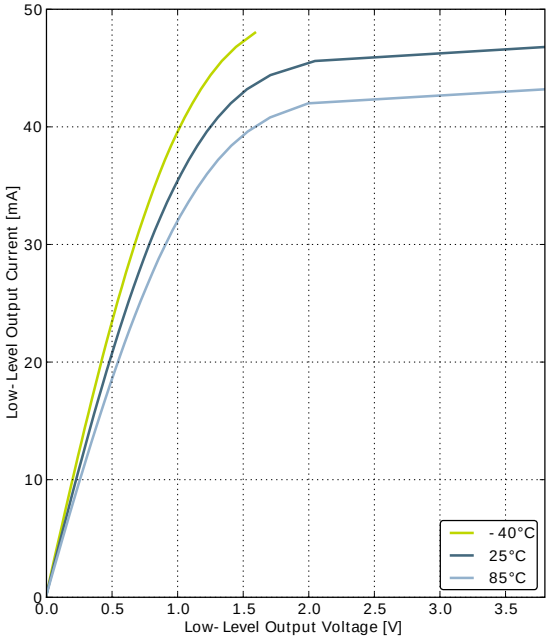
Figure 3.15. Typical Low-Level Output Current, 3.8V Supply Voltage



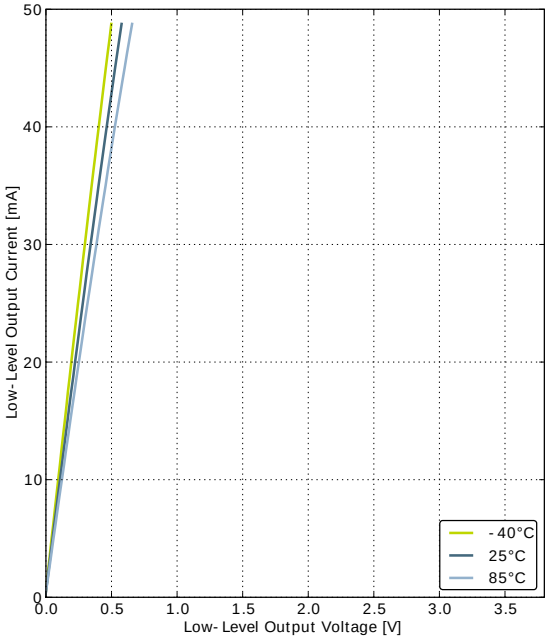
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C		31.29	32.768	34.28	kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			300		nA
$TUNESTEP_{L-FRCO}$	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.17. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

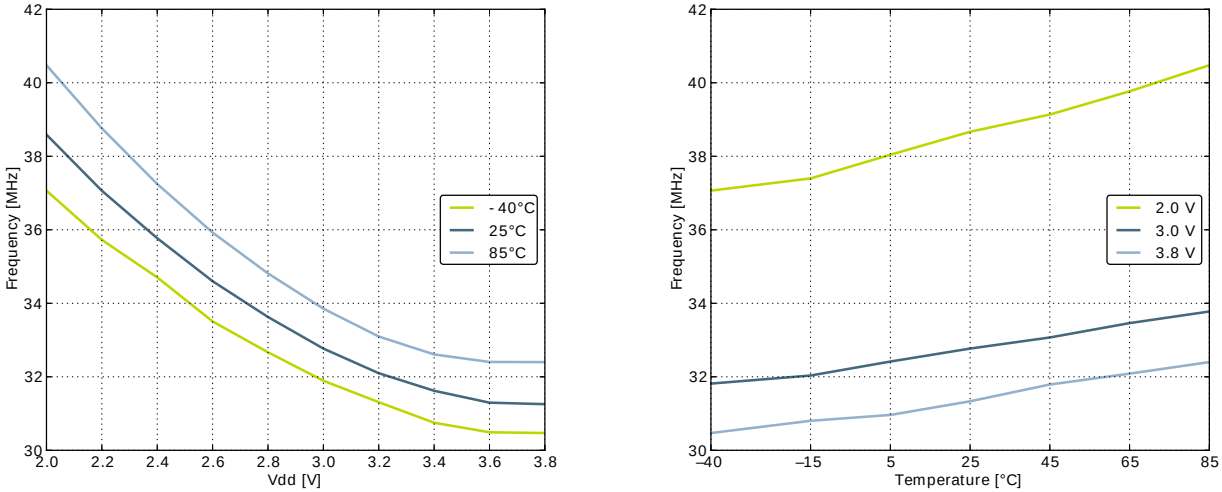
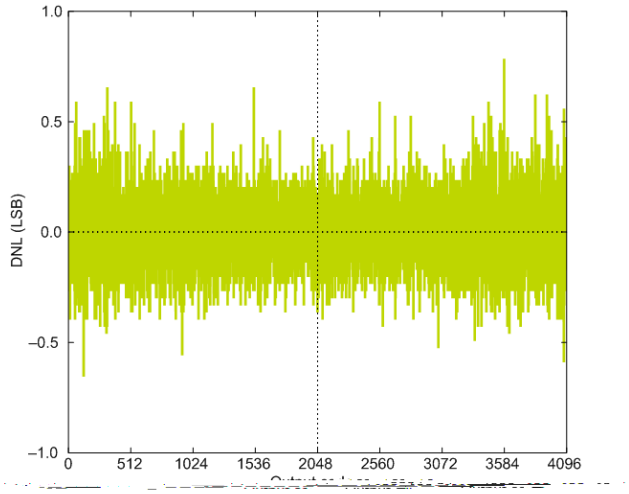
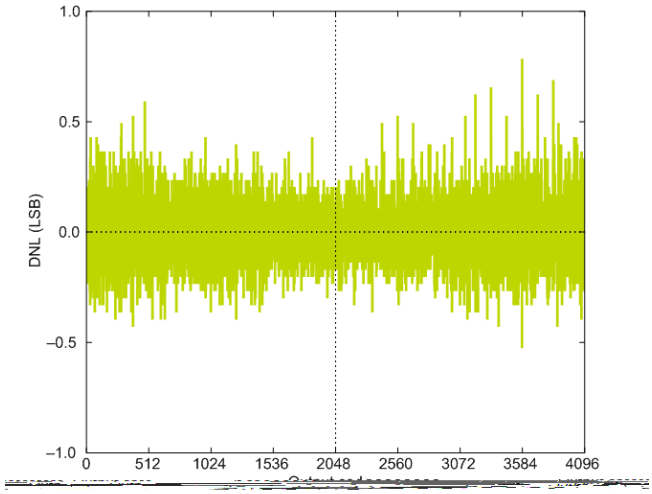


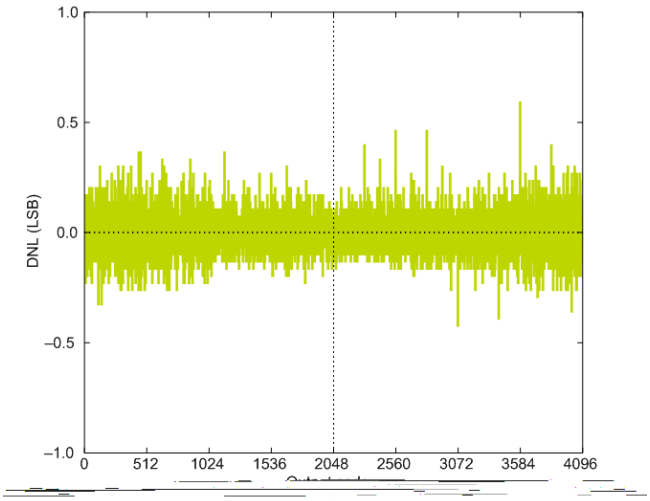
Figure 3.28. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C



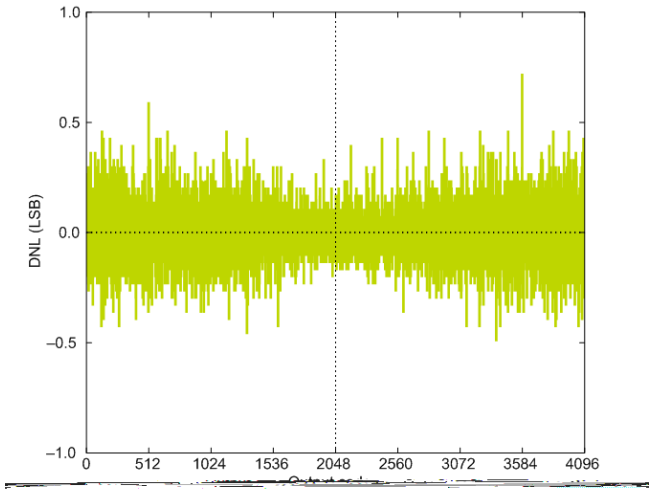
1.25V Reference



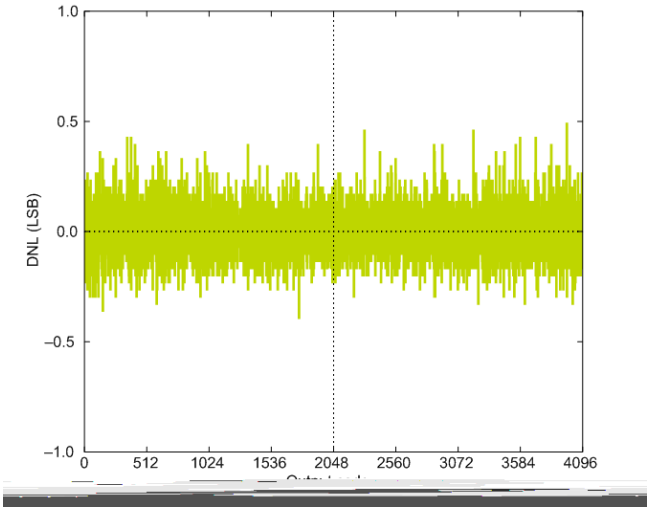
2.5V Reference



2XVDDVSS Reference

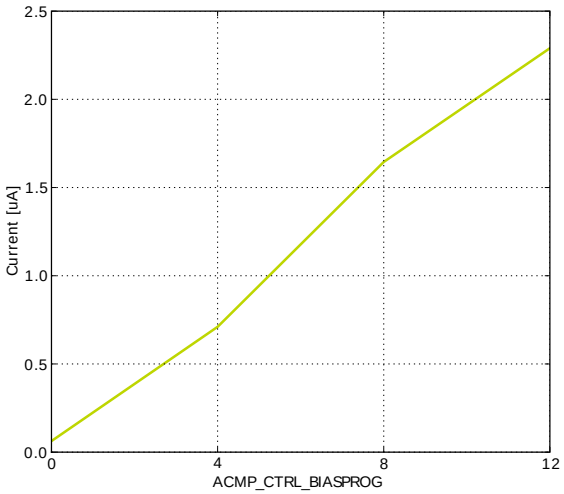


5VDIFF Reference

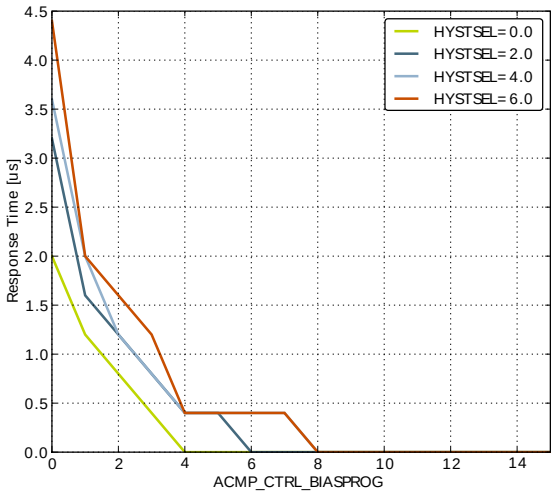


VDD Reference

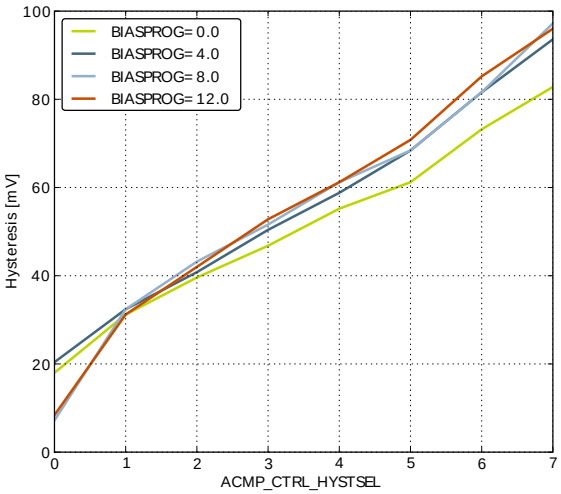
Figure 3.37. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time



Hysteresis

3.14 Voltage Comparator (VCMP)

Table 3.18. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	0.6	µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	35	µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			61	210	mV
$t_{VCMPSTART}$	Startup time				10	µs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

3.15 I2C

Table 3.19. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		100[1]	kHz
t_{LOW}	SCL clock low time	4.7			µs
t_{HIGH}	SCL clock high time	4.0			µs
$t_{SU,DAT}$	SDA set-up time	250			ns
$t_{HD,DAT}$	SDA hold time	8		3450[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	4.7			µs
$t_{HD,STA}$	(Repeated) START condition hold time	4.0			µs
$t_{SU,STO}$	STOP condition set-up time	4.0			µs
t_{BUF}	Bus free time between a STOP and a START condition	4.7			µs

[1]For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32WG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

3.16 USART SPI

Figure 3.38. SPI Master Timing

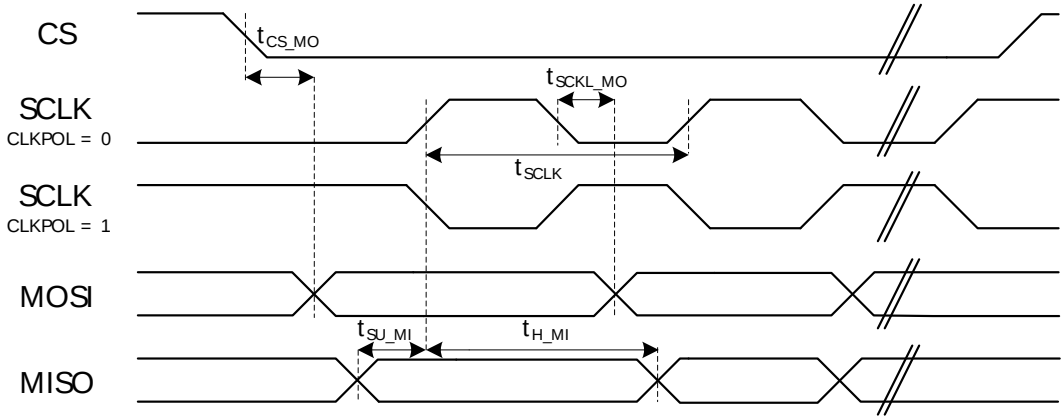


Table 3.22. SPI Master Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1] [2]	SCLK period		2 * $t_{HFPER-CLK}$			ns
t_{CS_MO} [1] [2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1] [2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1] [2]	MISO setup time	IOVDD = 3.0 V	36.00			ns
t_{H_MI} [1] [2]	MISO hold time		-6.00			ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Table 3.23. SPI Master Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1] [2]	SCLK period		2 * $t_{HFPER-CLK}$			ns
t_{CS_MO} [1] [2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1] [2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1] [2]	MISO setup time	IOVDD = 3.0 V	-32.00			ns
t_{H_MI} [1] [2]	MISO hold time		63.00			ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCLK_MI} [1][2]	SCLK to MISO	-264 + $t_{HF-PERCLK}$		-234 + 2 * $t_{HFPERCLK}$	ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

3.17 Digital Peripherals

Table 3.26. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		4.0		µA/MHz
I_{UART}	UART current	UART idle current, clock enabled		3.8		µA/MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		194.0		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		7.6		µA/MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		6.5		µA/MHz
$I_{LETIMER}$	LETIMER current	LETIMER idle current, clock enabled		85.8		nA
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		91.4		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		54.6		nA
I_{AES}	AES current	AES idle current, clock enabled		1.8		µA/MHz
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		3.4		µA/MHz
I_{PRS}	PRS current	PRS idle current		3.9		µA/MHz
I_{DMA}	DMA current	Clock enable		10.9		µA/MHz

CSP81 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
					DBG_SWO #0 GPIO_EM4WU4
A4	VSS	Ground			
A5	IOVDD_5	Digital IO power supply 5.			
A6	PE9		PCNT2_S1IN #1		
A7	PE11		TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
A8	PE12		TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
A9	PA15		TIM3_CC2 #0		
B1	USB_VREGI				
B2	USB_VBUS	USB 5.0 V VBUS input.			
B3	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT	TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
B4	PF1		TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
B5	PF5		TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
B6	PE8		PCNT2_S0IN #1		PRS_CH3 #1
B7	PE13			US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
B8	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
B9	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
C1	USB_VREGO				
C2	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT	TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0
C3	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
C4	PF0		TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
C5	PF12			USB_ID	
C6	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
C7	PE14		TIM3_CC0 #0	LEU0_TX #2	
C8	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
C9	PA3		TIM0_CDTI0 #0	U0_TX #2	LES_ALTEX2 #0 ETM_TD1 #3
D1	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
D2	PC11	ACMP1_CH3		US0_TX #2	LES_CH11 #0
D3	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT		U1_TX #0	CMU_CLK0 #1 LES_CH12 #0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32WG360 is shown in Table 4.3 (p. 62). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	-	-	-	-	PA10	PA9	PA8	-	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	PB12	PB11	-	-	PB8	PB7	PB6	PB5	PB4	PB3	-	-	-
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	-	-	-	-	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	-	-	PE5	PE4	PE3	PE2	-	-
Port F	-	-	-	PF12	PF11	PF10	-	-	-	-	PF5	-	-	PF2	PF1	PF0

4.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG360 is shown in Figure 4.2 (p. 62) .

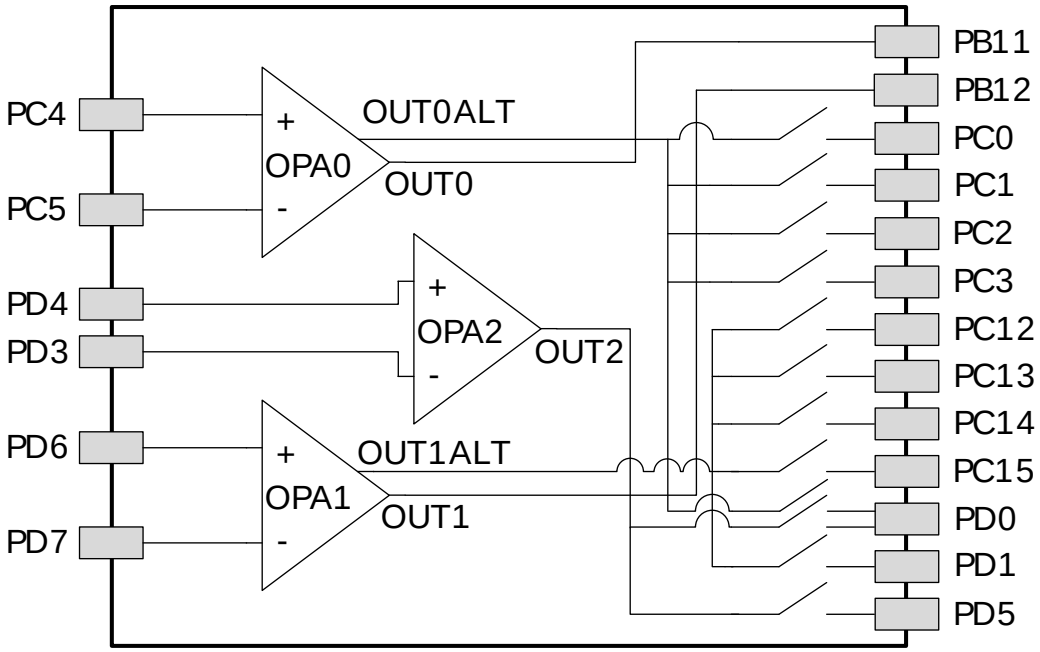



Figure 4.2. Opamp Pinout