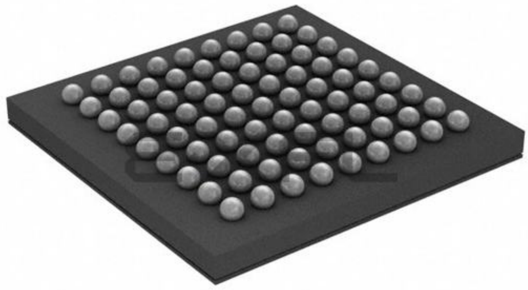

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 65 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 81-UFBGA, CSPBGA |
| Supplier Device Package | 81-CSP (4.35x4.27) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32wg360f128g-a-csp81r |

### 2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32WG microcontroller. The flash memory is readable and writable from both the Cortex-M4 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

### 2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32WG.

### 2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32WG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

### 2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32WG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

### 2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

### 2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 2.1.10 Universal Serial Bus Controller (USB)

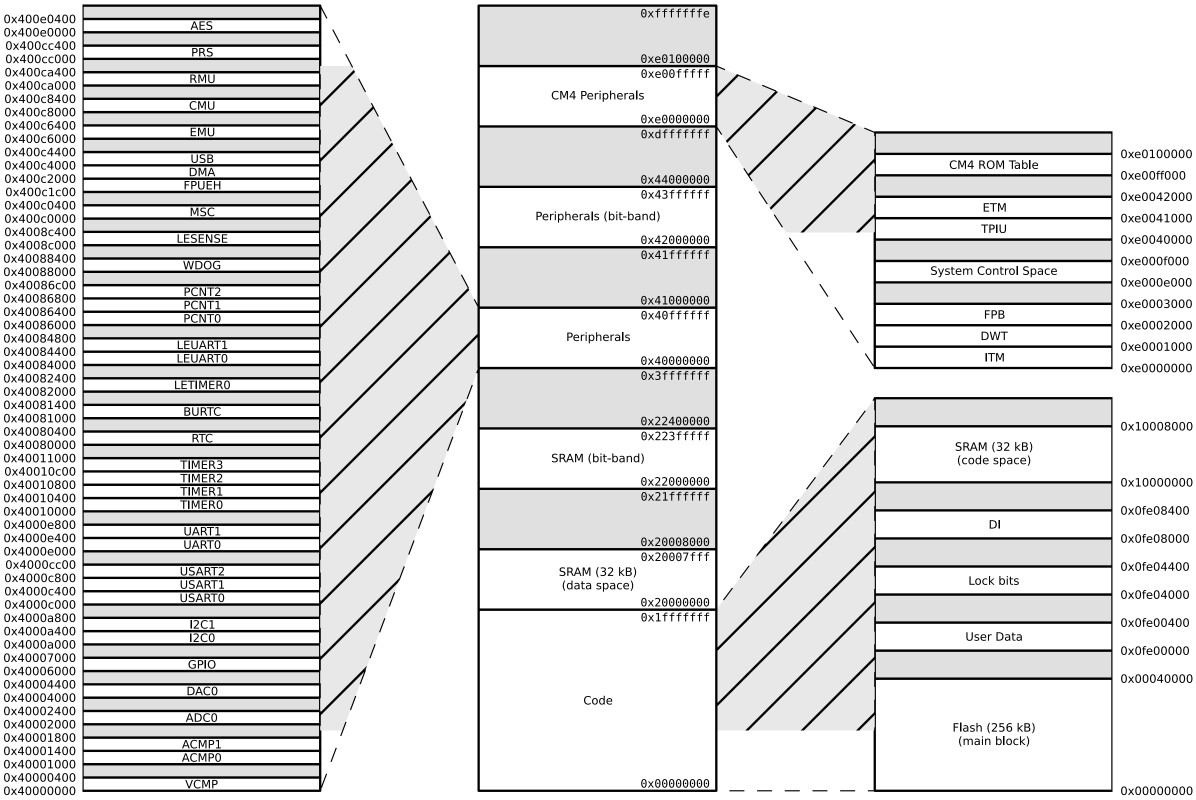
The USB is a full-speed USB 2.0 compliant OTG host/device controller. The USB can be used in Device, On-the-go (OTG) Dual Role Device or Host-only configuration. In OTG mode the USB supports both Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation. The USB device includes an internal dedicated Descriptor-Based Scatter/Garther DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes all OTG features, except for the voltage booster for supplying 5V to VBUS when operating as host.

| Module | Configuration | Pin Connections |
|---|---|---|
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 65 pins | Available pins are shown in Table 4.3 (p. 62) |

## 2.3 Memory Map

The *EFM32WG360* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

*Figure 2.2. EFM32WG360 Memory Map with largest RAM and Flash sizes*



| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 65 | 76 | µA/ MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 64 | 75 | µA/ MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 65 | 77 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 65 | 76 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 66 | 78 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 67 | 79 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 68 | 82 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 68 | 81 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 70 | 83 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 74 | 87 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 76 | 89 | µA/ MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 106 | 120 | µA/ MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 112 | 129 | µA/ MHz |
| $I_{EM2}$ | EM2 current | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.95[1] | 1.7[1] | µA |
| | | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 3.0[1] | 4.0[1] | µA |
| $I_{EM3}$ | EM3 current | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.65 | 1.3 | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 2.65 | 4.0 | µA |
| $I_{EM4}$ | EM4 current | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.02 | 0.055 | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 0.44 | 0.9 | µA |

[1]Using backup RTC.

## 3.4.1 EM1 Current Consumption

***Figure 3.1. EM1 Current consumption with all peripheral clocks disabled and HFXO running at 48 MHz***

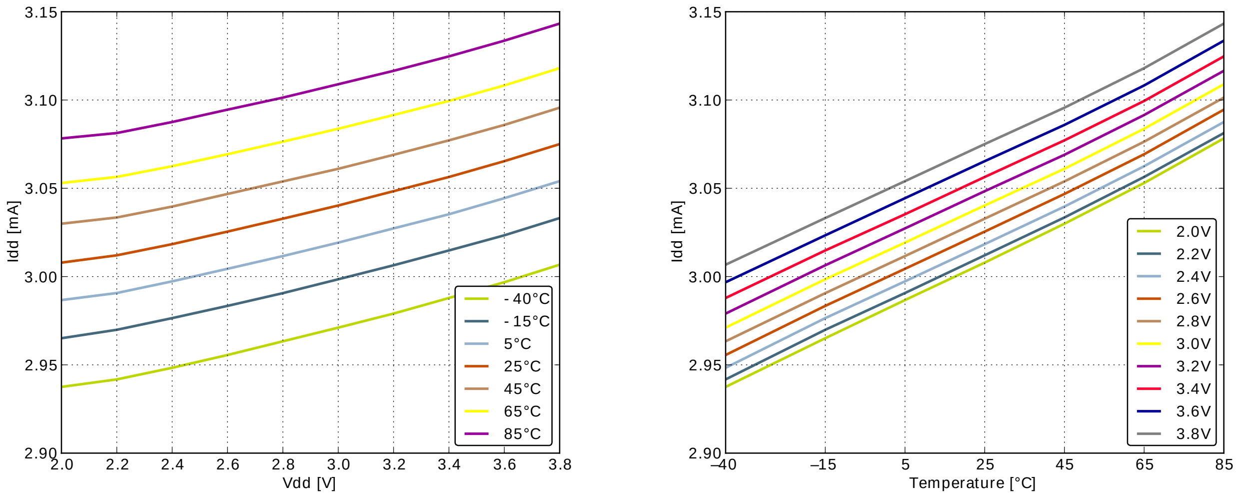
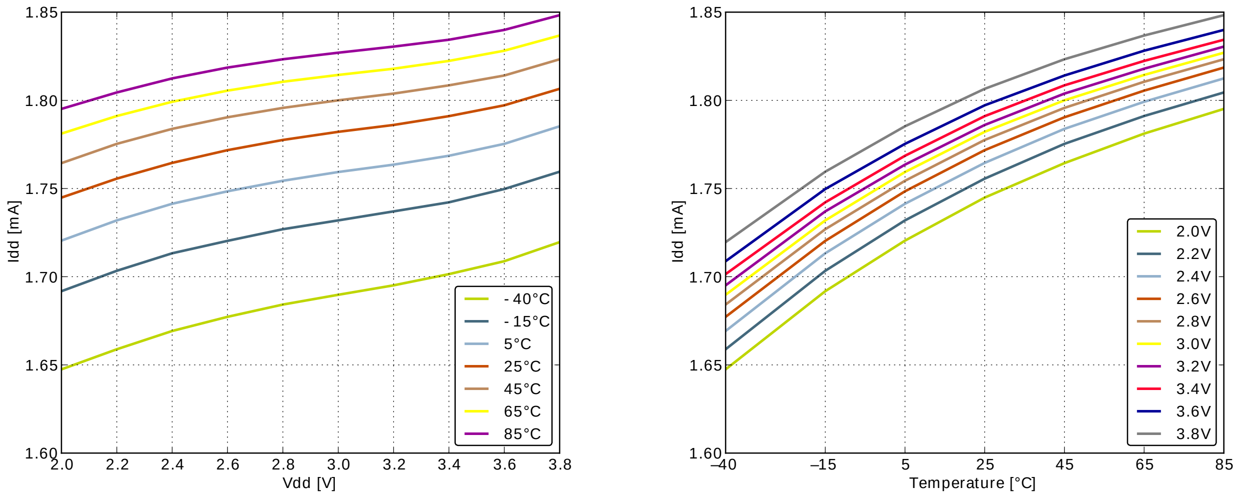



***Figure 3.2. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 28 MHz***



## 3.6 Power Management

The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

***Table 3.5. Power Management***

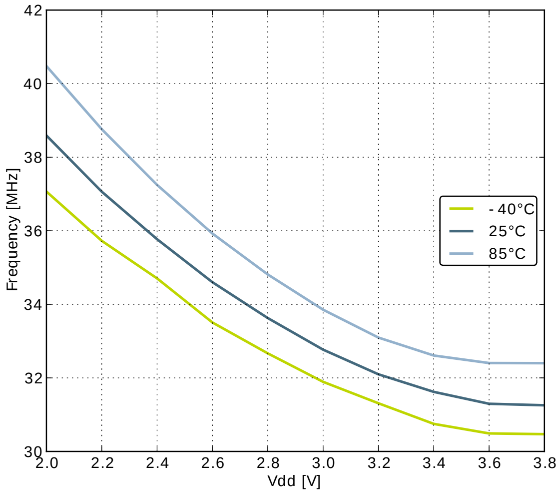
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | | 1.74 | | 1.96 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | 1.98 | V |
| $V_{PORthr+}$ | Power-on Reset (POR) threshold on rising external supply voltage | | | | 1.98 | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGO}$ | USB voltage regulator out decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGO pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGI}$ | USB voltage regulator in decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGI pin and GROUND | | 4.7 | | µF |

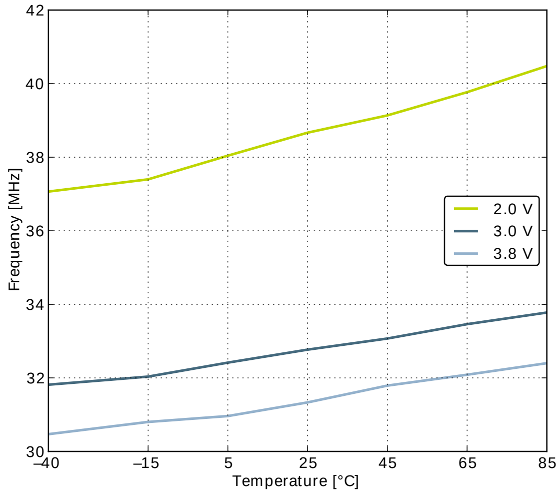
## 3.9.3 LFRCO

*Table 3.10. LFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFRCO}$ | Oscillation frequency , $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 31.29 | 32.768 | 34.28 | kHz |
| $t_{LFRCO}$ | Startup time not including software calibration | | | 150 | | µs |
| $I_{LFRCO}$ | Current consumption | | | 300 | | nA |
| $TUNESTEP_{LFRCO}$ | Frequency step for LSB change in TUNING value | | | 1.5 | | % |

*Figure 3.17. Calibrated LFRCO Frequency vs Temperature and Supply Voltage*



| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 78 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 68 | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 79 | | dBc |
| $V_{ADCOFFSET}$ | Offset voltage | After calibration, single ended | -3.5 | 0.3 | 3 | mV |
| | | After calibration, differential | | 0.3 | | mV |
| $TGRAD_{ADCTH}$ | Thermometer output gradient | | | -1.92 | | mV/°C |
| | | | | -6.3 | | ADC Codes/°C |
| $DNL_{ADC}$ | Differential non-linearity (DNL) | | -1 | ±0.7 | 4 | LSB |
| $INL_{ADC}$ | Integral non-linearity (INL), End point method | | | ±1.2 | ±3 | LSB |
| $MC_{ADC}$ | No missing codes | | 11.999[1] | 12 | | bits |
| $GAIN_{ED}$ | Gain error drift | 1.25V reference | | 0.01[2] | 0.033[3] | %/°C |
| | | 2.5V reference | | 0.01[2] | 0.03[3] | %/°C |
| $OFFSET_{ED}$ | Offset error drift | 1.25V reference | | 0.2[2] | 0.7[3] | LSB/°C |
| | | 2.5V reference | | 0.2[2] | 0.62[3] | LSB/°C |

[1]On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.
[2]Typical numbers given by abs(Mean) / (85 - 25).
[3]Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.24 (p. 37) and Figure 3.25 (p. 37) , respectively.

***Figure 3.24. Integral Non-Linearity (INL)***

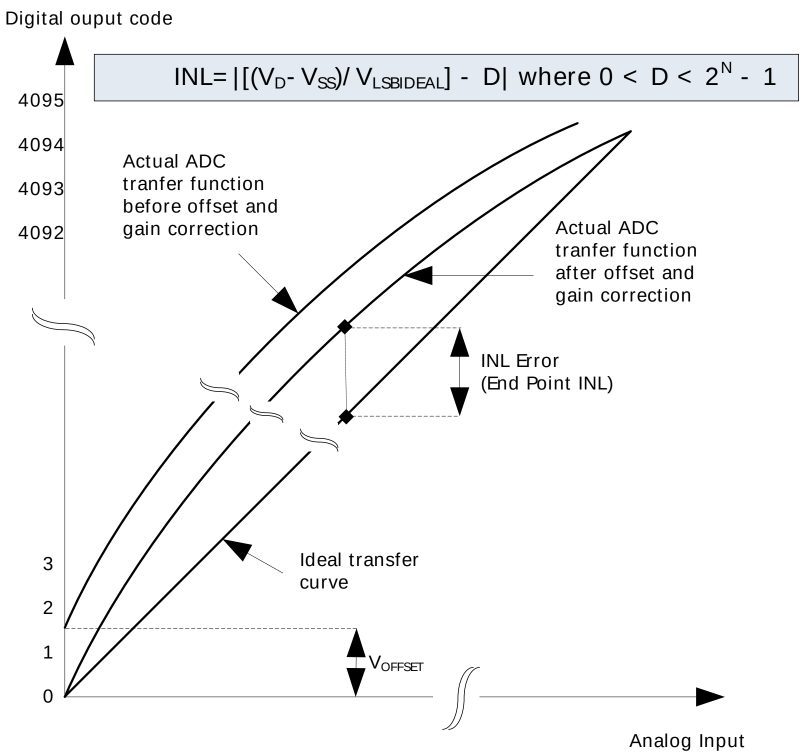
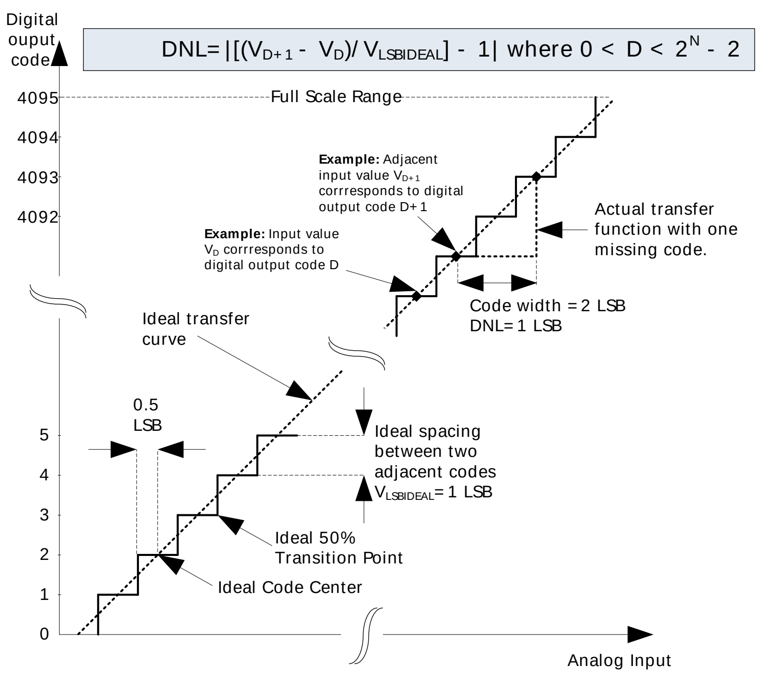
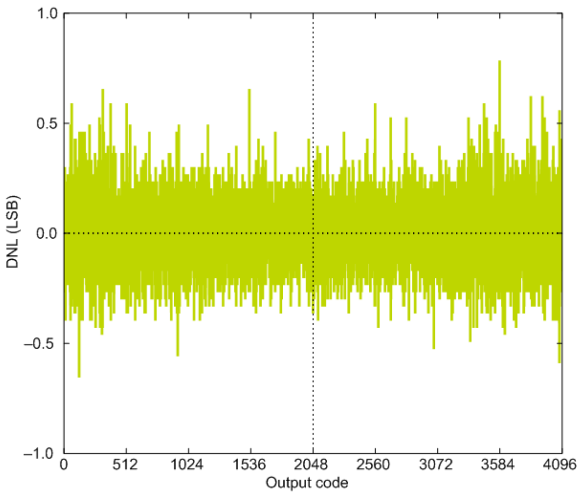


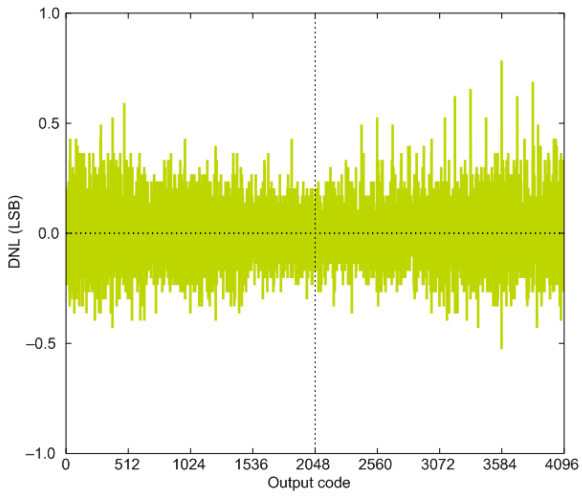

***Figure 3.25. Differential Non-Linearity (DNL)***



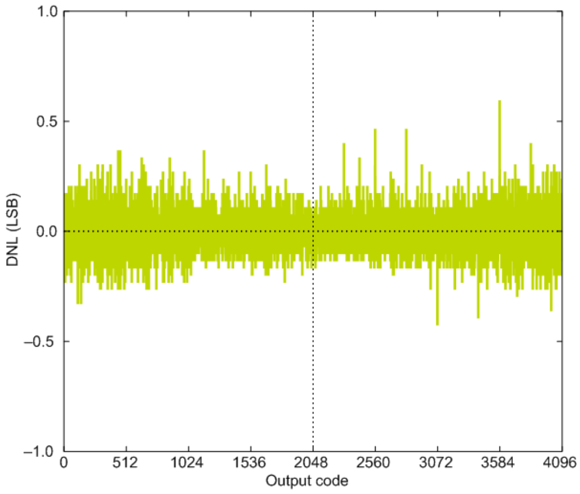
### *Figure 3.28. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C*



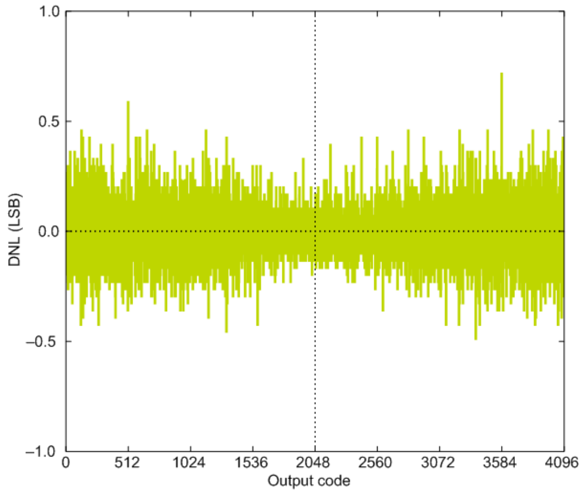

1.25V Reference



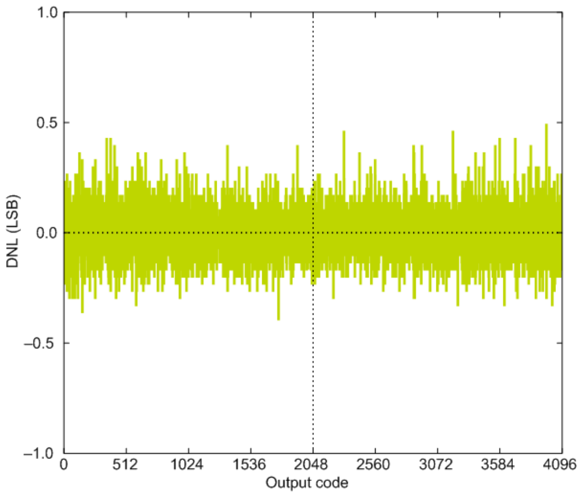

2.5V Reference




2XVDDVSS Reference

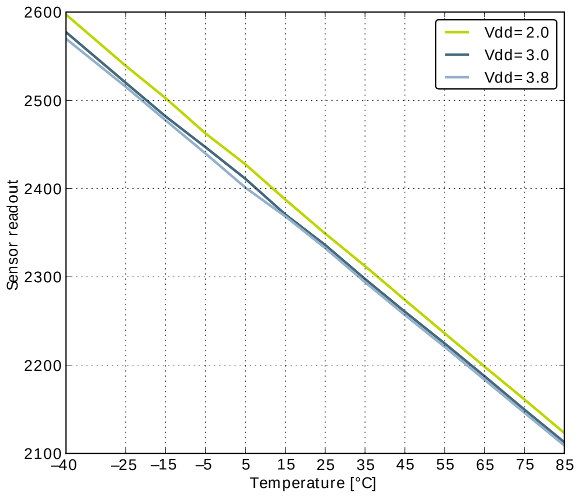



5VDIFF Reference




VDD Reference

**Figure 3.31. ADC Temperature sensor readout**




# 3.11 Digital Analog Converter (DAC)

**Table 3.15. DAC**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DACOUT}$ | Output voltage range | VDD voltage reference, single ended | 0 | | $V_{DD}$ | V |
| | | VDD voltage reference, differential | $-V_{DD}$ | | $V_{DD}$ | V |
| $V_{DACCM}$ | Output common mode voltage range | | 0 | | $V_{DD}$ | V |
| $I_{DAC}$ | Active current including references for 2 channels | 500 kSamples/s, 12 bit | | 400[1] | | µA |
| | | 100 kSamples/s, 12 bit | | 200[1] | | µA |
| | | 1 kSamples/s 12 bit NORMAL | | 17[1] | | µA |
| $SR_{DAC}$ | Sample rate | | | | 500 | ksamples/s |
| $f_{DAC}$ | DAC clock frequency | Continuous Mode | | | 1000 | kHz |
| | | Sample/Hold Mode | | | 250 | kHz |
| | | Sample/Off Mode | | | 250 | kHz |
| $CYC_{DACCONV}$ | Clock cyckles per conversion | | | 2 | | |
| $t_{DACCONV}$ | Conversion time | | 2 | | | µs |
| $t_{DACSETTLE}$ | Settling time | | | 5 | | µs |
| $SNR_{DAC}$ | Signal to Noise Ratio (SNR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 58 | | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 59 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 58 | | dB |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain | | 13 | 25 | µA |
| $G_{OL}$ | Open Loop Gain | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 101 | | dB |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 98 | | dB |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 91 | | dB |
| $GBW_{OPAMP}$ | Gain Bandwidth Product | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 6.1 | | MHz |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 1.8 | | MHz |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.25 | | MHz |
| $PM_{OPAMP}$ | Phase Margin | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, $C_L$=75 pF | | 64 | | ° |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| $R_{INPUT}$ | Input Resistance | | | 100 | | Mohm |
| $R_{LOAD}$ | Load Resistance | | 200 | | | Ohm |
| $I_{LOAD\_DC}$ | DC Load Current | | | | 11 | mA |
| $V_{INPUT}$ | Input Voltage | OPAxHCMDIS=0 | $V_{SS}$ | | $V_{DD}$ | V |
| | | OPAxHCMDIS=1 | $V_{SS}$ | | $V_{DD}$-1.2 | V |
| $V_{OUTPUT}$ | Output Voltage | | $V_{SS}$ | | $V_{DD}$ | V |
| $V_{OFFSET}$ | Input Offset Voltage | Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$, OPAxHCMDIS=0 | | 0 | | mV |
| | | Unity Gain, $V_{SS}$<$V_{in}$<$_{DD}$-1.2, OPAxHCMDIS=1 | | 1 | | mV |
| $V_{OFFSET\_DRIFT}$ | Input Offset Voltage Drift | | | | 0.02 | mV/°C |
| $SR_{OPAMP}$ | Slew Rate | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 3.2 | | V/µs |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 0.8 | | V/µs |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.1 | | V/µs |
| $N_{OPAMP}$ | Voltage Noise | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=0 | | 101 | | $µV_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=1 | | 141 | | $µV_{RMS}$ |

## 3.13 Analog Comparator (ACMP)

***Table 3.17. ACMP***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ACMPIN}$ | Input voltage range | | 0 | | $V_{DD}$ | V |
| $V_{ACMPCM}$ | ACMP Common Mode voltage range | | 0 | | $V_{DD}$ | V |
| $I_{ACMP}$ | Active current | BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register | | 0.1 | 0.4 | µA |
| | | BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | | 2.87 | 15 | µA |
| | | BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register | | 195 | 520 | µA |
| $I_{ACMPREF}$ | Current consumption of internal voltage reference | Internal voltage reference off. Using external voltage reference | | 0 | | µA |
| | | Internal voltage reference | | 5 | | µA |
| $V_{ACMPOFFSET}$ | Offset voltage | BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | -12 | 0 | 12 | mV |
| $V_{ACMPHYST}$ | ACMP hysteresis | Programmable | | 17 | | mV |
| $R_{CSRES}$ | Capacitive Sense Internal Resistance | CSRESSEL=0b00 in ACMPn_INPUTSEL | | 39 | | kOhm |
| | | CSRESSEL=0b01 in ACMPn_INPUTSEL | | 71 | | kOhm |
| | | CSRESSEL=0b10 in ACMPn_INPUTSEL | | 104 | | kOhm |
| | | CSRESSEL=0b11 in ACMPn_INPUTSEL | | 136 | | kOhm |
| $t_{ACMPSTART}$ | Startup time | | | | 10 | µs |

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 47) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

***Total ACMP Active Current***

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

# 4 Pinout and Package

**Note**

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32WG360.

## 4.1 Pinout

The *EFM32WG360* pinout is shown in Figure 4.1 (p. 54) and Table 4.1 (p. 54). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

***Figure 4.1. EFM32WG360 Pinout (top view, not to scale)***

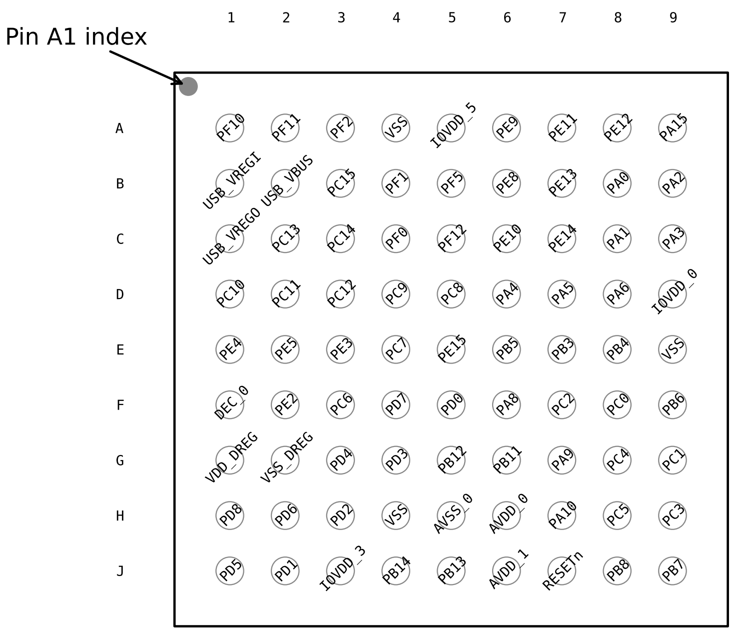



***Table 4.1. Device Pinout***

| CSP81 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| A1 | PF10 | | | U1_TX #1<br>USB_DM | |
| A2 | PF11 | | | U1_RX #1<br>USB_DP | |
| A3 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 |

| CSP81 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| D4 | PC9 | ACMP1_CH1 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| D5 | PC8 | ACMP1_CH0 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| D6 | PA4 | | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| D7 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| D8 | PA6 | | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| D9 | IOVDD_0 | Digital IO power supply 0. | | | |
| E1 | PE4 | | | US0_CS #1 | |
| E2 | PE5 | | | US0_CLK #1 | |
| E3 | PE3 | BU_STAT | | U1_RX #3 | ACMP1_O #1 |
| E4 | PC7 | ACMP0_CH7 | | LEU1_RX #0<br>I2C0_SCL #2 | LES_CH7 #0<br>ETM_TD0 #2 |
| E5 | PE15 | | TIM3_CC1 #0 | LEU0_RX #2 | |
| E6 | PB5 | | | US2_CLK #1 | |
| E7 | PB3 | | PCNT1_S0IN #1 | US2_TX #1 | |
| E8 | PB4 | | PCNT1_S1IN #1 | US2_RX #1 | |
| E9 | VSS | Ground | | | |
| F1 | DEC_0 | Decouple output for on-chip voltage regulator. | | | |
| F2 | PE2 | BU_VOUT | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| F3 | PC6 | ACMP0_CH6 | | LEU1_TX #0<br>I2C0_SDA #2 | LES_CH6 #0<br>ETM_TCLK #2 |
| F4 | PD7 | ADC0_CH7<br>DAC0_N1 /<br>OPAMP_N1 | TIM1_CC1 #4<br>LETIM0_OUT1 #0<br>PCNT0_S1IN #3 | US1_TX #2<br>I2C0_SCL #1 | CMU_CLK0 #2<br>LES_ALTEX1 #0<br>ACMP1_O #2<br>ETM_TCLK #0 |
| F5 | PD0 | ADC0_CH0<br>DAC0_OUT0ALT #4/<br>OPAMP_OUT0ALT<br>OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |
| F6 | PA8 | | TIM2_CC0 #0 | | |
| F7 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| F8 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| F9 | PB6 | | | US2_CS #1 | |
| G1 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| G2 | VSS_DREG | Ground for on-chip voltage regulator. | | | |
| G3 | PD4 | ADC0_CH4<br>OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| G4 | PD3 | ADC0_CH3<br>OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| G5 | PB12 | DAC0_OUT1 /<br>OPAMP_OUT1 | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| G6 | PB11 | DAC0_OUT0 / | TIM1_CC2 #3 | I2C1_SDA #1 | |

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

### Table 4.2. Alternate functionality overview

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX |
| BOOT_TX | PE10 | | | | | | | Bootloader TX |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N0 / OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| DAC0_N1 / OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM0_CDTI0 | PA3 | PC13 | | PC13 | PC2 | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | | PC14 | PC3 | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | | | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | | | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | PF11 | | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | PF10 | | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br><br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br><br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br><br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br><br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br><br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br><br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |

# 5 PCB Layout and Soldering

## 5.1 Recommended PCB Layout

*Figure 5.1. CSP81 PCB Land Pattern*

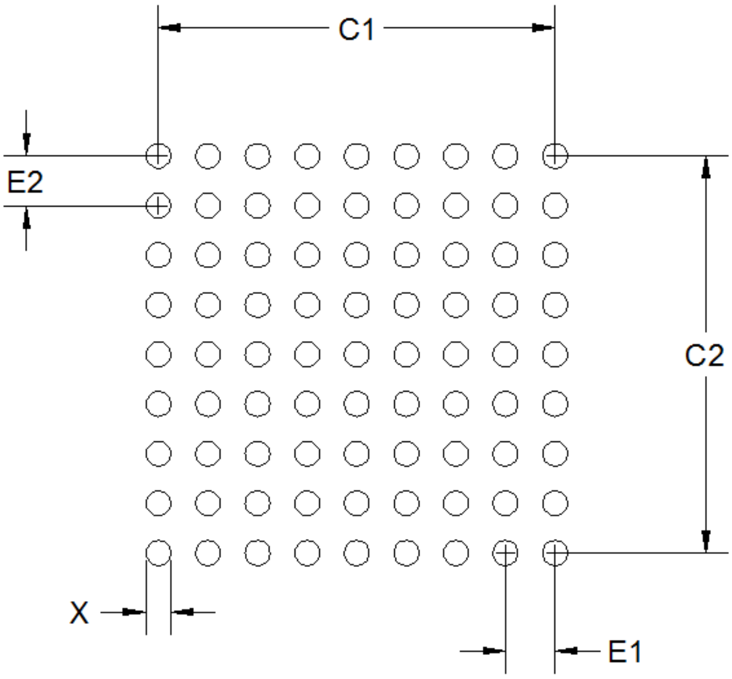



*Table 5.1. CSP81 PCB Land Pattern Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| X | 0.20 |
| C1 | 3.20 |
| C2 | 3.20 |
| E1 | 0.40 |
| E2 | 0.40 |

# List of Tables