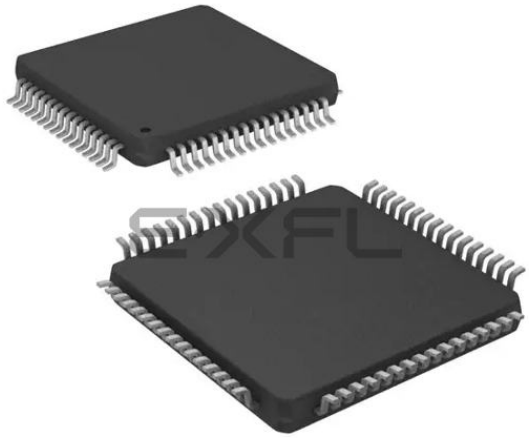

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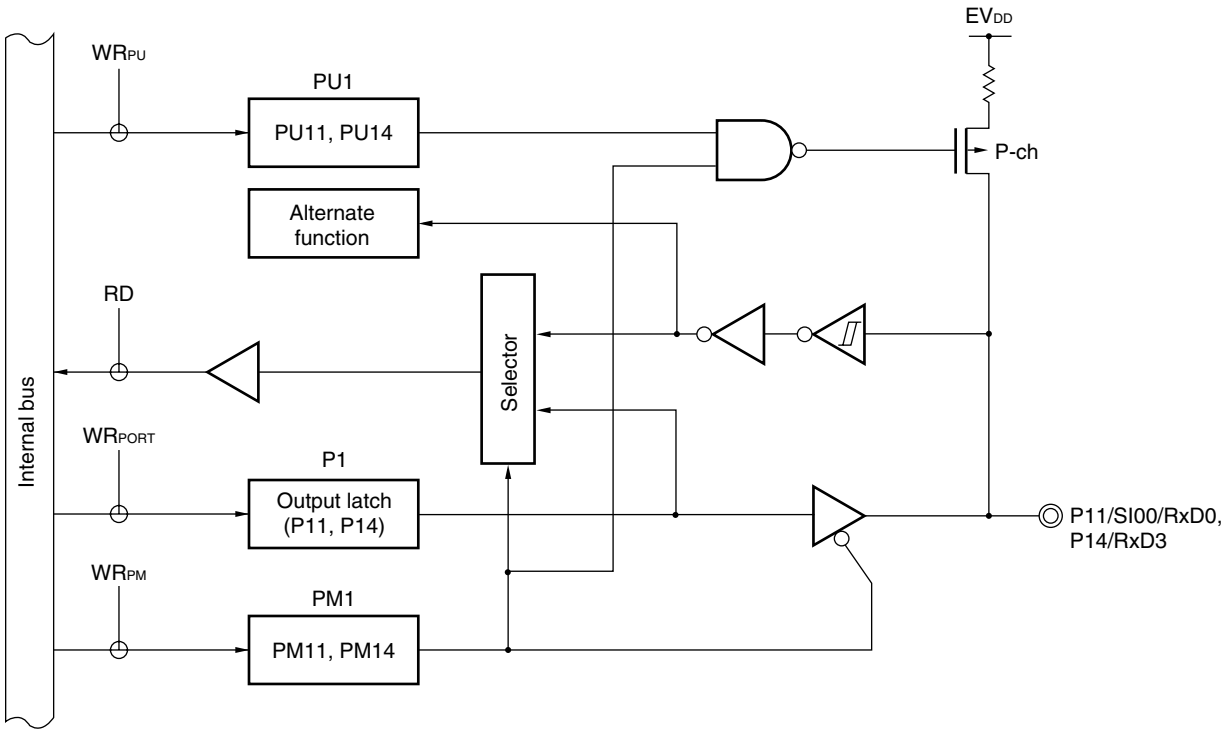
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1142aga-hab-ax

Figure 4-8. Block Diagram of P11 and P14



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

6.2 Configuration of Timer Array Unit

The timer array unit includes the following hardware.

Table 6-1. Configuration of Timer Array Unit

Item	Configuration
Timer/counter	Timer counter register 0n (TCR0n)
Register	Timer data register 0n (TDR0n)
Timer input	TI00 to TI06 pins, RxD3 pin (for LIN-bus)
Timer output	TO00 to TO06 pins, output controller
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Timer clock select register 0 (TPS0) • Timer channel enable status register 0 (TE0) • Timer channel start register 0 (TS0) • Timer channel stop register 0 (TT0) • Timer input select register 0 (TIS0) • Timer output enable register 0 (TOE0) • Timer output register 0 (TO0) • Timer output level register 0 (TOL0) • Timer output mode register 0 (TOM0)
	<Registers of each channel> • Timer mode register 0n (TMR0n) • Timer status register 0n (TSR0n) • Input switch control register (ISC) (channel 7 only) • Noise filter enable register 1 (NFEN1) • Port mode registers 0, 1, 3, 4 (PM0, PM1, PM3, PM4) • Port registers 0, 1, 3, 4 (P0, P1, P3, P4)

Remark n: Channel number (n = 0 to 7)

Figure 6-1 shows the block diagram.

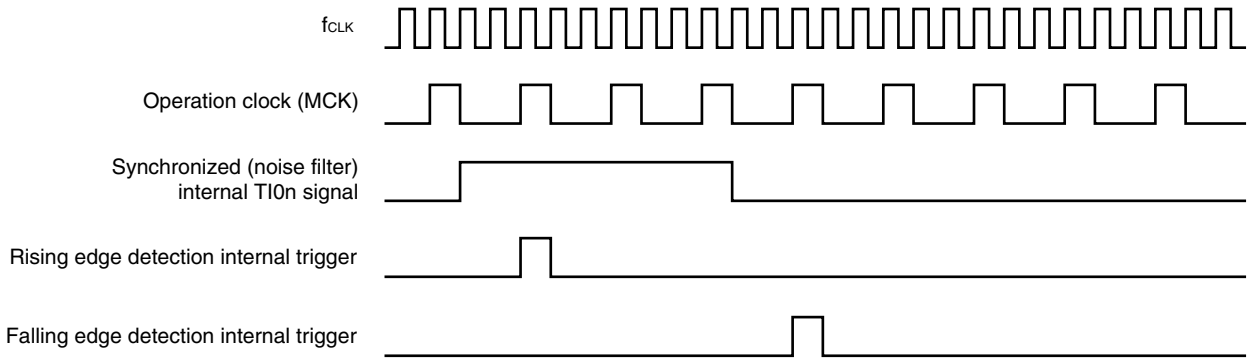
6.5 Channel Input (TI0n Pin) Control

6.5.1 TI0n edge detection circuit

(1) Edge detection basic operation timing

Edge detection circuit sampling is done in accordance with the operation clock (MCK).

Figure 6-34. Edge Detection Basic Operation Timing



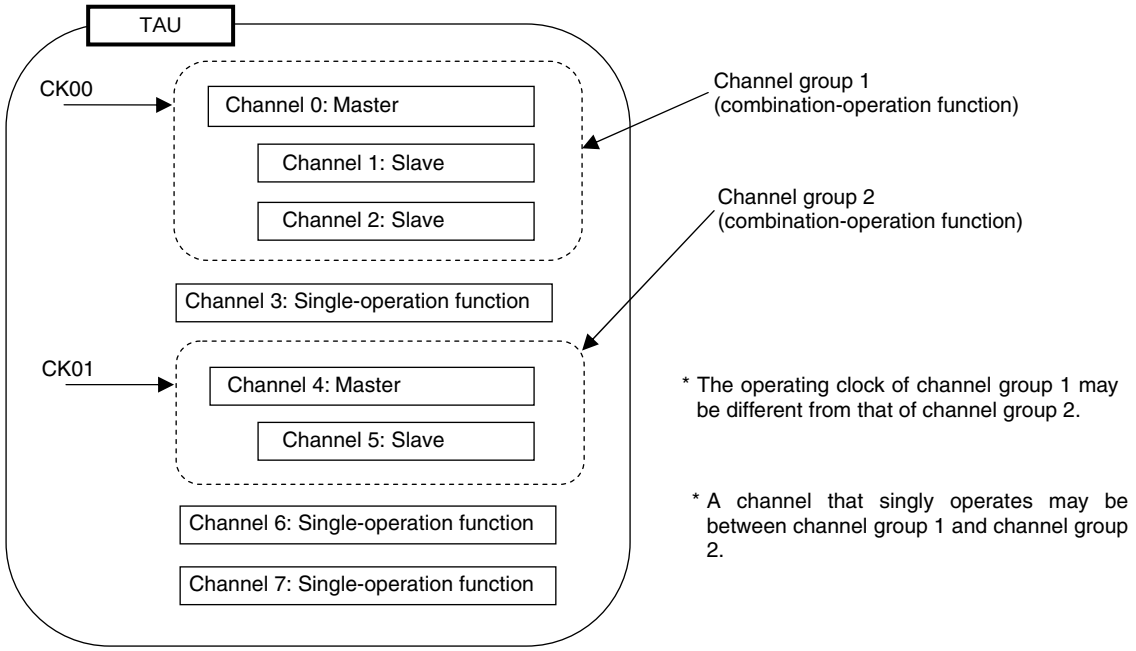
Remark n = 0 to 6

6.6.3 Applicable range of basic rules of combination-operation function

The rules of the combination-operation function are applied in a channel group (a master channel and slave channels forming one combination-operation function).

If two or more channel groups that do not operate in combination are specified, the basic rules of the combination-operation function in **6.6.2 Basic rules of combination-operation function** do not apply to the channel groups.

Example



6.7 Operation of Timer Array Unit as Independent Channel

6.7.1 Operation as interval timer/square wave output

(1) Interval timer

The timer array unit can be used as a reference timer that generates INTTM0n (timer interrupt) at fixed intervals.

The interrupt generation period can be calculated by the following expression.

Generation period of INTTM0n (timer interrupt) = Period of count clock × (Set value of TDR0n + 1)

A subsystem clock divided by four ($f_{SUB}/4$) can be selected as the count clock, in addition to CK00 and CK01. Consequently, the interval timer can be operated with the count clock fixed to $f_{SUB}/4$, regardless of the f_{CLK} frequency (main system clock, subsystem clock). When changing the clock selected as f_{CLK} (changing the value of the system clock control register (CKC)), however, stop the timer array unit (TAU) (TT0 = 00FFH) first.

(2) Operation as square wave output

TO0k performs a toggle operation as soon as INTTM0n has been generated, and outputs a square wave with a duty factor of 50%.

The period and frequency for outputting a square wave from TO0k can be calculated by the following expressions.

- Period of square wave output from TO0k = Period of count clock × (Set value of TDR0n + 1) × 2
- Frequency of square wave output from TO0k = Frequency of count clock/{(Set value of TDR0n + 1) × 2}

TCR0n operates as a down counter in the interval timer mode.

TCR0n loads the value of TDR0n at the first count clock after the channel start trigger bit (TS0n) is set to 1. If MD0n0 of TMR0n = 0 at this time, INTTM0n is not output and TO0k is not toggled. If MD0n0 of TMR0n = 1, INTTM0n is output and TO0k is toggled.

After that, TCR0n count down in synchronization with the count clock.

When TCR0n = 0000H, INTTM0n is output and TO0k is toggled at the next count clock. At the same time, TCR0n loads the value of TDR0n again. After that, the same operation is repeated.

TDR0n can be rewritten at any time. The new value of TDR0n becomes valid from the next period.

Remarks 1. n = 0 to 7, k = 0 to 6

2. f_{CLK}: CPU/peripheral hardware clock frequency

f_{SUB}: Subsystem clock oscillation frequency

(3) 10-bit A/D conversion result register (ADCR)

Use the ADCR register in the same manner as during A/D converter basic operation (see **10.3 (3) 10-bit A/D conversion result register (ADCR)**).

Caution When using a temperature sensor, use the result of the second or later A/D conversion for temperature sensor 0 (ANI0 side), and the result of the third or later A/D conversion for temperature sensor 1 (ANI1 side).

(4) Analog input channel specification register (ADS)

This register specifies the channel from which an analog voltage to be A/D-converted is input, in the same manner as during A/D converter basic operation. When a temperature sensor is used, however, some settings differ from those of A/D converter basic operation.

ADS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-16. Format of Analog Input Channel Specification Register (ADS) When Using Temperature Sensor

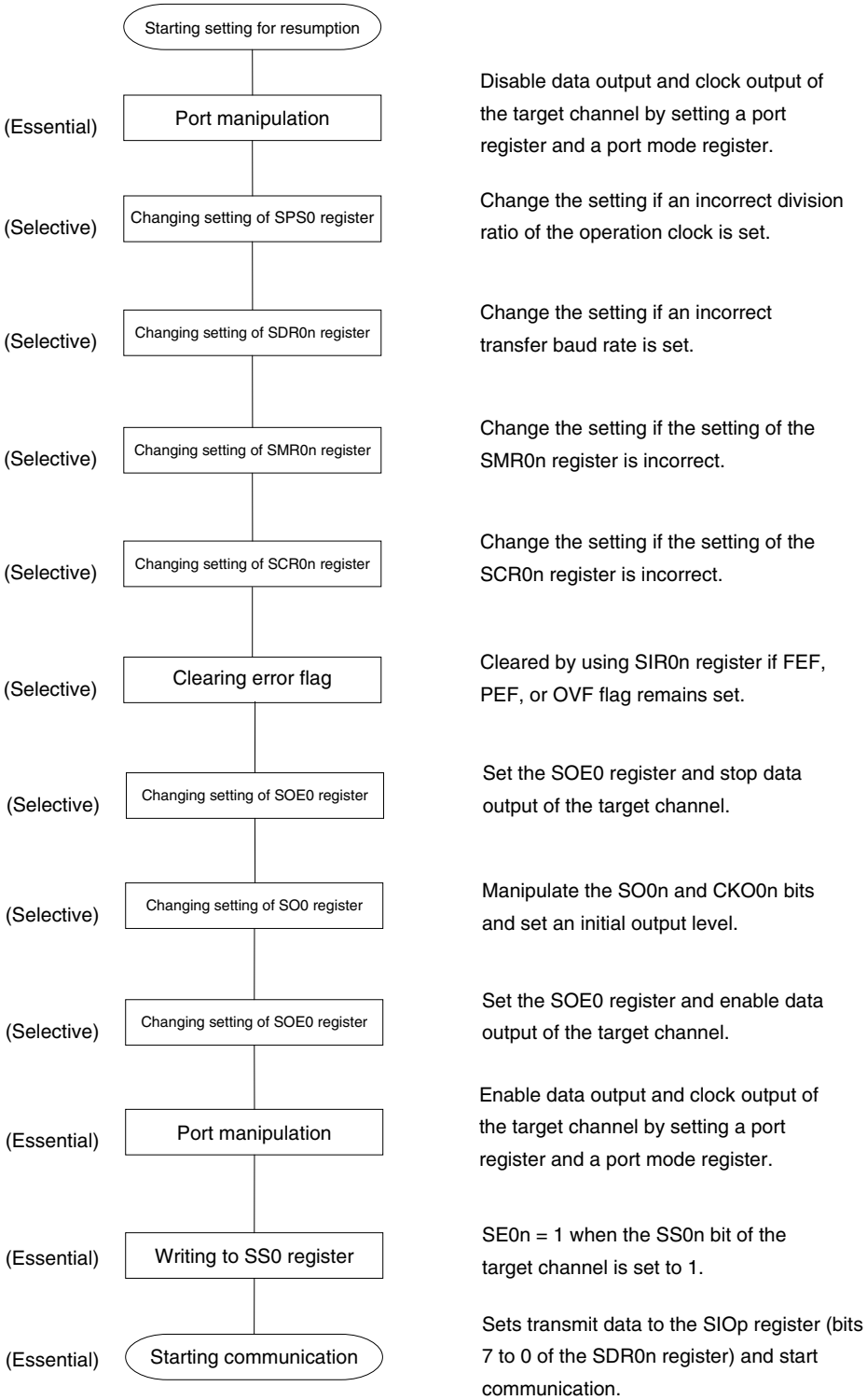
Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	0	ADS3	ADS2	ADS1	ADS0

ADISS	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
1	0	0	0	0	ANI0	Temperature sensor 0 output
1	0	0	0	1	ANI1	Temperature sensor 1 output
Other than above					Setting prohibited	

Caution Be sure to clear bits 4 to 6 to "0".

Figure 11-27. Procedure for Resuming Master Transmission



(1) Register setting

Figure 11-32. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O (CSI00, CSI10)

(a) Serial output register 0 (SO0) … Sets only the bits of the target channel.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	1	CKO02 0/1	1	CKO00 0/1	0	0	0	0	1	SO02 ×	1	SO00 ×

Communication starts when these bits are 1 if the data phase is forward (CKP0n = 0). If the phase is reversed (CKP0n = 1), communication starts when these bits are 0.

<R> **(b) Serial output enable register 0 (SOE0) …The register that not used in this mode.**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE02 ×	×	SOE00 ×

(c) Serial channel start register 0 (SS0) … Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS0	0	0	0	0	0	0	0	0	0	0	0	0	SS03 ×	SS02 0/1	SS01 ×	SS00 0/1

<R> **(d) Serial mode register 0n (SMR0n)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMR0n	CKS0n 0/1	CCS0n 0	0	0	0	0	0	STS0n 0	0	SIS0n0 0	1	0	0	MD0n2 0	MD0n1 0	MD0n0 0/1

Interrupt sources of channel n
0: Transfer end interrupt
1: Buffer empty interrupt

(e) Serial communication operation setting register 0n (SCR0n)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR0n	TXE0n 0	RXE0n 1	DAP0n 0/1	CKP0n 0/1	0	EOC0n 0	PTC0n1 0	PTC0n0 0	DIR0n 0/1	0	SLC0n1 0	SLC0n0 0	0	DLS0n2 1	DLS0n1 1	DLS0n0 0/1

(f) Serial data register 0n (SDR0n) (lower 8 bits: SIOp)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDR0n	Baud rate setting							0	Receive data register (Write FFH as dummy data.)							

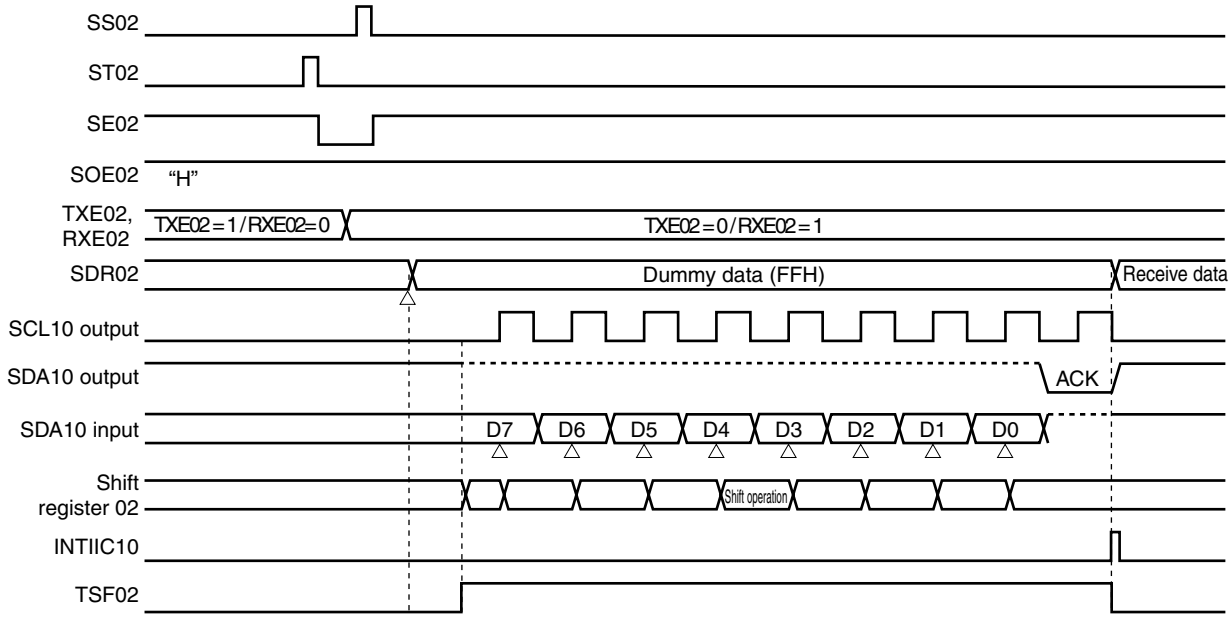
SIOp

Remark n: Channel number (n = 0, 2), p: CSI number (p = 00, 10)
□: Setting is fixed in the CSI master reception mode, ▒: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

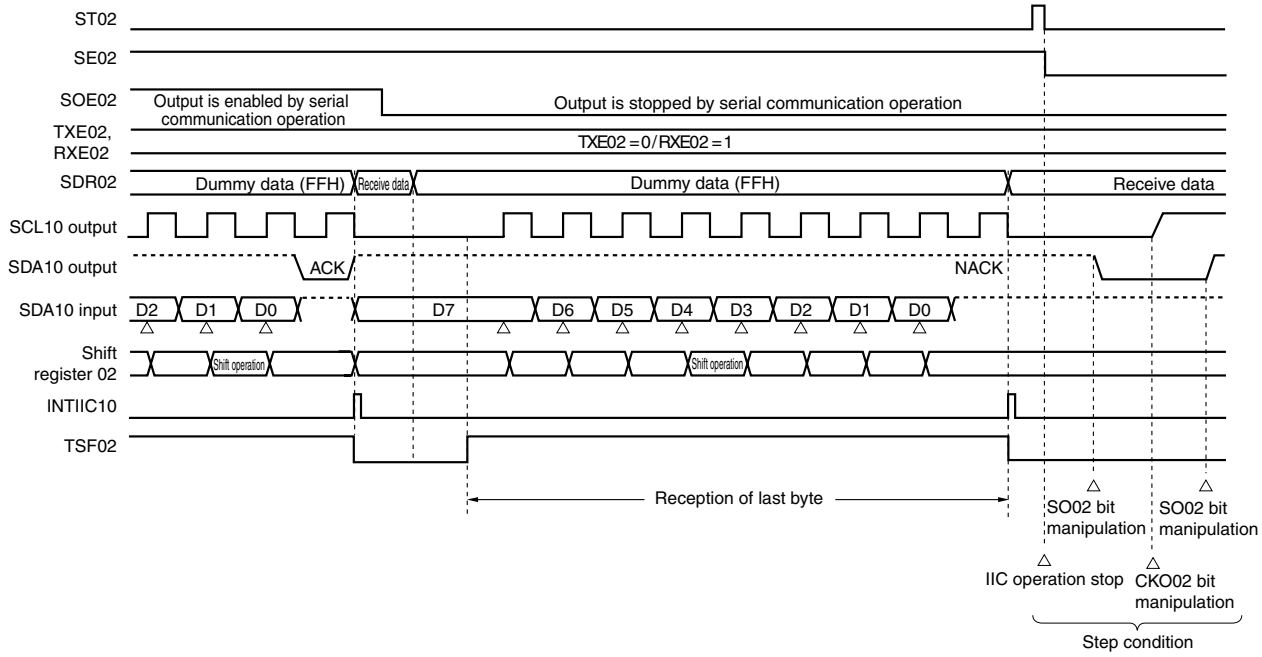
(2) Processing flow

Figure 11-101. Timing Chart of Data Reception

(a) When starting data reception



(b) When receiving last data



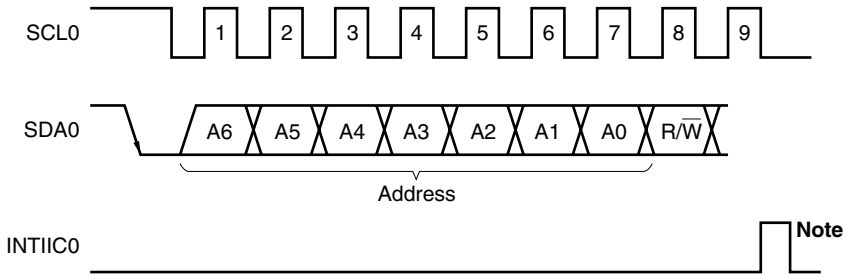
12.5.2 Addresses

The address is defined by the 7 bits of data that follow the start condition.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via the bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in slave address register 0 (SVA0). If the address data matches the SVA0 values, the slave device is selected and communicates with the master device until the master device generates a start condition or stop condition.

Figure 12-15. Address



Note INTIIC0 is not issued if data other than a local address or extension code is received during slave device operation.

The slave address and the eighth bit, which specifies the transfer direction as described in **12.5.3 Transfer direction specification** below, are together written to IIC shift register 0 (IIC0) and are then output. Received addresses are written to IIC0.

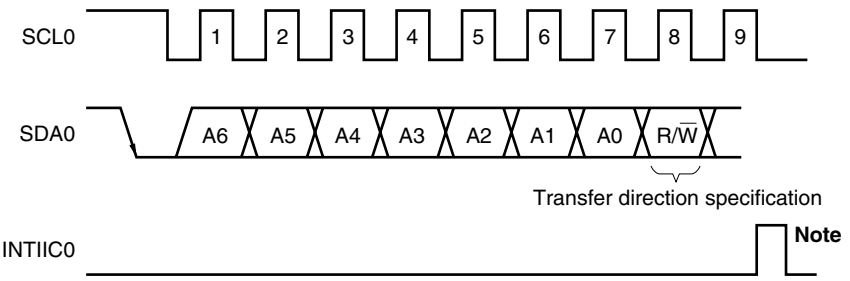
The slave address is assigned to the higher 7 bits of IIC0.

12.5.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction.

When this transfer direction specification bit has a value of “0”, it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of “1”, it indicates that the master device is receiving data from a slave device.

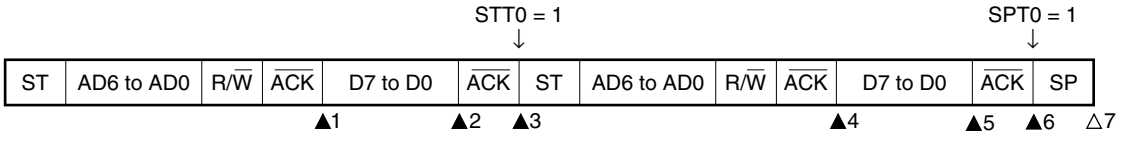
Figure 12-16. Transfer Direction Specification



Note INTIIC0 is not issued if data other than a local address or extension code is received during slave device operation.

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

(i) When WTIM0 = 0



▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000×000B (Sets WTIM0 to 1)[Note 1]
▲3: IICS0 = 1000××00B (Clears WTIM0 to 0[Note 2], sets STT0 to 1)
▲4: IICS0 = 1000×110B
▲5: IICS0 = 1000×000B (Sets WTIM0 to 1)[Note 3]
▲6: IICS0 = 1000××00B (Sets SPT0 to 1)
△7: IICS0 = 00000001B

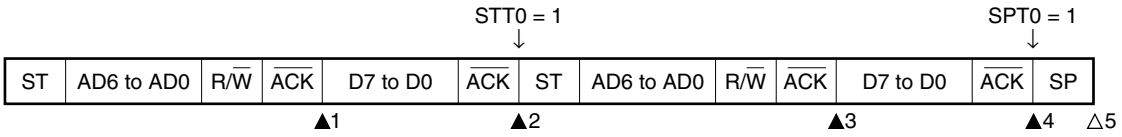
Notes 1. To generate a start condition, set WTIM0 to 1 and change the timing for generating the INTIIC0 interrupt request signal.

2. Clear WTIM0 to 0 to restore the original setting.

3. To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIIC0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1

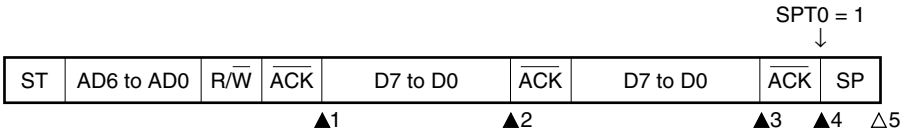


▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000××00B (Sets STT0 to 1)
▲3: IICS0 = 1000×110B
▲4: IICS0 = 1000××00B (Sets SPT0 to 1)
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When WTIM0 = 0

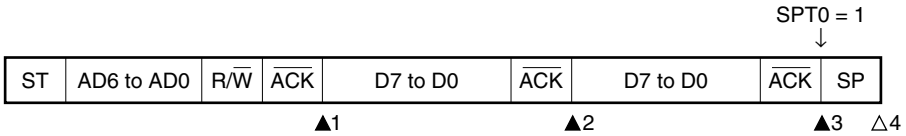


▲1: IICS0 = 1010×110B
▲2: IICS0 = 1010×000B
▲3: IICS0 = 1010×000B (Sets WTIM0 to 1)[Note]
▲4: IICS0 = 1010××00B (Sets SPT0 to 1)
△5: IICS0 = 00000001B

Note To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIIC0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1



▲1: IICS0 = 1010×110B
▲2: IICS0 = 1010×100B
▲3: IICS0 = 1010××00B (Sets SPT0 to 1)
△4: IICS0 = 00001001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

14.3 Registers Controlling DMA Controller

DMA controller is controlled by the following registers.

- DMA mode control register n (DMCn)
- DMA operation control register n (DRCn)

Remark n: DMA channel number (n = 0, 1)

Table 17-1. Operating Statuses in HALT Mode (2/2)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock
			When CPU Is Operating on XT1 Clock (f_{XT})
System clock			Clock supply to the CPU is stopped
	Main system clock	f_{IH}	Status before HALT mode was set is retained
		f_X	
		f_{EX}	Operates or stops by external clock input
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped)
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Oscillates • WTON = 1 and WDSTBYON = 0: Stops
CPU			Operation stopped
Flash memory			Operable in low-current consumption mode
RAM			Operation stopped. However, status before HALT mode was set is retained at voltage higher than POC detection voltage.
Port (latch)			Status before HALT mode was set is retained
Timer array unit (TAU)			Operable
Real-time counter (RTC)			
Watchdog timer			Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Operates • WTON = 1 and WDSTBYON = 0: Stops
Clock output/buzzer output			Operable
A/D converter			Cannot operate
Serial array unit (SAU)			Operable
Serial interface (IIC0)			Cannot operate
Multiplier			Operation stopped
DMA controller			Operable
Power-on-clear function			
Low-voltage detection function			
External interrupt			
Key interrupt function			

Remark f_{IH}: Internal high-speed oscillation clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{IL}: Internal low-speed oscillation clock

17.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the main system clock.

Caution Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.

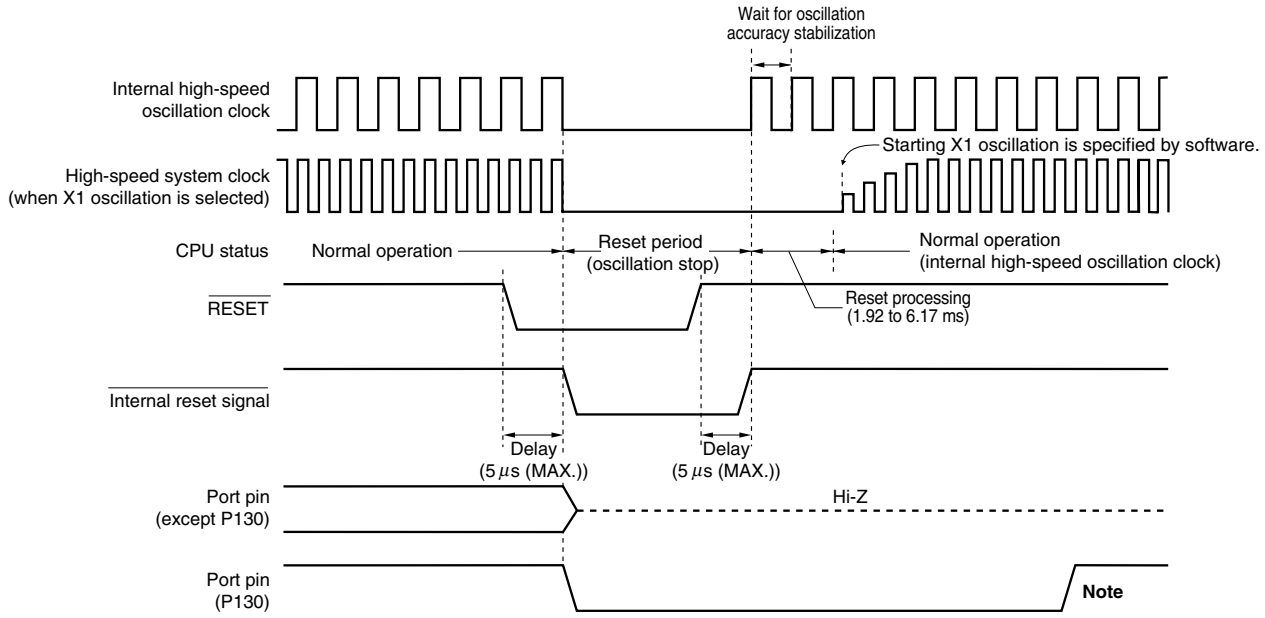
The operating statuses in the STOP mode are shown below.

Table 17-2. Operating Statuses in STOP Mode

Item \ STOP Mode Setting	When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
	When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
System clock	Clock supply to the CPU is stopped		
Main system clock (f_{IH})	Stopped		
Main system clock (f_X)	Stopped		
Main system clock (f_{EX})	Stopped		
Subsystem clock (f_{XT})	Status before STOP mode was set is retained		
f_{IL}	Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Oscillates • WTON = 1 and WDSTBYON = 0: Stops		
CPU	Operation stopped		
Flash memory	Operation stopped		
RAM	Operation stopped. However, status before STOP mode was set is retained at voltage higher than POC detection voltage.		
Port (latch)	Status before STOP mode was set is retained		
Timer array unit (TAU)	Operation stopped		
Real-time counter (RTC)	Operable		
Watchdog timer	Set by bits 0 (WDSTBYON) and 4 (WTON) of option byte (000C0H) • WTON = 0: Stops • WTON = 1 and WDSTBYON = 1: Operates • WTON = 1 and WDSTBYON = 0: Stops		
Clock output/buzzer output	Operable only when subsystem clock is selected as the count clock		
A/D converter	Operation stopped		
Serial array unit (SAU)	Operation stopped		
Serial interface (IIC0)	Operation stopped		
Multiplier	Operation stopped		
DMA controller	Operation stopped		
Power-on-clear function	Operable		
Low-voltage detection function	Operable		
External interrupt	Operable		
Key interrupt function	Operable		

Remark f_{IH}: Internal high-speed oscillation clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{IL}: Internal low-speed oscillation clock

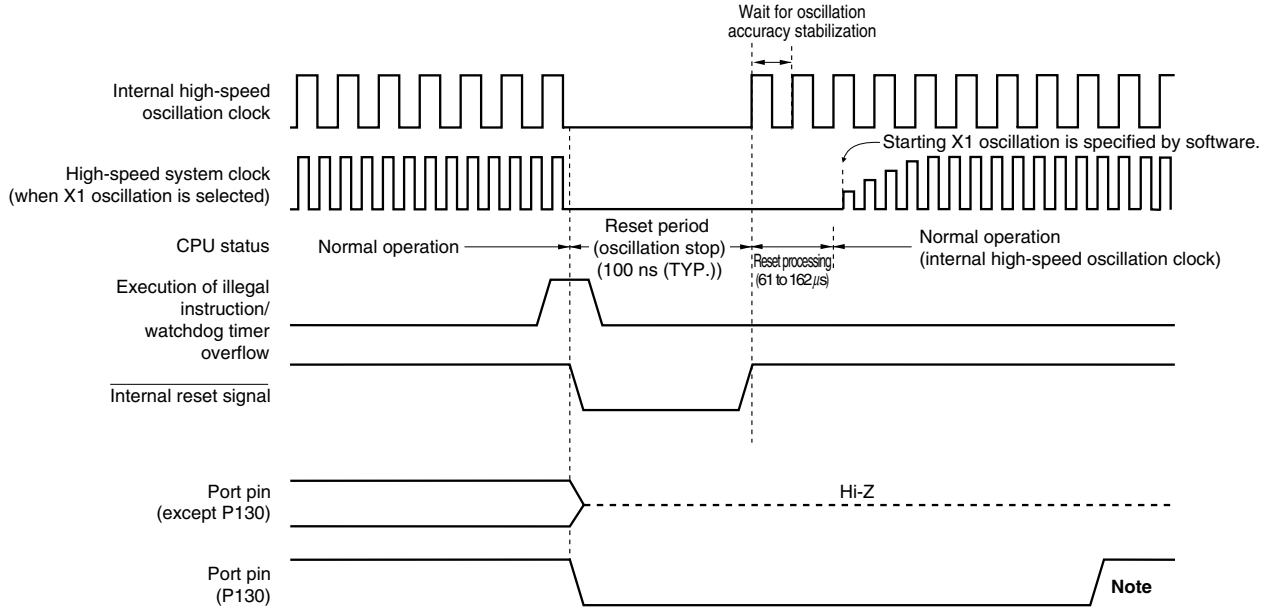
Figure 18-2. Timing of Reset by $\overline{\text{RESET}}$ Input



Note Set P130 to high-level output by software.

Remark When reset is effected, P130 outputs a low level. If P130 is set to output a high level before reset is effected, the output signal of P130 can be dummy-output as the CPU reset signal.

Figure 18-3. Timing of Reset Due to Execution of Illegal Instruction or Watchdog Timer Overflow



Note Set P130 to high-level output by software.

Caution A watchdog timer internal reset resets the watchdog timer.

Remark When reset is effected, P130 outputs a low level. If P130 is set to output a high level before reset is effected, the output signal of P130 can be dummy-output as the CPU reset signal.

DC Characteristics (3/10)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P01, P02, P12, P13, P15, P41, P52 to P55, P121 to P124		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00, P03 to P06, P10, P11, P14, P16, P17, P30, P31, P40, P42, P43, P50, P51, P70 to P77, P120, P140, P141, EXCLK, $\overline{RESET}$	Normal input buffer	0.8V_{DD}		V_{DD}	V
	V_{IH3}	P03, P04	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 2.7 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 1.8 V ≤ V_{DD} < 2.7 V	1.6		V_{DD}	V
	V_{IH4}	P20 to P27	2.7 V ≤ AV_{REF} ≤ V_{DD}	0.7AV_{REF}		AV_{REF}	V
			AV_{REF} = V_{DD} < 2.7 V				
	V_{IH5}	P60 to P63		0.7V_{DD}		6.0	V
	V_{IH6}	FLMD0		0.9V_{DD} Note 1		V_{DD}	V
Input voltage, low	V_{IL1}	P01, P02, P12, P13, P15, P41, P52 to P55, P121 to P124		0		0.3V_{DD}	V
	V_{IL2}	P00, P03 to P06, P10, P11, P14, P16, P17, P30, P31, P40, P42, P43, P50, P51, P70 to P77, P120, P140, P141, EXCLK, $\overline{RESET}$	Normal input buffer	0		0.2V_{DD}	V
	V_{IL3}	P03, P04	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 2.7 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.8 V ≤ V_{DD} < 2.7 V	0		0.2	V
	V_{IL4}	P20 to P27	2.7 V ≤ AV_{REF} ≤ V_{DD}	0		0.3AV_{REF}	V
			AV_{REF} = V_{DD} < 2.7 V				
	V_{IL5}	P60 to P63		0		0.3V_{DD}	V
	V_{IL6}	FLMD0 Note 2		0		0.1V_{DD}	V

Notes 1. The high-level input voltage (V_{IH6}) must be greater than 0.9V_{DD} when using it in the flash memory programming mode.

2. When disabling writing of the flash memory, connect the FLMD0 pin processing directly to V_{SS}, and maintain a voltage less than 0.1V_{DD}.

Cautions 1. The maximum value of V_{IH} of pins P02 to P04 is V_{DD}, even in the N-ch open-drain mode.

2. For P122/EXCLK, the value of V_{IH} and V_{IL} differs according to the input port mode or external clock mode.

Make sure to satisfy the DC characteristics of EXCLK in external clock input mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(2) Serial interface: Serial array unit (15/18)

Caution Select the TTL input buffer for SI10 and $\overline{SCK10}$ and the N-ch open drain output (V_{DD} tolerance) mode for SO10 by using the PIM0 and POM0 registers.

Remarks 1. R_b[Ω]:Communication line (SO10) pull-up resistance,
C_b[F]: Communication line (SO10) load capacitance, V_b[V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS02 bit of the SMR02 register.)

3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

$4.0\ V \le V_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$: $V_{IH} = 2.2\ V$, $V_{IL} = 0.8\ V$

$2.7\ V \le V_{DD} \le 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$

4. CSI00 cannot communicate at different potential. Use CSI10 for communication at different potential.

APPENDIX C REVISION HISTORY

C.1 Major Revisions in This Edition

(1/5)

Page	Description	Classification
Throughout		
–	Change of status of **(A) grade products of the expanded-specification products** and **64-pin plastic FBGA (6 × 6) package** from under development to mass production	(b), (d)
CHAPTER 1 OUTLINE		
p.17	Change of **1.1 Differences Between Conventional-Specification Products (μPD78F114x) and Expanded-Specification Products (μPD78F114xA)**	(c)
CHAPTER 3 CPU ARCHITECTURE		
pp.58 to 62	Change of **Figure 3-7** to **Figure 3-11 Correspondence Between Data Memory and Addressing**	(c)
p.64	Addition of **Caution** to **3.2.1 (3) Stack pointer (SP)**	(c)
CHAPTER 5 CLOCK GENERATOR		
pp.141, 142	Addition of f_{MAINC} to **Figure 5-1. Block Diagram of Clock Generator** and **Remark**	(c)
p.143	Change of description of AMPH bit in **Figure 5-2. Format of Clock Operation Mode Control Register (CMC)**	(c)
p.151	Change of description of RTCEN bit in **Figure 5-7. Format of Peripheral Enable Register (1/2)**	(c)
p.153	Change of **Caution 5** in **Figure 5-8. Format of Operation Speed Mode Control Register (OSMC)**	(c)
p.173	Change of description of AMPH bit in **Table 5-4. CPU Clock Transition and SFR Register Setting Examples (1/4) (2)** and addition of **Remark**	(c)
p.174	Change of description of AMPH bit in **Table 5-4. CPU Clock Transition and SFR Register Setting Examples (2/4) (4)** and addition of **Remark**	(c)
p.176	Change of **(9) CPU clock changing from subsystem clock (D) to high-speed system clock (C)** in **Table 5-4. CPU Clock Transition and SFR Register Setting Examples (4/4)**	(c)
p.176	Change of **(11) • STOP mode (H) set while CPU is operating with internal high-speed oscillation clock (B) • STOP mode (I) set while CPU is operating with high-speed system clock (C)** in **Table 5-4. CPU Clock Transition and SFR Register Setting Examples (4/4)**	(c)
p.179	Change of **Table 5-6. Maximum Time Required for Main System Clock Switchover**	(c)
p.179	Change of **Table 5-8. Maximum Number of Clocks Required in Type 2**	(c)
p.180	Change of **Table 5-9. Maximum Number of Clocks Required in Type 3** and addition of **Remark**	(c)
CHAPTER 6 TIMER ARRAY UNIT		
p.191	Change of **CKS0n** bit in **Figure 6-6. Format of Timer Mode Register 0n (TMR0n) (1/3)**	(c)
p.199	Change of **Figure 6-13. Start Timing (In One-count Mode)**	(a)
p.200	Change of **Figure 6-14. Start Timing (In Capture & One-count Mode)**	(a)
p.206	Change of description of ISC1 and ISC0 bits in **Figure 6-21. Format of Input Switch Control Register (ISC)**	(a)
CHAPTER 7 REAL-TIME COUNTER		
p.261	Change of **Table 7-1. Configuration of Real-Time Counter**	(c)
p.263	Change of **7.3 Registers Controlling Real-Time Counter**	(c)
p.265	Change of description of AMPM bit in **Figure 7-3. Format of Real-Time Counter Control Register 0 (RTCC0)**	(c)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents