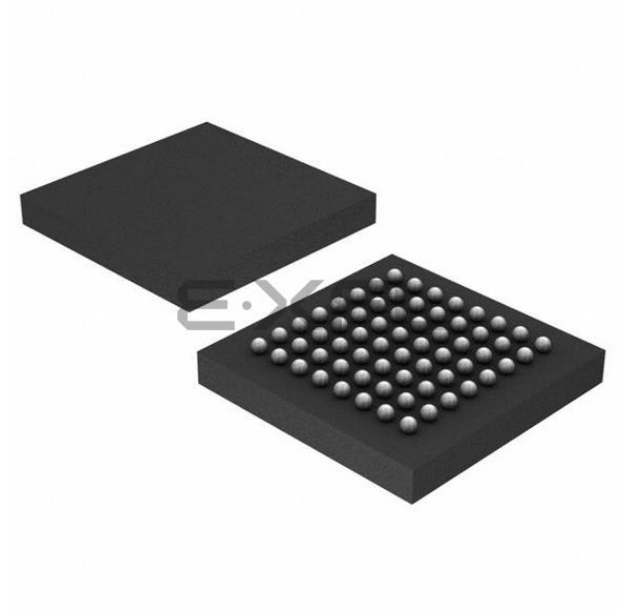

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Correspondence between the address values and block numbers in the flash memory are shown below.

Table 3-1. Correspondence Between Address Values and Block Numbers in Flash Memory

Address Value	Block Number	Address Value	Block Number	Address Value	Block Number	Address Value	Block Number
00000H to 007FFH	00H	10000H to 107FFH	20H	20000H to 207FFH	40H	30000H to 307FFH	60H
00800H to 00FFFH	01H	10800H to 10FFFH	21H	20800H to 20FFFH	41H	30800H to 30FFFH	61H
01000H to 017FFH	02H	11000H to 117FFH	22H	21000H to 217FFH	42H	31000H to 317FFH	62H
01800H to 01FFFH	03H	11800H to 11FFFH	23H	21800H to 21FFFH	43H	31800H to 31FFFH	63H
02000H to 027FFH	04H	12000H to 127FFH	24H	22000H to 227FFH	44H	32000H to 327FFH	64H
02800H to 02FFFH	05H	12800H to 12FFFH	25H	22800H to 22FFFH	45H	32800H to 32FFFH	65H
03000H to 037FFH	06H	13000H to 137FFH	26H	23000H to 237FFH	46H	33000H to 337FFH	66H
03800H to 03FFFH	07H	13800H to 13FFFH	27H	23800H to 23FFFH	47H	33800H to 33FFFH	67H
04000H to 047FFH	08H	14000H to 147FFH	28H	24000H to 247FFH	48H	34000H to 347FFH	68H
04800H to 04FFFH	09H	14800H to 14FFFH	29H	24800H to 24FFFH	49H	34800H to 34FFFH	69H
05000H to 057FFH	0AH	15000H to 157FFH	2AH	25000H to 257FFH	4AH	35000H to 357FFH	6AH
05800H to 05FFFH	0BH	15800H to 15FFFH	2BH	25800H to 25FFFH	4BH	35800H to 35FFFH	6BH
06000H to 067FFH	0CH	16000H to 167FFH	2CH	26000H to 267FFH	4CH	36000H to 367FFH	6CH
06800H to 06FFFH	0DH	16800H to 16FFFH	2DH	26800H to 26FFFH	4DH	36800H to 36FFFH	6DH
07000H to 077FFH	0EH	17000H to 177FFH	2EH	27000H to 277FFH	4EH	37000H to 377FFH	6EH
07800H to 07FFFH	0FH	17800H to 17FFFH	2FH	27800H to 27FFFH	4FH	37800H to 37FFFH	6FH
08000H to 087FFH	10H	18000H to 187FFH	30H	28000H to 287FFH	50H	38000H to 387FFH	70H
08800H to 08FFFH	11H	18800H to 18FFFH	31H	28800H to 28FFFH	51H	38800H to 38FFFH	71H
09000H to 097FFH	12H	19000H to 197FFH	32H	29000H to 297FFH	52H	39000H to 397FFH	72H
09800H to 09FFFH	13H	19800H to 19FFFH	33H	29800H to 29FFFH	53H	39800H to 39FFFH	73H
0A000H to 0A7FFH	14H	1A000H to 1A7FFH	34H	2A000H to 2A7FFH	54H	3A000H to 3A7FFH	74H
0A800H to 0AFFFH	15H	1A800H to 1AFFFH	35H	2A800H to 2AFFFH	55H	3A800H to 3AFFFH	75H
0B000H to 0B7FFH	16H	1B000H to 1B7FFH	36H	2B000H to 2B7FFH	56H	3B000H to 3B7FFH	76H
0B800H to 0BFFFH	17H	1B800H to 1BFFFH	37H	2B800H to 2BFFFH	57H	3B800H to 3BFFFH	77H
0C000H to 0C7FFH	18H	1C000H to 1C7FFH	38H	2C000H to 2C7FFH	58H	3C000H to 3C7FFH	78H
0C800H to 0CFFFH	19H	1C800H to 1CFFFH	39H	2C800H to 2CFFFH	59H	3C800H to 3CFFFH	79H
0D000H to 0D7FFH	1AH	1D000H to 1D7FFH	3AH	2D000H to 2D7FFH	5AH	3D000H to 3D7FFH	7AH
0D800H to 0DFFFH	1BH	1D800H to 1DFFFH	3BH	2D800H to 2DFFFH	5BH	3D800H to 3DFFFH	7BH
0E000H to 0E7FFH	1CH	1E000H to 1E7FFH	3CH	2E000H to 2E7FFH	5CH	3E000H to 3E7FFH	7CH
0E800H to 0EFFFH	1DH	1E800H to 1EFFFH	3DH	2E800H to 2EFFFH	5DH	3E800H to 3EFFFH	7DH
0F000H to 0F7FFH	1EH	1F000H to 1F7FFH	3EH	2F000H to 2F7FFH	5EH	3F000H to 3F7FFH	7EH
0F800H to 0FFFFH	1FH	1F800H to 1FFFFH	3FH	2F800H to 2FFFFH	5FH	3F800H to 3FFFFH	7FH

Remark μPD78F1142, PD78F1142A: Block numbers 00H to 1FH
μPD78F1143, PD78F1143A: Block numbers 00H to 2FH
μPD78F1144, PD78F1144A: Block numbers 00H to 3FH
μPD78F1145, PD78F1145A: Block numbers 00H to 5FH
μPD78F1146, PD78F1146A: Block numbers 00H to 7FH

4.3 Registers Controlling Port Function

Port functions are controlled by the following six types of registers.

- Port mode registers (PM0 to PM7, PM12, PM14)
- Port registers (P0 to P7, P12 to P14)
- Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7, PU12, PU14)
- Port input mode register (PIM0)
- Port output mode register (POM0)
- A/D port configuration register (ADPC)

(1) Port mode registers (PM0 to PM7, PM12, PM14)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register by referencing **4.5 Settings of Port Mode Register and Output Latch When Using Alternate Function**.

(6) A/D port configuration register (ADPC)

This register switches the P20/ANI0 to P27/ANI7 pins to digital I/O of port or analog input of A/D converter.

ADPC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 4-33. Format of A/D Port Configuration Register (ADPC)

Address: F0017H After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching							
					ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	0	A	A	A	A	A	A	A	A
0	0	0	0	1	A	A	A	A	A	A	A	D
0	0	0	1	0	A	A	A	A	A	A	D	D
0	0	0	1	1	A	A	A	A	A	D	D	D
0	0	1	0	0	A	A	A	A	D	D	D	D
0	0	1	0	1	A	A	A	D	D	D	D	D
0	0	1	1	0	A	A	D	D	D	D	D	D
0	0	1	1	1	A	D	D	D	D	D	D	D
0	1	0	0	0	D	D	D	D	D	D	D	D
1	0	0	0	0	D	D	D	D	D	D	D	D
Other than above					Setting prohibited							

Cautions 1. Set the channel used for A/D conversion to the input mode by using port mode registers 2 (PM2).

2. Do not set the pin set by ADPC as digital I/O by analog input channel specification register (ADS).

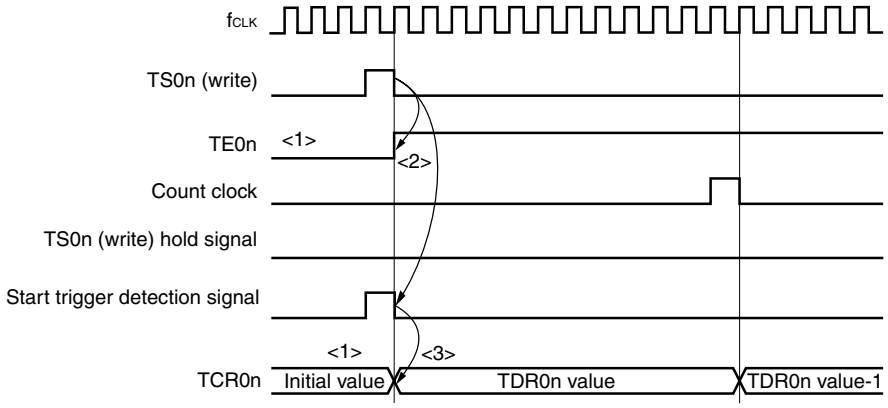
3. When using all ANI0/P20 to ANI7/P27 pins as digital I/O (D), the setting can be done by ADPC4 to ADPC0 = either 01000 or 10000.

4. P20/ANI0 to P27/ANI7 are set as analog inputs in the order of P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 as analog inputs, start designing from P27/ANI7.

(b) Start timing in event counter mode

<1> While TE0n is set to 0, TCR0n holds the initial value.
<2> Writing 1 to TS0n sets 1 to TE0n.
<3> As soon as 1 has been written to TS0n and 1 has been set to TE0n, the "TDR0n value" is loaded to TCR0n to start counting.
<4> After that, the TCR0n value is counted down according to the count clock.

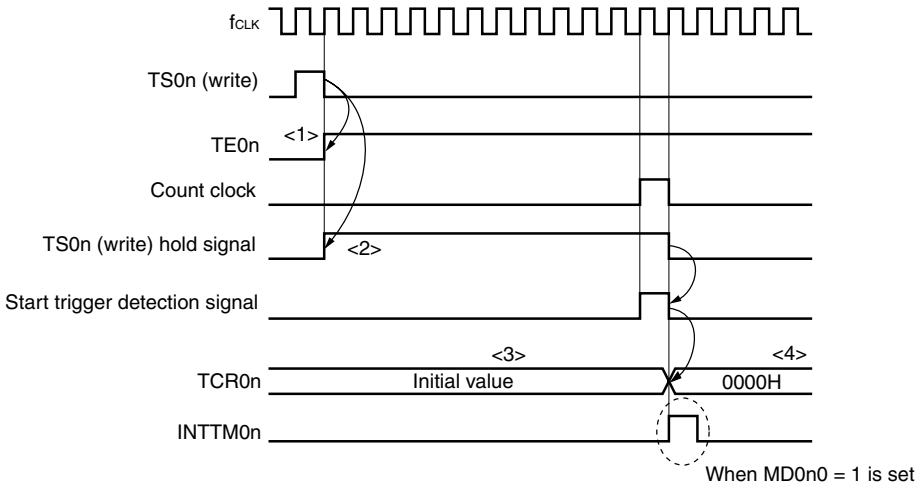
Figure 6-11. Start Timing (In Event Counter Mode)



(c) Start timing in capture mode

<1> Writing 1 to TS0n sets TE0n = 1
<2> The write data to TS0n is held until count clock generation.
<3> TCR0n holds the initial value until count clock generation.
<4> On generation of count clock, 0000H is loaded to TCR0n and count starts.

Figure 6-12. Start Timing (In Capture Mode)



Caution In the first cycle operation of count clock after writing TS0n, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting MD0n0 = 1.

(e) Start timing in capture & one-count mode

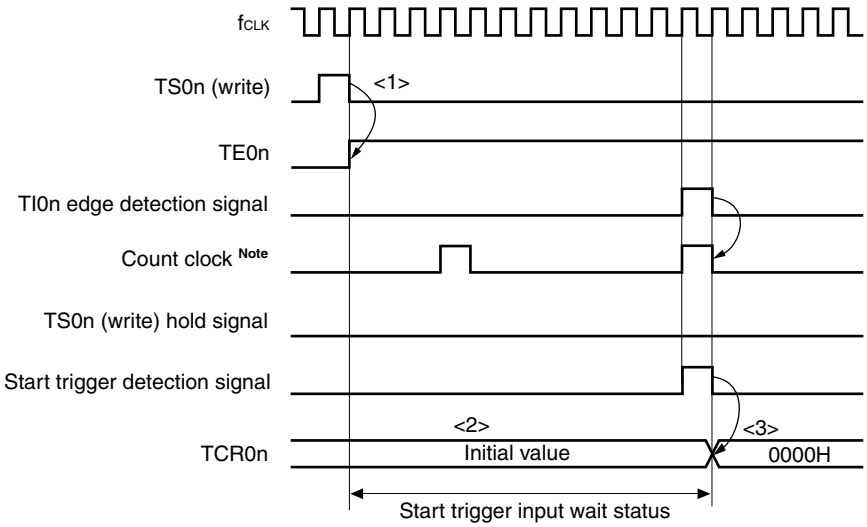
<1> Writing 1 to TS0n sets TE0n = 1

<2> Enters the start trigger input wait status, and TCR0n holds the initial value.

<3> On start trigger detection, 0000H is loaded to TCR0n and count starts.

Figure 6-14. Start Timing (In Capture & One-count Mode)

<R>



Note When the capture & one-count mode is set, the operation clock (MCK) is selected as count clock (CCS0n = 0).

Caution An input signal sampling error is generated since operation starts upon start trigger detection (The error is one count clock when TI0k is used).

6.7.3 Operation as frequency divider (channel 0 only)

The timer array unit can be used as a frequency divider that divides a clock input to the TI00 pin and outputs the result from TO00.

The divided clock frequency output from TO00 can be calculated by the following expression.

- When rising edge/falling edge is selected:
  Divided clock frequency = Input clock frequency/{(Set value of TDR00 + 1) × 2}
- When both edges are selected:
  Divided clock frequency ≅ Input clock frequency/(Set value of TDR00 + 1)

TCR00 operates as a down counter in the interval timer mode.

After the channel start trigger bit (TS00) is set to 1, TCR00 loads the value of TDR00 when the TI00 valid edge is detected. If MD000 of TMR00 = 0 at this time, INTTM00 is not output and TO00 is not toggled. If MD000 of TMR00 = 1, INTTM00 is output and TO00 is toggled.

After that, TCR00 counts down at the valid edge of TI0k. When TCR00 = 0000H, it toggles TO00. At the same time, TCR00 loads the value of TDR00 again, and continues counting.

If detection of both the edges of TI00 is selected, the duty factor error of the input clock affects the divided clock period of the TO00 output.

The period of the TO00 output clock includes a sampling error of one period of the operation clock.

Clock period of TO00 output = Ideal TO00 output clock period ± Operation clock period (error)

TDR00 can be rewritten at any time. The new value of TDR00 becomes valid during the next count period.

Figure 6-43. Block Diagram of Operation as Frequency Divider

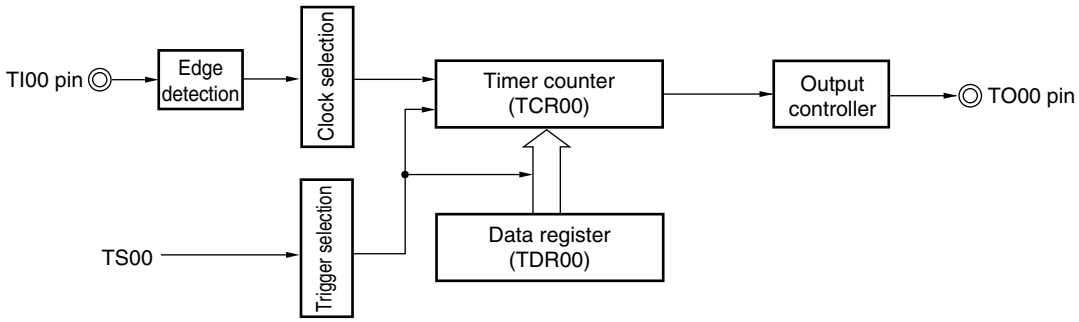


Figure 6-64. Operation Procedure of One-Shot Pulse Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPS0 register. Determines clock frequencies of CK00 and CK01.	
Channel default setting	Sets the TMR0n and TMR0m registers of two channels to be used (determines operation mode of channels). An output delay is set to the TDR0n register of the master channel, and a pulse width is set to the TDR0m register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOM0m bit of the TOM0 register is set to 1 (combination-operation mode). Sets the TOL0m bit. Sets the TO0m bit and determines default level of the TO0m output. →	The TO0m pin goes into Hi-Z output state. The TO0m default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets TOE0m to 1 and enables operation of TO0m. →	TO0m does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TO0m pin outputs the TO0m set level.

Remark n = 0, 2, 4
m = n + 1

(12) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 10-28. Internal Equivalent Circuit of ANIn Pin

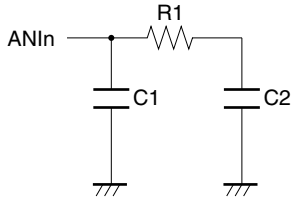


Table 10-6. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{REF}	R1	C1	C2
4.0 V ≤ V_{DD} ≤ 5.5 V	8.1 kΩ	8 pF	5 pF
2.7 V ≤ V_{DD} < 4.0 V	31 kΩ	8 pF	5 pF
2.3 V ≤ V_{DD} < 2.7 V	381 kΩ	8 pF	5 pF

Remarks 1. The resistance and capacitance values shown in Table 10-6 are not guaranteed values.

2. n = 0 to 7

<R> **(13) Starting the A/D converter**

Start the A/D converter after the AV_{REF} voltage stabilize.

(9) Serial channel start register m (SSm)

SSm is a trigger register that is used to enable starting communication/count by each channel.

When 1 is written a bit of this register (SSmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is set to 1. Because SSmn is a trigger bit, it is cleared immediately when SEmn = 1.

SSm can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of SSm can be set with an 1-bit or 8-bit memory manipulation instruction with SSmL.

Reset signal generation clears this register to 0000H.

Figure 11-12. Format of Serial Channel Start Register m (SSm)

Address: F0122H, F0123H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS0	0	0	0	0	0	0	0	0	0	0	0	0	SS03	SS02	SS01	SS00

Address: F0162H, F0163H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS1	0	0	0	0	0	0	0	0	0	0	0	0	SS13	SS12	0	0

SSmn	Operation start trigger of channel n
0	No trigger operation
1	Sets SEmn to 1 and enters the communication wait status (if a communication operation is already under execution, the operation is stopped and the start condition is awaited).

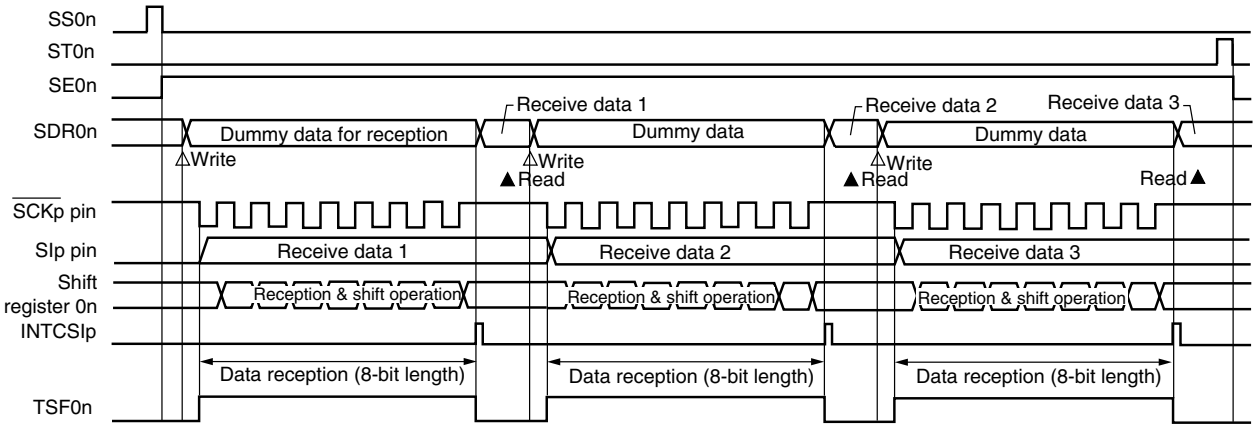
Caution Be sure to clear bits 15 to 4 of SS0, and bits 15 to 4, 1 and 0 of SS1 to "0".

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 12, 13

2. When the SSm register is read, 0000H is always read.

(3) Processing flow (in single-reception mode)

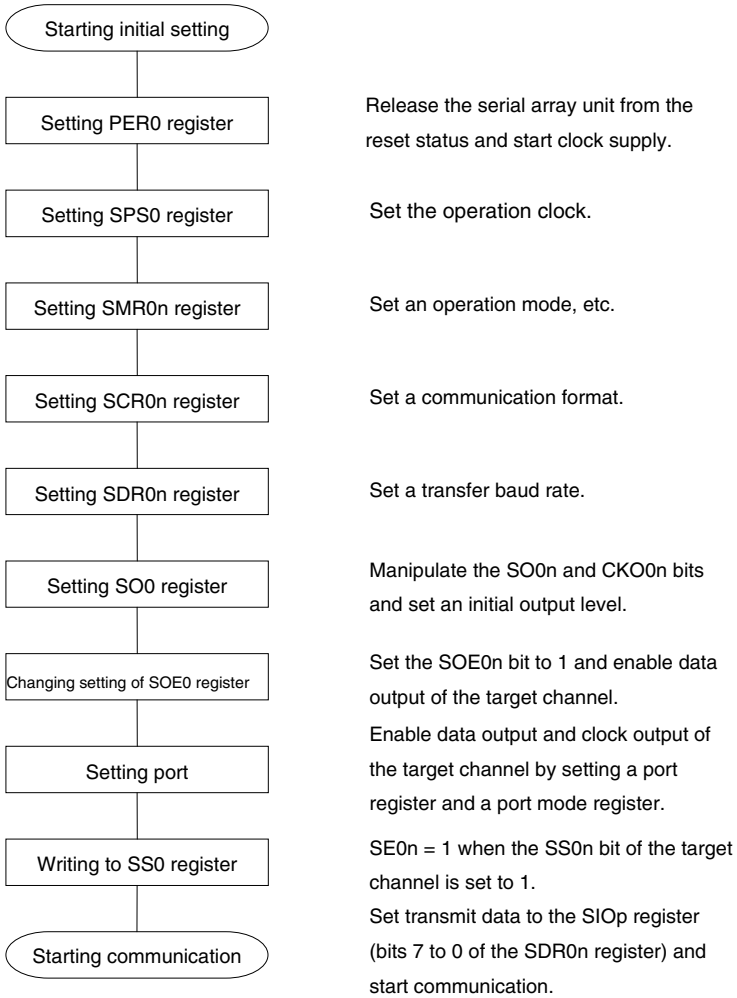
Figure 11-36. Timing Chart of Master Reception (in Single-Reception Mode) (Type 1: DAP0n = 0, CKP0n = 0)



Remark n: Channel number (n = 0, 2), p: CSI number (p = 00, 10)

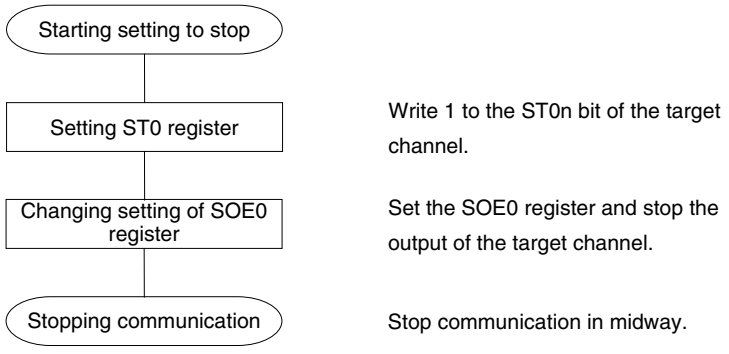
(2) Operation procedure

Figure 11-41. Initial Setting Procedure for Master Transmission/Reception



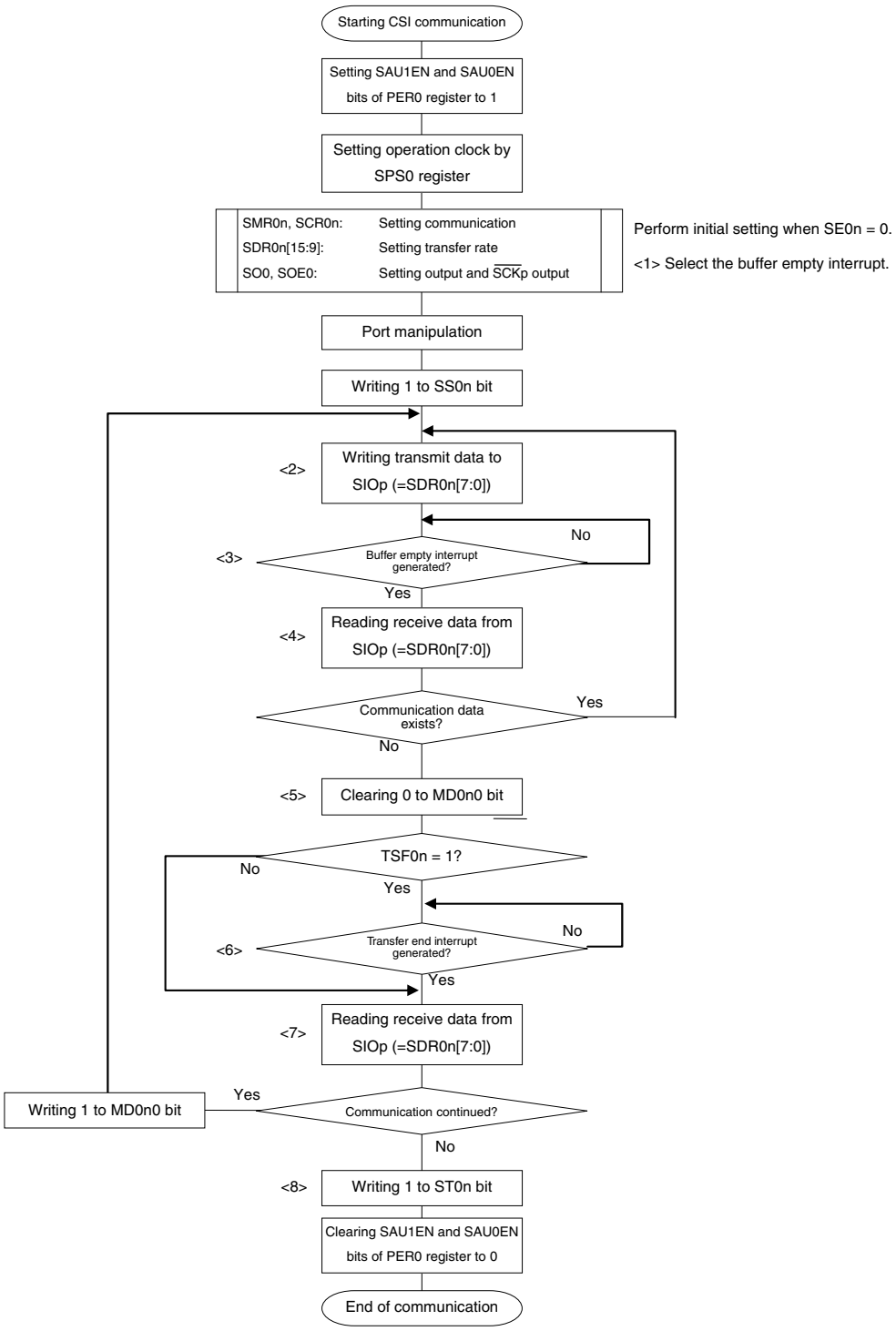
Caution After setting the PER0 register to 1, be sure to set the SPS0 register after 4 or more clocks have elapsed.

Figure 11-42. Procedure for Stopping Master Transmission/Reception



Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set the SO0 register (see **Figure 11-43 Procedure for Resuming Master Transmission/Reception**).

Figure 11-47. Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)



Caution After setting the PER0 register to 1, be sure to set the SPS0 register after 4 or more clocks have elapsed.

Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 11-46 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**.

(1) Register setting

Figure 11-97. Example of Contents of Registers for Data Transmission of Simplified I^2C (IIC10)

(a) Serial output register 0 (SO0) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	1	CKO02 0/1 Note	1	CKO00 ×	0	0	0	0	1	SO02 0/1 Note	1	SO00 ×

(b) Serial output enable register 0 (SOE0) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE02 1	0	SOE00 ×

(c) Serial channel start register 0 (SS0) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS0	0	0	0	0	0	0	0	0	0	0	0	0	SS03 ×	SS02 0/1	SS01 ×	SS00 ×

(d) Serial mode register 02 (SMR02) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMR02	CKS02 0/1	CCS02 0	0	0	0	0	0	STS02 0	0	SIS020 0	1	0	0	MD022 1	MD021 0	MD020 0

(e) Serial communication operation setting register 02 (SCR02) … Do not manipulate the bits of this register, except the TXE02 and RXE02 bits, during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR02	TXE02 1	RXE02 0	DAP02 0	CKP02 0	0	EOC02 0	PTC021 0	PTC020 0	DIR02 0	0	SLC021 0	SLC020 1	0	DLS022 1	DLS021 1	DLS020 1

(f) Serial data register 02 (SDR02) (lower 8 bits: SIO10)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDR02	Baud rate setting							0	Transmit data setting							

SIO10

Note The value varies depending on the communication data during communication operation.

Remark □: Setting is fixed in the IIC mode, ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Processing flow

Figure 11-98. Timing Chart of Data Transmission

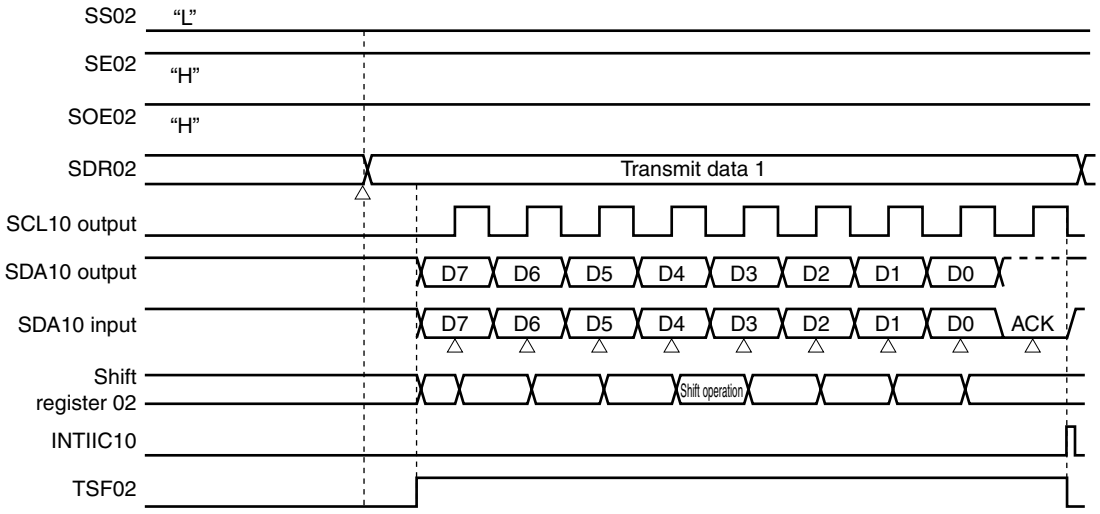


Figure 11-99. Flowchart of Data Transmission

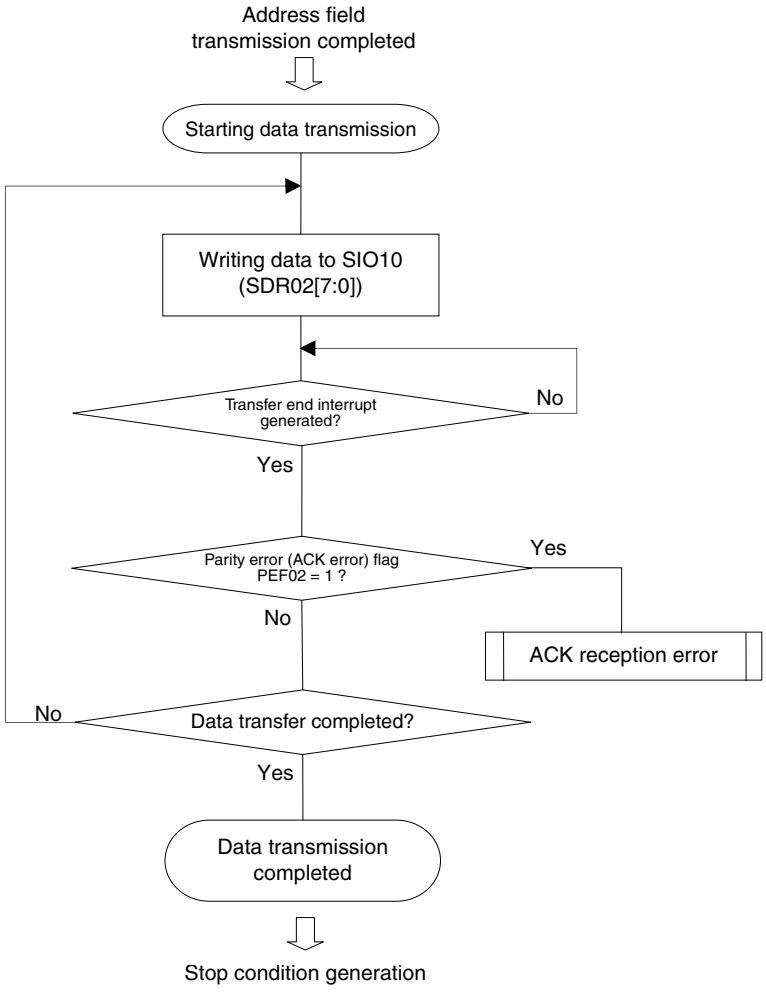


Table 15-1. Interrupt Source List (2/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	24	INTAD	End of A/D conversion	Internal	0034H	(A)
	25	INTRTC	Fixed-cycle signal of real-time counter/alarm match detection		0036H	
	26	INTRTCI	Interval signal detection of real-time counter		0038H	
	27	INTKR	Key return signal detection	External	003AH	(C)
	28	INTTM04	End of timer channel 4 count or capture	Internal	0042H	(A)
	29	INTTM05	End of timer channel 5 count or capture		0044H	
	30	INTTM06	End of timer channel 6 count or capture		0046H	
	31	INTTM07	End of timer channel 7 count or capture		0048H	
	32	INTP6	Pin input edge detection	External	004AH	(B)
	33	INTP7			004CH	
	34	INTP8			004EH	
	35	INTP9			0050H	
	36	INTP10			0052H	
	37	INTP11			0054H	
Software	–	BRK	Execution of BRK instruction	–	007EH	(D)
Reset	–	RESET	$\overline{\text{RESET}}$ pin input	–	0000H	–
		POC	Power-on-clear			
		LVI	Low-voltage detection[Note 3]			
		WDT	Overflow of watchdog timer			
		TRAP	Execution of illegal instruction[Note 4]			

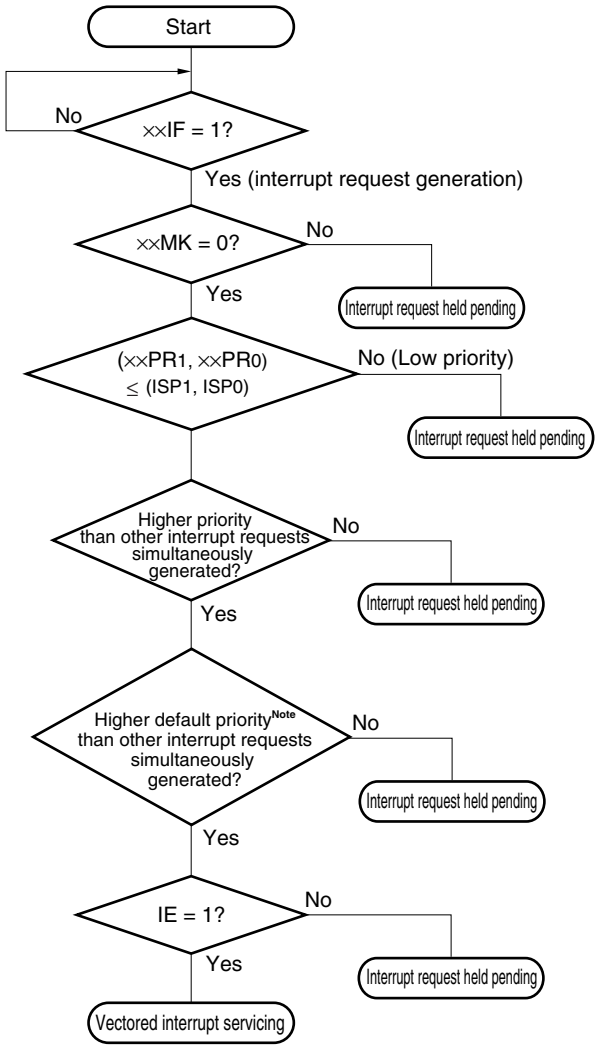
Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 37 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 15-1.

3. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is set to 1.

4. When the instruction code in FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Figure 15-7. Interrupt Request Acknowledgment Processing Algorithm



××IF: Interrupt request flag
××MK: Interrupt mask flag
××PR0: Priority specification flag 0
××PR1: Priority specification flag 1
IE: Flag that controls acknowledgment of maskable interrupt request (1 = Enable, 0 = Disable)
ISP0, ISP1: Flag that indicates the priority level of the interrupt currently being serviced (see **Figure 15-6**)

Note For the default priority, refer to **Table 15-1 Interrupt Source List**.

CHAPTER 16 KEY INTERRUPT FUNCTION

16.1 Functions of Key Interrupt

A key interrupt (INTKR) can be generated by setting the key return mode register (KRM) and inputting a falling edge to the key interrupt input pins (KR0 to KR7).

Table 16-1. Assignment of Key Interrupt Detection Pins

Flag	Description
KRM0	Controls KR0 signal in 1-bit units.
KRM1	Controls KR1 signal in 1-bit units.
KRM2	Controls KR2 signal in 1-bit units.
KRM3	Controls KR3 signal in 1-bit units.
KRM4	Controls KR4 signal in 1-bit units.
KRM5	Controls KR5 signal in 1-bit units.
KRM6	Controls KR6 signal in 1-bit units.
KRM7	Controls KR7 signal in 1-bit units.

16.2 Configuration of Key Interrupt

The key interrupt includes the following hardware.

Table 16-2. Configuration of Key Interrupt

<R>

Item	Configuration
Control register	Key return mode register (KRM) Port mode register 7 (PM7)

Figure 16-1. Block Diagram of Key Interrupt

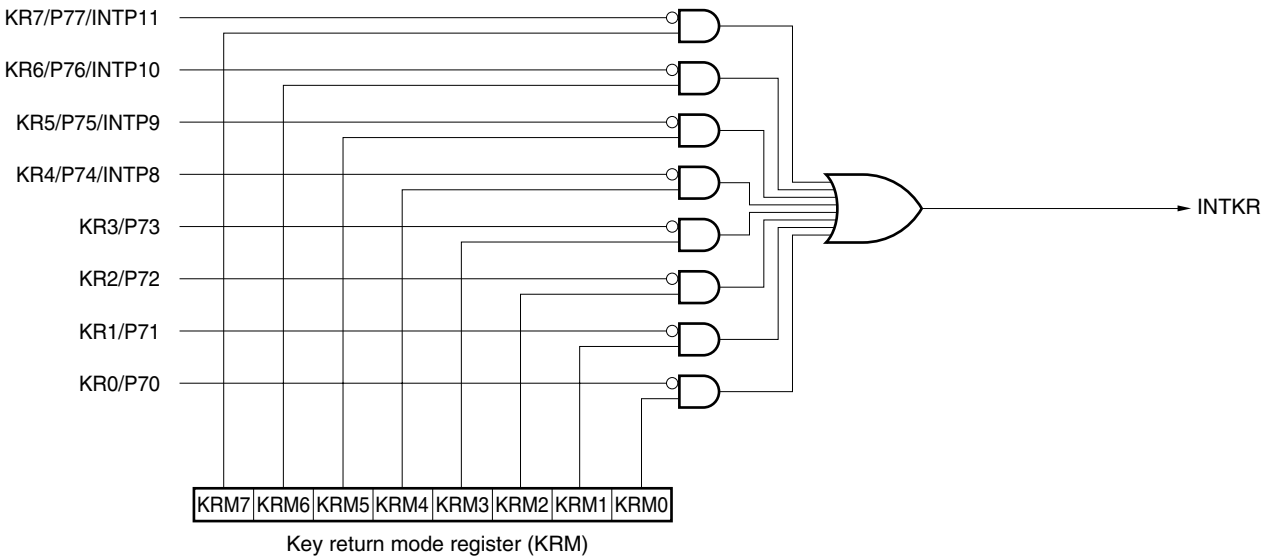


Table 23-3. Relationship Between FLMD0 Pin and Operation Mode After Reset Release

FLMD0	Operation Mode
0	Normal operation mode
V_{DD}	Flash memory programming mode

23.6.3 Selecting communication mode

Communication mode of the 78K0R/KE3 is as follows.

Table 23-4. Communication Modes

Communication Mode	Standard Setting[Note 1]				Pins Used
	Port	Speed[Note 2]	Frequency	Multiply Rate	
1-line mode (single-line UART)	UART	115,200 bps, 250,000 bps, 500,000 bps, 1 Mbps	–	–	TOOL0

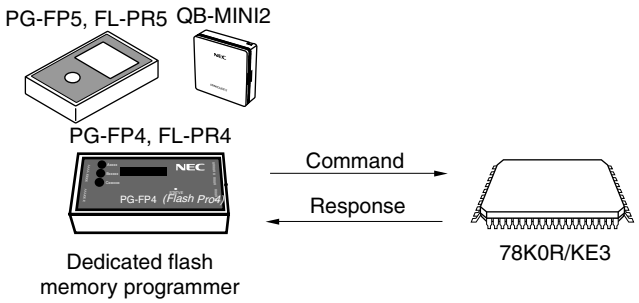
Notes 1. Selection items for Standard settings on GUI of the flash memory programmer.

2. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

23.6.4 Communication commands

The 78K0R/KE3 communicates with the dedicated flash memory programmer by using commands. The signals sent from the flash memory programmer to the 78K0R/KE3 are called commands, and the signals sent from the 78K0R/KE3 to the dedicated flash memory programmer are called response.

Figure 23-9. Communication Commands



The flash memory control commands of the 78K0R/KE3 are listed in the table below. All these commands are issued from the programmer and the 78K0R/KE3 perform processing corresponding to the respective commands.

DC Characteristics (2/10)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P02, P05, P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.5	mA
		Per pin for P03, P04	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.6	mA
		Per pin for P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			3.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77 (When duty = 70%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty = 60%[Note 2])	4.0 V ≤ V_{DD} ≤ 5.5 V			65.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			50.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			29.0	mA
	I_{OL2}	Per pin for P20 to P27	AV_{REF} ≤ V_{DD}			0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to EV_{SS}, V_{SS}, and AV_{SS} pin.

2. Specification under conditions where the duty factor is 60% or 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where I_{OL} = 20.0 mA and n = 50%

Total output current of pins = (20.0 × 0.7)/(50 × 0.01) = 28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.