Renesas Electronics America Inc - UPD78F1145AGK-GAJ-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1145agk-gaj-ax

Table 3-3. Vector Table

Vector Table Address	Interrupt Source	Vector Table Address	Interrupt Source
00000H	$\overline{\text{RESET}}$ input, POC, LVI, WDT, TRAP	0002AH	INTIIC0
		0002CH	INTTM00
00004H	INTWDTI	0002EH	INTTM01
00006H	INTLVI	00030H	INTTM02
00008H	INTP0	00032H	INTTM03
0000AH	INTP1	00034H	INTAD
0000CH	INTP2	00036H	INTRTC
0000EH	INTP3	00038H	INTRTCI
00010H	INTP4	0003AH	INTKR
00012H	INTP5	00042H	INTTM04
00014H	INTST3	00044H	INTTM05
00016H	INTSR3	00046H	INTTM06
00018H	INTSRE3	00048H	INTTM07
0001AH	INTDMA0	0004AH	INTP6
0001CH	INTDMA1	0004CH	INTP7
0001EH	INTST0/INTCSI00	0004EH	INTP8
00020H	INTSR0	00050H	INTP9
00022H	INTSRE0	00052H	INTP10
00024H	INTST1/INTCSI10/INTIIC10	00054H	INTP11
00026H	INTSR1	0007EH	BRK
00028H	INTSRE1		

(2) CALLT instruction table area

The 64-byte area 00080H to 000BFH can store the subroutine entry address of a 2-byte call instruction (CALLT). Set the subroutine entry address to a value in a range of 00000H to 0FFFFH (because an address code is of 2 bytes).

To use the boot swap function, set a CALLT instruction table also at 01080H to 010BFH.

(3) Option byte area

A 4-byte area of 000C0H to 000C3H can be used as an option byte area. Set the option byte at 010C0H to 010C3H when the boot swap is used. For details, see **CHAPTER 22 OPTION BYTE**.

(4) On-chip debug security ID setting area

A 10-byte area of 000C4H to 000CDH and 010C4H to 010CDH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when the boot swap is not used and at 000C4H to 000CDH and 010C4H to 010CDH when the boot swap is used. For details, see **CHAPTER 24 ON-CHIP DEBUG FUNCTION**.

Figure 4-28. Format of Port Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	1	PM31	PM30	FFF23H	FFH	R/W
PM4	1	1	1	1	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	PM55	PM54	PM53	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	1	1	1	1	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM14	1	1	1	1	1	1	PM141	PM140	FFF2EH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 7, 12, 14; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bit 7 of PM0, bits 2 to 7 of PM3, bits 4 to 7 of PM4, bits 6 and 7 of PM5, bits 4 to 7 of PM6, bits 1 to 7 of PM12, and bits 2 to 7 of PM14 to “1”.

(12) Timer output mode register 0 (TOM0)

TOM0 is used to control the timer output mode of each channel.

When a channel is used for the single-operation function, set the corresponding bit of the channel to be used to 0.

When a channel is used for the combination-operation function (PWM output, one-shot pulse output, or multiple PWM output), set the corresponding bit of the master channel to 0 and the corresponding bit of the slave channel to 1.

The setting of each channel n by this register is reflected at the timing when the timer output signal is set or reset while the timer output is enabled (TOE0n = 1).

TOM0 can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of TOM0 can be set with an 8-bit memory manipulation instruction with TOM0L.

Reset signal generation clears this register to 0000H.

Figure 6-20. Format of Timer Output Mode Register 0 (TOM0)

Address: F01BEH, F01BFH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOM0	0	0	0	0	0	0	0	0	0	TOM06	TOM05	TOM04	TOM03	TOM02	TOM01	TOM00

TOM0n	Control of timer output mode of channel n
0	Toggle mode (to produce toggle output by timer interrupt request signal (INTTM0n))
1	Combination-operation mode (output is set by the timer interrupt request signal (INTTM0n) of the master channel, and reset by the timer interrupt request signal (INTTM0m) of the slave channel)

Caution Be sure to clear bits 15 to 7 to "0".

Remark n: Channel number, m: Slave channel number
n = 0 to 6 (n = 0, 2, 4 for master channel)
n < m ≤ 6 (where m is a consecutive integer greater than n)

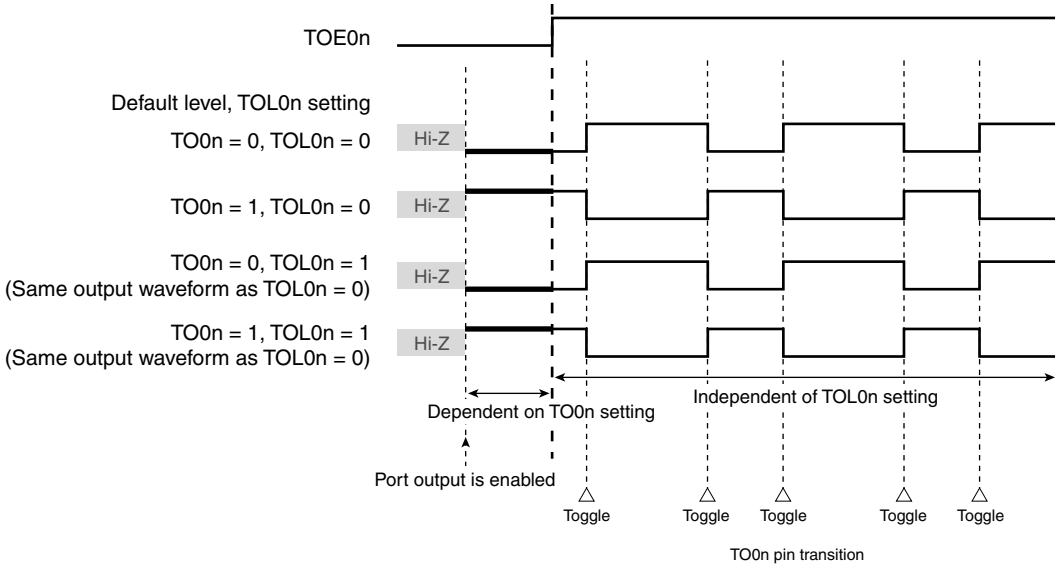
(2) Default level of TO0n pin and output level after timer operation start

The following figure shows the TO0n pin output level transition when writing has been done in the state of TOE0n = 0 before port output is enabled and TOE0n = 1 is set after changing the default level.

(a) When operation starts with TOM0n = 0 setting (toggle output)

The setting of TOL0n is invalid when TOM0n = 0. When the timer operation starts after setting the default level, the toggle signal is generated and the output level of TO0n pin is reversed.

Figure 6-26. TO0n Pin Output Status at Toggle Output (TOM0n = 0)



Remarks 1. Toggle: Reverse TO0n pin output status

2. n = 0 to 6

CHAPTER 7 REAL-TIME COUNTER

7.1 Functions of Real-Time Counter

The real-time counter has the following features.

- Having counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.
- Constant-period interrupt function (period: 1 month to 0.5 seconds)
- Alarm interrupt function (alarm: week, hour, minute)
- Interval interrupt function
- Pin output function of 1 Hz
- Pin output function of 512 Hz or 16.384 kHz or 32.768 kHz

7.2 Configuration of Real-Time Counter

The real-time counter includes the following hardware.

<R>

Table 7-1. Configuration of Real-Time Counter

Item	Configuration
Control registers	Peripheral enable register 0 (PER0) Real-time counter control register 0 (RTCC0) Real-time counter control register 1 (RTCC1) Real-time counter control register 2 (RTCC2) Sub-count register (RSUBC) Second count register (SEC) Minute count register (MIN) Hour count register (HOUR) Day count register (DAY) Week count register (WEEK) Month count register (MONTH) Year count register (YEAR) Watch error correction register (SUBCUD) Alarm minute register (ALARMWM) Alarm hour register (ALARMWH) Alarm week register (ALARMWW) Port mode registers 1 and 3 (PM1, PM3) Port registers 1 and 3 (P1, P3)

(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale − 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 10-21. Zero-Scale Error

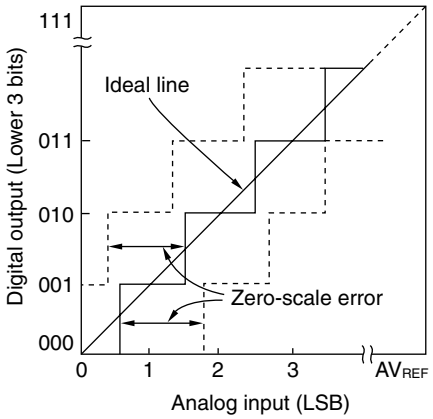


Figure 10-22. Full-Scale Error

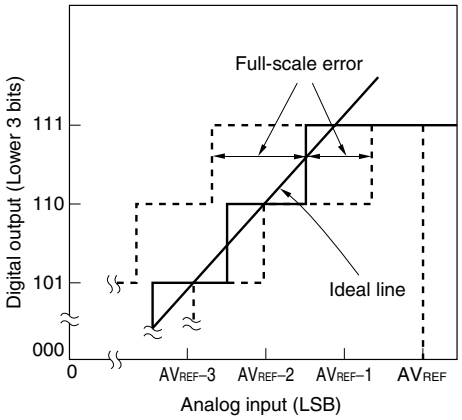


Figure 10-23. Integral Linearity Error

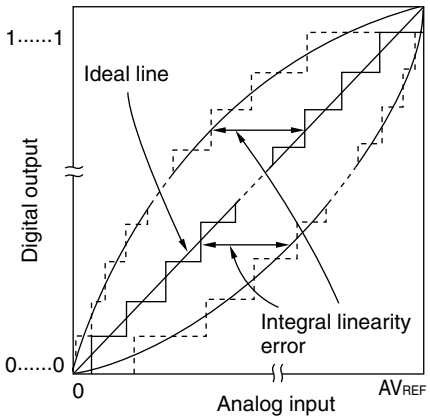
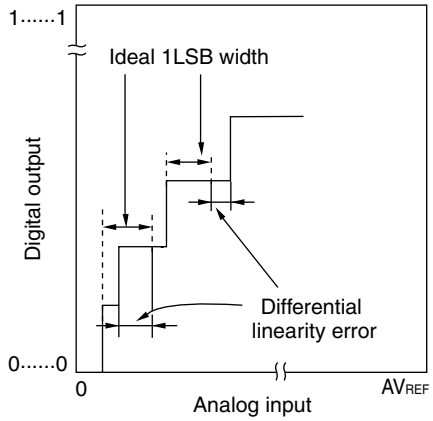


Figure 10-24. Differential Linearity Error



(8) Conversion time

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.

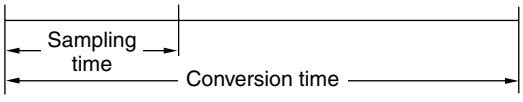


Figure 11-9. Format of Serial Status Register mn (SSRmn) (2/2)

Address: F0100H, F0101H (SSR00) to F0106H, F0107H (SSR03), F0144H, F0145H (SSR12), F0146H, F0147H (SSR13)

After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSRmn	0	0	0	0	0	0	0	0	0	TSF mn	BFF mn	0	0	FEF mn	PEF mn	OVF mn

FEF mn	Framing error detection flag of channel n
0	No error occurs.
1	A framing error occurs during UART reception. <Framing error cause> A framing error occurs if the stop bit is not detected upon completion of UART reception.
This is a cumulative flag and is not cleared until 1 is written to the FECTmn bit of the SIRmn register.	

PEF mn	Parity error detection flag of channel n
0	Error does not occur.
1	A parity error occurs during UART reception or ACK is not detected during I^2C transmission. <Parity error cause> • A parity error occurs if the parity of transmit data does not match the parity bit on completion of UART reception. • ACK is not detected if the ACK signal is not returned from the slave in the timing of ACK reception during I^2C transmission.
This is a cumulative flag and is not cleared until 1 is written to the PECTmn bit of the SIRmn register.	

OVF mn	Overrun error detection flag of channel n
0	No error occurs.
1	An overrun error occurs. <Causes of overrun error> • Receive data stored in the SDRmn register is not read and transmit data is written or the next receive data is written. • Transmit data is not ready for slave transmission or reception in the CSI mode.
This is a cumulative flag and is not cleared until 1 is written to the OVCTmn bit of the SIRmn register.	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 12, 13

(16) Port input mode registers 0 (PIM0)

This register set the input buffer of ports 0 in 1-bit units.

PIM0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 11-19. Format of Port Input Mode Registers 0 (PIM0)

Address F0040H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM0	0	0	0	PIM04	PIM03	0	0	0

PIM0n	P0n pin input buffer selection (n = 3, 4)
0	Normal input buffer
1	TTL input buffer

(17) Port output mode registers 0 (POM0)

This register set the output mode of ports 0 in 1-bit units.

POM0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

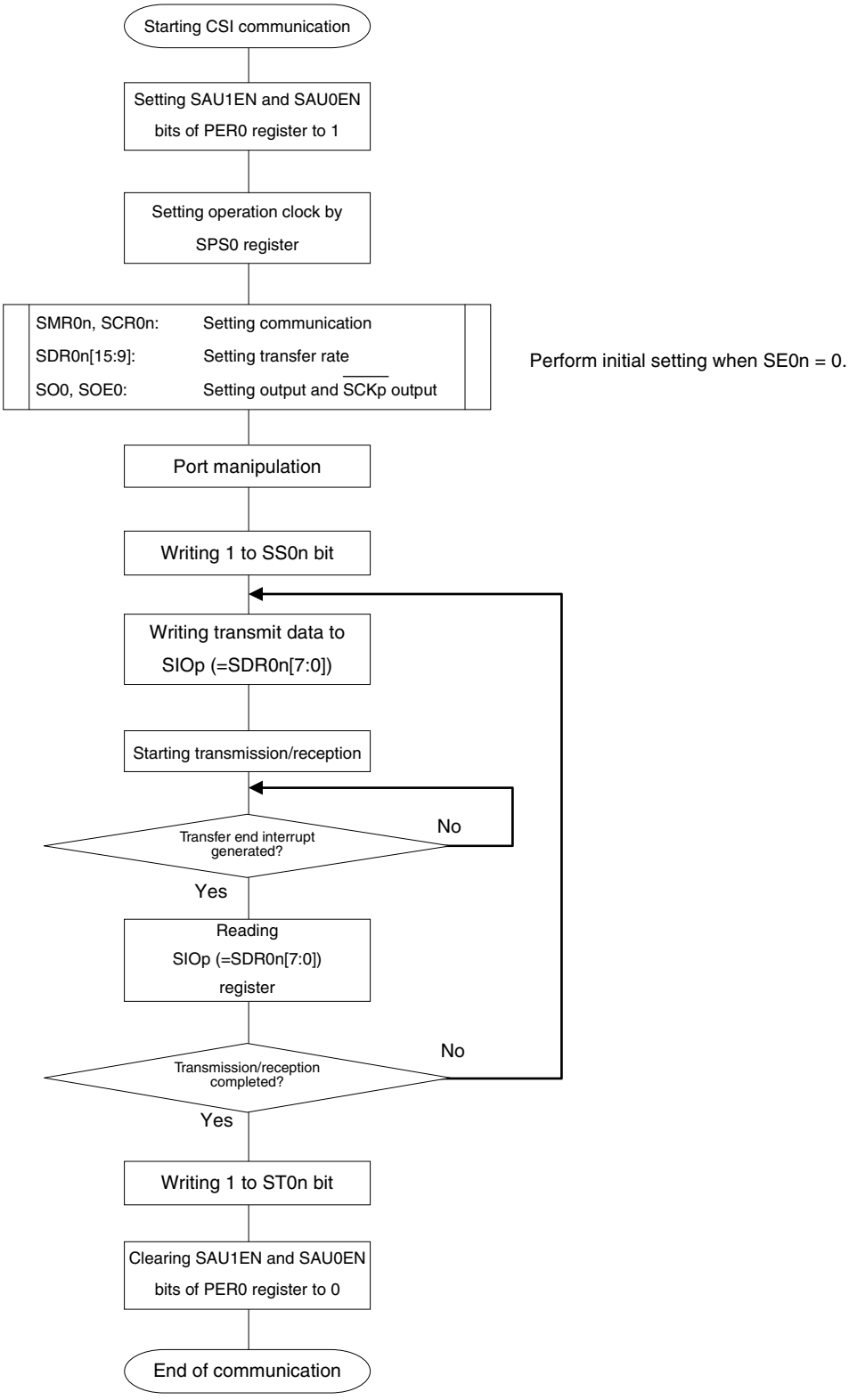
Figure 11-20. Format of Port Output Mode Registers 0 (POM0)

Address F0050H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
POM0	0	0	0	POM04	POM03	POM02	0	0

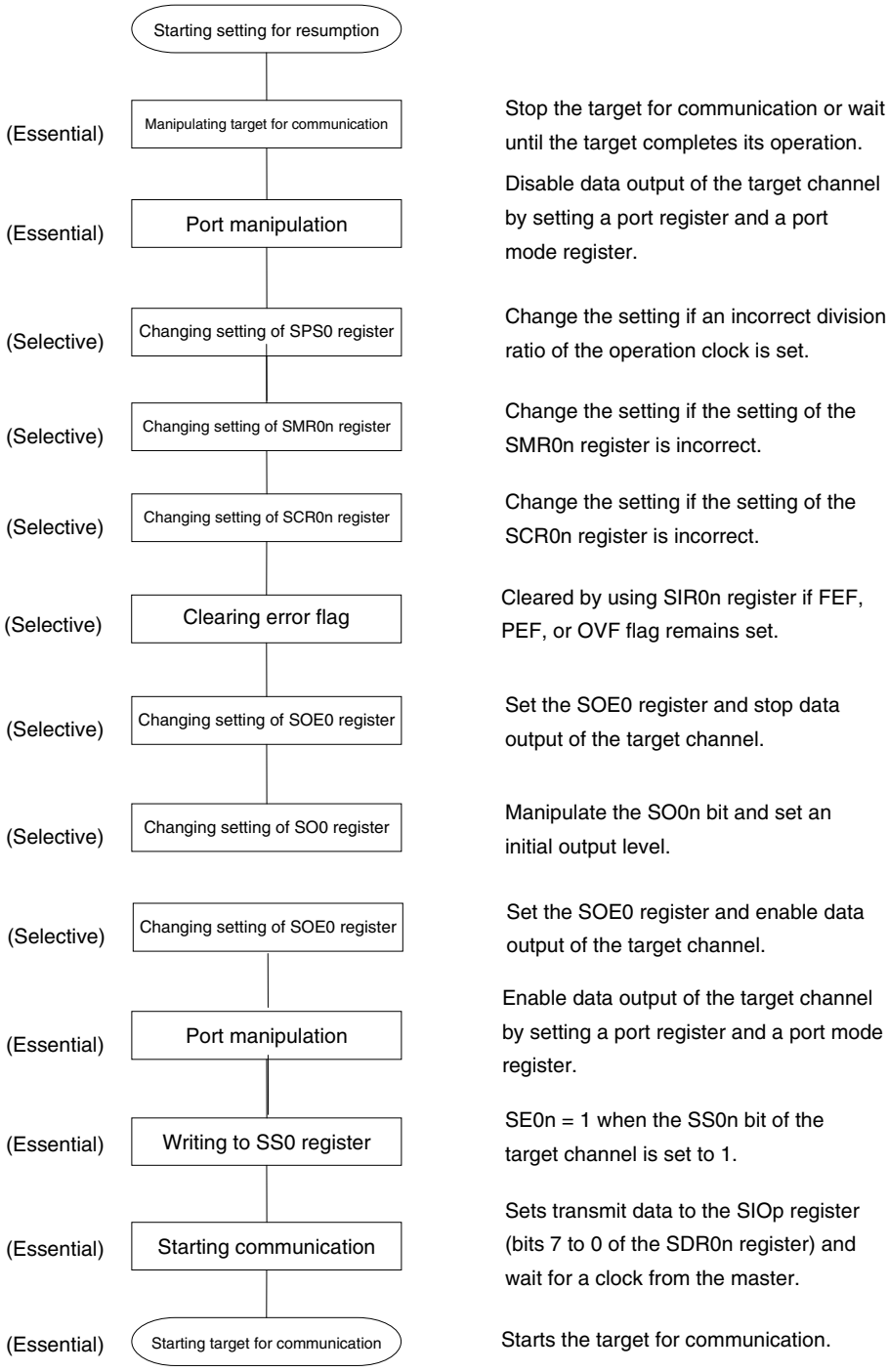
POM0n	P0n pin output buffer selection (n = 2 to 4)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance) mode

Figure 11-45. Flowchart of Master Transmission/Reception (in Single- Transmission/Reception Mode)



Caution After setting the PER0 register to 1, be sure to set the SPS0 register after 4 or more clocks have elapsed.

Figure 11-65. Procedure for Resuming Slave Transmission/Reception



<R> **Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.**

11.7.1 Address field transmission

Address field transmission is a transmission operation that first executes in I^2C communication to identify the target for transfer (slave). After a start condition is generated, an address (7 bits) and a transfer direction (1 bit) are transmitted in one frame.

Simplified I^2C	IIC10
Target channel	Channel 2 of SAU0
Pins used	SCL10, SDA10[Note]
Interrupt	INTIIC10
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)
Error detection flag	Parity error detection flag (PEF02)
Transfer data length	8 bits (transmitted with specifying the higher 7 bits as address and the least significant bit as R/W control)
<R> Transfer rate	Max. f_{MCK}/4 [Hz] (SDR02[15:9] = 1 or more) f_{MCK}: Operation clock (MCK) frequency of target channel However, the following condition must be satisfied in each mode of I^2C. • Max. 400 kHz (first mode) • Max. 100 kHz (standard mode)
Data level	Forward output (default: high level)
Parity bit	No parity bit
Stop bit	Appending 1 bit (for ACK reception timing)
Data direction	MSB first

Note To perform communication via simplified I^2C, set the N-ch open-drain output (V_{DD} tolerance) mode (POM03 = 1) for the port output mode registers (POM0) (see **4.3 Registers Controlling Port Function** for details). When communicating with an external device with a different potential, set the N-ch open-drain output (V_{DD} tolerance) mode (POM04 = 1) also for the clock input/output pins (SCL10) (see **4.4.4 Connecting to external device with different potential (2.5 V, 3 V)** for details).

Figure 12-6. Format of IIC Control Register 0 (IICC0) (2/4)

SPIE0[Note 1]	Enable/disable generation of interrupt request when stop condition is detected
0	Disable
1	Enable

Condition for clearing (SPIE0 = 0)	Condition for setting (SPIE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

WTIM0[Note 1]	Control of wait and interrupt request generation
0	Interrupt request is generated at the eighth clock's falling edge. Master mode: After output of eight clocks, clock output is set to low level and wait is set. Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.
1	Interrupt request is generated at the ninth clock's falling edge. Master mode: After output of nine clocks, clock output is set to low level and wait is set. Slave mode: After input of nine clocks, the clock is set to low level and wait is set for master device.

An interrupt is generated at the falling edge of the ninth clock during address transfer independently of the setting of this bit. The setting of this bit is valid when the address transfer is completed. When in master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after an acknowledge ($\overline{ACK}$) is issued. However, when the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.

Condition for clearing (WTIM0 = 0)	Condition for setting (WTIM0 = 1)
• Cleared by instruction • Reset	• Set by instruction

ACKE0[Notes 1, 2]	Acknowledgment control
0	Disable acknowledgment.
1	Enable acknowledgment. During the ninth clock period, the SDA0 line is set to low level.

Condition for clearing (ACKE0 = 0)	Condition for setting (ACKE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

Notes 1. The signal of this bit is invalid while IICE0 is 0. Set this bit during that period.

2. The set value is invalid during address transfer and if the code is not an extension code. When the device serves as a slave and the addresses match, an acknowledgment is generated regardless of the set value.

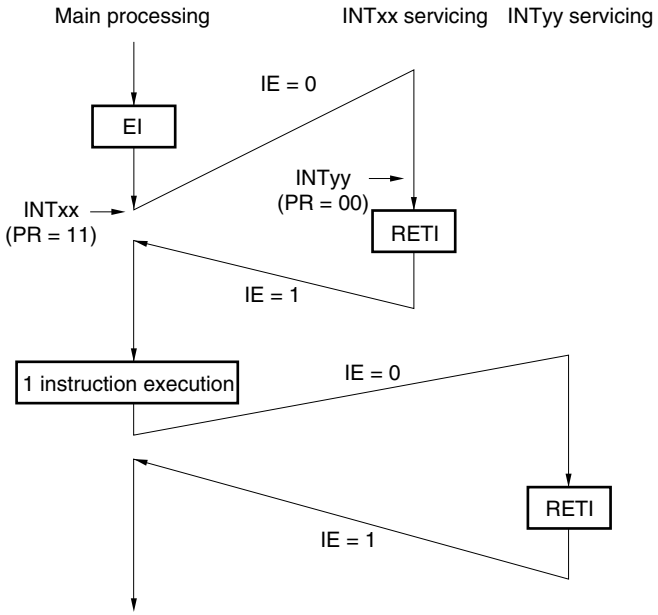
14.5.4 Consecutive capturing of A/D conversion results

A flowchart of an example of setting for consecutively capturing A/D conversion results is shown below.

- Consecutive capturing of A/D conversion results.
- DMA channel 1 is used for DMA transfer.
- DMA start source: INTAD
- Interrupt of A/D is specified by IFC13 to IFC10 (bits 3 to 0 of the DMC1 register) = 1100B.
- Transfers FFF1EH and FFF1FH (2 bytes) of the 10-bit A/D conversion result register to 2048 bytes of FF380H to FFB7FH of RAM.

Figure 15-10. Examples of Multiple Interrupt Servicing (2/2)

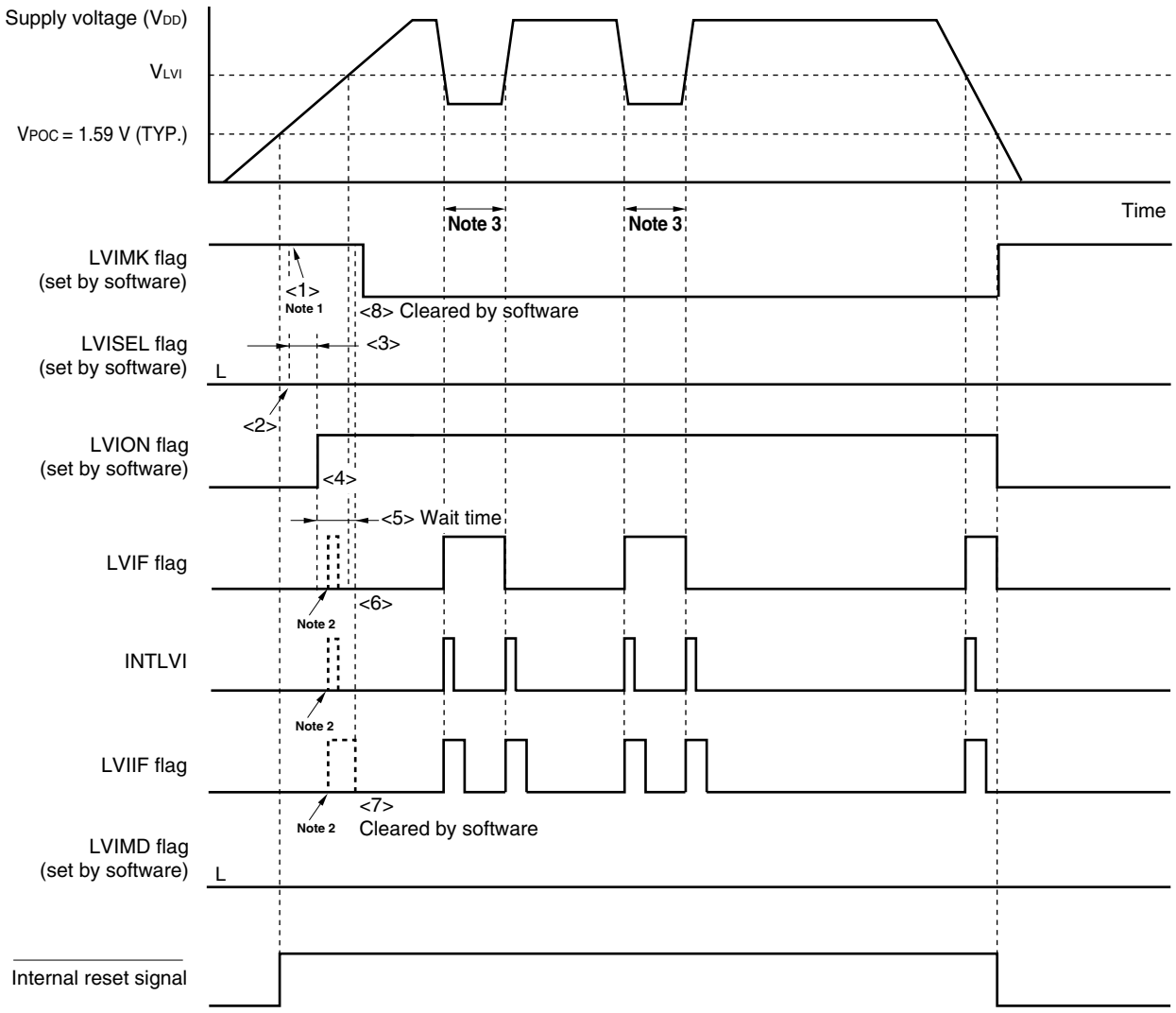
Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled



Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0
PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

Figure 20-8. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 0, Option Byte: LVIOFF = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVI operation is disabled when the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

Remark <1> to <8> in Figure 20-8 above correspond to <1> to <8> in the description of "When starting operation" in **20.4.2 (1) (a) When LVI Default Start Function Stopped Is Set (Option Byte: LVIOFF = 1).**

22.1.2 On-chip debug option byte (000C3H/ 010C3H)

- Control of on-chip debug operation
  - On-chip debug operation is disabled or enabled.
- Handling of data of flash memory in case of failure in on-chip debug security ID authentication
  - Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication.

Caution Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

22.2 Format of User Option Byte

The format of user option byte is shown below.

Figure 22-1. Format of User Option Byte (000C0H/010C0H) (1/2)

Address: 000C0H/010C0H[Note 1]

7	6	5	4	3	2	1	0
WDTINIT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON

WDTINIT	Use of interval interrupt of watchdog timer
0	Interval interrupt is not used.
1	Interval interrupt is generated when 75% of the overflow time is reached.

WINDOW1	WINDOW0	Watchdog timer window open period[Note 2]
0	0	25%
0	1	50%
1	0	75%
1	1	100%

WDTON	Operation control of watchdog timer counter
0	Counter operation disabled (counting stopped after reset)
1	Counter operation enabled (counting started after reset)

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time
0	0	0	$2^{10}/f_{IL}$ (3.88 ms)
0	0	1	$2^{11}/f_{IL}$ (7.76 ms)
0	1	0	$2^{12}/f_{IL}$ (15.52 ms)
0	1	1	$2^{13}/f_{IL}$ (31.03 ms)
1	0	0	$2^{15}/f_{IL}$ (124.12 ms)
1	0	1	$2^{17}/f_{IL}$ (496.48 ms)
1	1	0	$2^{18}/f_{IL}$ (992.97 ms)
1	1	1	$2^{20}/f_{IL}$ (3971.88 ms)

Table 26-5. Operation List (13/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Rotate	ROR	A, 1	2	1	–	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1	×
	ROL	A, 1	2	1	–	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1	×
	RORC	A, 1	2	1	–	(CY $\leftarrow A_0$, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1	×
	ROLC	A, 1	2	1	–	(CY $\leftarrow A_7$, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1	×
	ROLWC	AX,1	2	1	–	(CY $\leftarrow AX_{15}$, $AX_0 \leftarrow$ CY, $AX_{m+1} \leftarrow AX_m$) × 1	×
		BC,1	2	1	–	(CY $\leftarrow BC_{15}$, $BC_0 \leftarrow$ CY, $BC_{m+1} \leftarrow BC_m$) × 1	×
Bit manipulate	MOV1	CY, saddr.bit	3	1	–	CY ← (saddr).bit	×
		CY, sfr.bit	3	1	–	CY ← sfr.bit	×
		CY, A.bit	2	1	–	CY ← A.bit	×
		CY, PSW.bit	3	1	–	CY ← PSW.bit	×
		CY,[HL].bit	2	1	4	CY ← (HL).bit	×
		saddr.bit, CY	3	2	–	(saddr).bit ← CY	
		sfr.bit, CY	3	2	–	sfr.bit ← CY	
		A.bit, CY	2	1	–	A.bit ← CY	
		PSW.bit, CY	3	4	–	PSW.bit ← CY	× ×
		[HL].bit, CY	2	2	–	(HL).bit ← CY	
		CY, ES:[HL].bit	3	2	5	CY ← (ES, HL).bit	×
		ES:[HL].bit, CY	3	3	–	(ES, HL).bit ← CY	
	AND1	CY, saddr.bit	3	1	–	CY ← CY ∧ (saddr).bit	×
		CY, sfr.bit	3	1	–	CY ← CY ∧ sfr.bit	×
		CY, A.bit	2	1	–	CY ← CY ∧ A.bit	×
		CY, PSW.bit	3	1	–	CY ← CY ∧ PSW.bit	×
		CY,[HL].bit	2	1	4	CY ← CY ∧ (HL).bit	×
		CY, ES:[HL].bit	3	2	5	CY ← CY ∧ (ES, HL).bit	×
	OR1	CY, saddr.bit	3	1	–	CY ← CY ∨ (saddr).bit	×
		CY, sfr.bit	3	1	–	CY ← CY ∨ sfr.bit	×
		CY, A.bit	2	1	–	CY ← CY ∨ A.bit	×
		CY, PSW.bit	3	1	–	CY ← CY ∨ PSW.bit	×
		CY, [HL].bit	2	1	4	CY ← CY ∨ (HL).bit	×
		CY, ES:[HL].bit	3	2	5	CY ← CY ∨ (ES, HL).bit	×

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CLK}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

(5) XT1 oscillation: Crystal resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (kHz)	Load Capacitance CL (pF)	Recommended Circuit Constants			Oscillation Voltage Range	
					C3 (pF)	C4 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Seiko Instruments Inc.	SP-T2A	SMD	32.768	6.0	5	5	0	1.8	5.5
				12.5	18	18	0		
	SSP-T7	Small SMD		7.0	7	7	0		
				12.5	18	18	0		
	VT-200	Lead		6.0	5	5	0		
				12.5	18	18	0		
CITIZEN FINETECH MIYOTA CO., LTD.	CM200S	SMD	32.768	9.0	12	15	0	1.8	5.5
					12	15	100		
	CM315	SMD		9.0	15	15	0		
					15	15	100		
	CM519	SMD		9.0	15	12	0		
					15	12	100		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

<R> **When doing so, check the conditions for using the RMC register, and whether to enter or exit the STOP mode.**

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KE3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(6) XT1 oscillation: Crystal resonator (T_A = –20 to +70°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (kHz)	Load Capacitance CL (pF)	Recommended Circuit Constants			Oscillation Voltage Range	
					C3 (pF)	C4 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
CITIZEN FINETECH MIYOTA CO., LTD.	CFS-206	Lead	32.768	12.5	22	18	0	1.8	5.5
					22	18	100		
				9.0	12	15	0		
					12	15	100		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

<R> **When doing so, check the conditions for using the RMC register, and whether to enter or exit the STOP mode.**

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KE3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 17	Soft	Standby function	STOP mode	To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), temporarily switch the CPU clock to the internal high-speed oscillation clock before the execution of the STOP instruction. Before changing the CPU clock from the internal high-speed oscillation clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).	p.610 ☐
Chapter 18	Hard	Reset function	–	For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin. (If an external reset is effected upon power application, the period during which the supply voltage is outside the operating range (V_{DD} < 1.8 V) is not counted in the 10 μs. However, the low-level input may be continued before POC is released.)	p.615 ☐
				During reset input, the X1 clock, XT1 clock, internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input becomes invalid.	p.615 ☐
				When the STOP mode is released by a reset, the RAM contents in the STOP mode are held during reset input. However, because SFR and 2nd SFR are initialized, the port pins become high-impedance, except for P130, which is set to low-level output.	p.615 ☐
	Soft		Block diagram of reset function	An LVI circuit internal reset does not reset the LVI circuit.	p.616 ☐
			Watchdog timer overflow	A watchdog timer internal reset resets the watchdog timer.	p.617 ☐
			RESF: Reset control flag register	Do not read data by a 1-bit memory manipulation instruction.	p.623 ☐
				When the LVI default start function (bit 0 (LVIOFF) of 000C1H = 0) is used, LVIRF flag may become 1 from the beginning depending on the power-on waveform.	p.623 ☐
Chapter 19	Soft	Power-on-clear circuit	–	If the low-voltage detector (LVI) is set to ON by an option byte by default, the reset signal is not released until the supply voltage (V_{DD}) exceeds 2.07 V ±0.2 V.	pp.624, 625 ☐
				If an internal reset signal is generated in the POC circuit, the reset control flag register (RESF) is cleared to 00H.	p.624 ☐
			Timing of generation of internal reset signal (LVIOFF = 1)	Set the low-voltage detector by software after the reset status is released (see CHAPTER 20 LOW-VOLTAGE DETECTOR).	p.626 ☐
			Timing of generation of internal reset signal (LVIOFF = 0)	Set the low-voltage detector by software after the reset status is released (see CHAPTER 20 LOW-VOLTAGE DETECTOR).	p.627 ☐
			Cautions for power-on-clear circuit	In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the POC detection voltage (V_{POC}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.	p.628 ☐
Chapter 20	Soft	Low-voltage detector	LVIM: Low-voltage detection register	To stop LVI, follow either of the procedures below. • When using 8-bit memory manipulation instruction: Write 00H to LVIM. • When using 1-bit memory manipulation instruction: Clear LVION to 0.	p.633 ☐
	Hard			Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.	p.633 ☐

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Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 28	Soft	Electrical specifications ((A) grade products)	During communication at same potential (UART mode) (dedicated baud rate generator output)	When using UART1, select the normal input buffer for RxD1 and the normal output mode for TxD1 by using the PIM0 and POM0 registers.	p.784 □
			During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$... internal clock input)	When using CSI10, select the normal input buffer for SI10 and the normal output mode for SO10 and $\overline{SCK10}$ by using the PIM0 and POM0 registers.	p.785 □
			During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)	When using CSI10, select the normal input buffer for SI10 and $\overline{SCK10}$ and the normal output mode for SO10 by using the PIM0 and POM0 registers.	p.786 □
			During communication at same potential (simplified I^2C mode)	Select the normal input buffer and the N-ch open-drain output (V_{DD} tolerance) mode for SDA10 and the normal output mode for SCL10 by using the PIM0 and POM0 registers.	p.789 □
			During communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output)	Select the TTL input buffer for RxD1 and the N-ch open drain output (V_{DD} tolerance) mode for TxD1 by using the PIM0 and POM0 registers.	pp.790, 791, 793 □
			During communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCK10}$... internal clock output)	Select the TTL input buffer for SI10 and the N-ch open-drain output (V_{DD} tolerance) mode for SO10 and $\overline{SCK10}$ by using the PIM0 and POM0 registers.	pp.794 to 795, 796 □