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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	624
Number of Logic Elements/Cells	4992
Total RAM Bits	49152
Number of I/O	274
Number of Gates	257000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k100ebc356-1b

■ Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800

■ Flexible package options
  – Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see Tables 3 and 4)
  – SameFrame™ pin-out compatibility between FLEX 10KA and FLEX 10KE devices across a range of device densities and pin counts

■ Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 3. FLEX 10KE Package Options & I/O Pin Count   Notes (1), (2)

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
EPF10K30E	102	147		176		220			220 (3)
EPF10K50E	102	147	189	191		254			254 (3)
EPF10K50S	102	147	189	191	220	254			254 (3)
EPF10K100E		147	189	191	274	338			338 (3)
EPF10K130E			186		274	369		424	413
EPF10K200E							470	470	470
EPF10K200S			182		274	369	470	470	470

Notes:
(1) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), pin-grid array (PGA), and ball-grid array (BGA) packages.
(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.
(3) This option is supported with a 484-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin, 484-pin, and 672-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

Table 5. FLEX 10KE Performance

Application	Resources Used		Performance			Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit loadable counter	16	0	285	250	200	MHz
16-bit accumulator	16	0	285	250	200	MHz
16-to-1 multiplexer *(1)*	10	0	3.5	4.9	7.0	ns
16-bit multiplier with 3-stage pipeline *(2)*	592	0	156	131	93	MHz
256 × 16 RAM read cycle speed *(2)*	0	1	196	154	118	MHz
256 × 16 RAM write cycle speed *(2)*	0	1	185	143	106	MHz

Notes:

(1)   This application uses combinatorial inputs and outputs.

(2)   This application uses registered inputs and outputs.

Table 6 shows FLEX 10KE performance for more complex designs. These designs are available as Altera MegaCore® functions.

Table 6. FLEX 10KE Performance for Complex Designs

Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
8-bit, 16-tap parallel finite impulse response (FIR) filter	597	192	156	116	MSPS
8-bit, 512-point fast Fourier transform (FFT) function	1,854	23.4	28.7	38.9	μs *(1)*
		113	92	68	MHz
a16450 universal asynchronous receiver/transmitter (UART)	342	36	28	20.5	MHz

Note:

(1)   These values are for calculation time. Calculation time = number of clocks required/f_{max}. Number of clocks required = ceiling [log 2 (points)/2] × [points +14 + ceiling]

Functional Description

Each FLEX 10KE device contains an enhanced embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a four-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10KE devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 0.9 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 3.0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 9 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 9. FLEX 10KE Carry Chain Operation (n-Bit Full Adder)
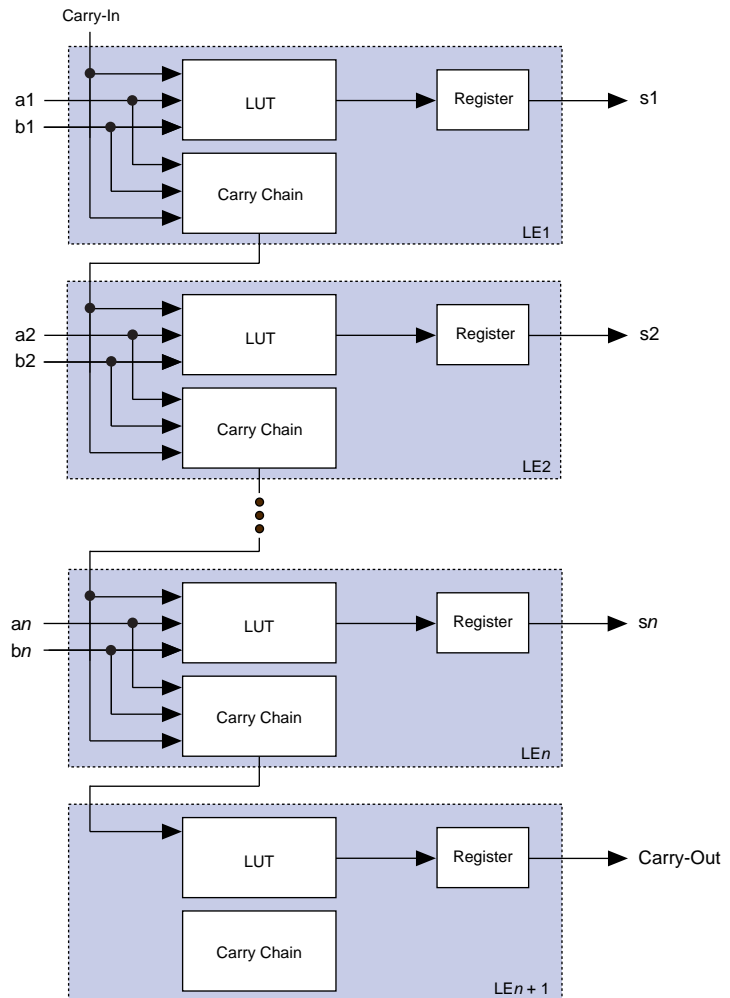
Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, so that asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

On all FLEX 10KE devices (except EPF10K50E and EPF10K200E devices), the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. EPF10K50S and EPF10K200S devices also support this feature. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across the device and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on a LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

ClockLock & ClockBoost Features

To support high-speed designs, FLEX 10KE devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

All FLEX 10KE devices, except EPF10K50E and EPF10K200E devices, support ClockLock and ClockBoost circuitry. EPF10K50S and EPF10K200S devices support this circuitry. Devices that support Clock-Lock and ClockBoost circuitry are distinguished with an "X" suffix in the ordering code; for instance, the EPF10K200SFC672-1X device supports this circuit.

The ClockLock and ClockBoost features in FLEX 10KE devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (GCLK1) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to the GCLK1 pin. In the Altera software, the GCLK1 pin can feed both the ClockLock and ClockBoost circuitry in the FLEX 10KE device. However, when both circuits are used, the other clock pin cannot be used.

Tables 12 and 13 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

Table 12. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		180	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		90	MHz
f_{CLKDEV}	Input deviation from user specification in the MAX+PLUS II software *(1)*				25,000 *(2)*	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(3)*				10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(4)*	$t_{INCLKSTB}$ < 100			250	ps
		$t_{INCLKSTB}$ < 50			200 *(4)*	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Figure 20 shows the timing requirements for the JTAG signals.

Figure 20. FLEX 10KE JTAG Waveforms
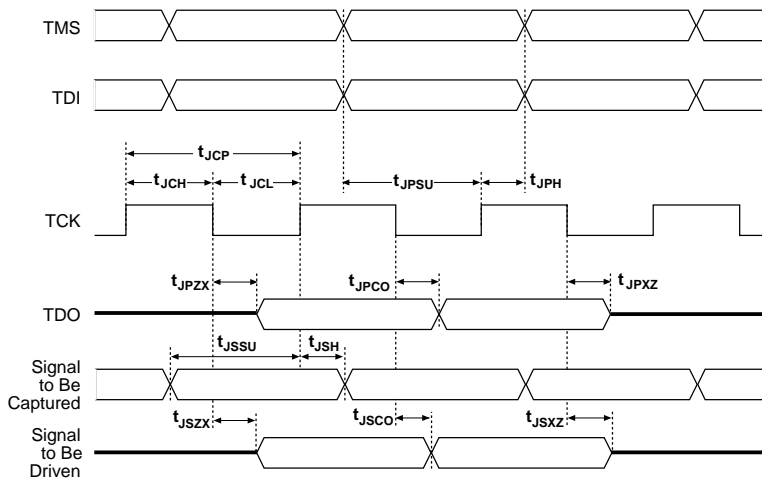
Table 18 shows the timing parameters and values for FLEX 10KE devices.

Symbol	Parameter	Min	Max	Unit
t_JCP	TCK clock period	100		ns
t_JCH	TCK clock high time	50		ns
t_JCL	TCK clock low time	50		ns
t_JPSU	JTAG port setup time	20		ns
t_JPH	JTAG port hold time	45		ns
t_JPCO	JTAG port clock to output		25	ns
t_JPZX	JTAG port high impedance to valid output		25	ns
t_JPXZ	JTAG port valid output to high impedance		25	ns
t_JSSU	Capture register setup time	20		ns
t_JSH	Capture register hold time	45		ns
t_JSCO	Update register clock to output		35	ns
t_JSZX	Update register high impedance to valid output		35	ns
t_JSXZ	Update register valid output to high impedance		35	ns

Table 18. FLEX 10KE JTAG Timing Parameters & Values

Figure 22 shows the required relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance.

Figure 22. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance
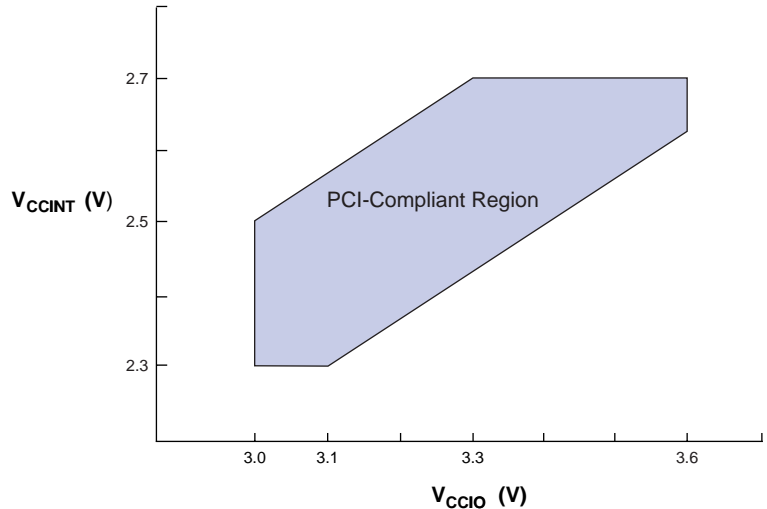
Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compliant to the 3.3-V *PCI Local Bus Specification*, *Revision 2.2* (when VCCIO pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the *PCI Local Bus Specification*, *Revision 2.2* (when VCCINT pins are powered with a minimum supply of 2.375 V, and VCCIO pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

Table 24. LE Timing Microparameters (Part 2 of 2)   Note (1)

Symbol	Parameter	Condition
t_{CLR}	LE register clear delay	
t_{CH}	Minimum clock high time from clock pin	
t_{CL}	Minimum clock low time from clock pin	

Table 25. IOE Timing Microparameters   Note (1)

Symbol	Parameter	Conditions
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
t_{IOH}	IOE register hold time for data and enable signals after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF (2)
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF (3)
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF (2)
t_{ZX2}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF (3)
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Symbol	Parameter	Conditions
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
t_{EABWEH}	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Table 27. EAB Timing Macroparameters *Note (1), (6)*

Table 34. EPF10K30E Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		6.4		7.6		8.8	ns
$t_{EABRCOMB}$	6.4		7.6		8.8		ns
$t_{EABRCREG}$	4.4		5.1		6.0		ns
t_{EABWP}	2.5		2.9		3.3		ns
$t_{EABWCOMB}$	6.0		7.0		8.0		ns
$t_{EABWCREG}$	6.8		7.8		9.0		ns
t_{EABDD}		5.7		6.7		7.7	ns
$t_{EABDATACO}$		0.8		0.9		1.1	ns
$t_{EABDATASU}$	1.5		1.7		2.0		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.3		1.4		1.7		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.5		1.7		2.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.0		3.6		4.3		ns
t_{EABWAH}	0.5		0.5		0.4		ns
t_{EABWO}		5.1		6.0		6.8	ns

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Table 53. EPF10K130E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{OD3}		4.0		5.6		7.5	ns
t_{XZ}		2.8		4.1		5.5	ns
t_{ZX1}		2.8		4.1		5.5	ns
t_{ZX2}		2.8		4.1		5.5	ns
t_{ZX3}		4.0		5.6		7.5	ns
t_{INREG}		2.5		3.0		4.1	ns
t_{IOFD}		0.4		0.5		0.6	ns
t_{INCOMB}		0.4		0.5		0.6	ns

Table 54. EPF10K130E Device EAB Internal Microparameters *(Part 1 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		2.0		2.6	ns
$t_{EABDATA2}$		0.0		0.0		0.0	ns
t_{EABWE1}		1.5		2.0		2.6	ns
t_{EABWE2}		0.3		0.4		0.5	ns
t_{EABRE1}		0.3		0.4		0.5	ns
t_{EABRE2}		0.0		0.0		0.0	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.4		0.5	ns
$t_{EABBYPASS}$		0.1		0.1		0.2	ns
t_{EABSU}	0.8		1.0		1.4		ns
t_{EABH}	0.1		0.2		0.2		ns
t_{EABCLR}	0.3		0.4		0.5		ns
t_{AA}		4.0		5.0		6.6	ns
t_{WP}	2.7		3.5		4.7		ns
t_{RP}	1.0		1.3		1.7		ns
t_{WDSU}	1.0		1.3		1.7		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	1.6		2.1		2.8		ns
t_{WAH}	1.6		2.1		2.8		ns
t_{RASU}	3.0		3.9		5.2		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		1.5		2.0		2.6	ns

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Table 54. EPF10K130E Device EAB Internal Microparameters (Part 2 of 2)   *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DD}		1.5		2.0		2.6	ns
t_{EABOUT}		0.2		0.3		0.3	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.7		3.5		4.7		ns

Table 55. EPF10K130E Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.9		7.5		9.9	ns
t_{EABRCOMB}	5.9		7.5		9.9		ns
t_{EABRCREG}	5.1		6.4		8.5		ns
t_{EABWP}	2.7		3.5		4.7		ns
t_{EABWCOMB}	5.9		7.7		10.3		ns
t_{EABWCREG}	5.4		7.0		9.4		ns
t_{EABDD}		3.4		4.5		5.9	ns
t_{EABDATACO}		0.5		0.7		0.8	ns
t_{EABDATASU}	0.8		1.0		1.4		ns
t_{EABDATAH}	0.1		0.1		0.2		ns
t_{EABWESU}	1.1		1.4		1.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
t_{EABWDSU}	1.0		1.3		1.7		ns
t_{EABWDH}	0.2		0.2		0.3		ns
t_{EABWASU}	4.1		5.1		6.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		3.4		4.5		5.9	ns

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 2 of 2)   *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABWCOMB}	6.7		8.1		10.7		ns
t_{EABWCREG}	6.6		8.0		10.6		ns
t_{EABDD}		4.0		5.1		6.7	ns
t_{EABDATACO}		0.8		1.0		1.3	ns
t_{EABDATASU}	1.3		1.6		2.1		ns
t_{EABDATAH}	0.0		0.0		0.0		ns
t_{EABWESU}	0.9		1.1		1.5		ns
t_{EABWEH}	0.4		0.5		0.6		ns
t_{EABWDSU}	1.5		1.8		2.4		ns
t_{EABWDH}	0.0		0.0		0.0		ns
t_{EABWASU}	3.0		3.6		4.7		ns
t_{EABWAH}	0.4		0.5		0.7		ns
t_{EABWO}		3.4		4.4		5.8	ns

Table 63. EPF10K200E Device Interconnect Timing Microparameters   *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DIN2IOE}		4.2		4.6		5.7	ns
t_{DIN2LE}		1.7		1.7		2.0	ns
t_{DIN2DATA}		1.9		2.1		3.0	ns
t_{DCLK2IOE}		2.5		2.9		4.0	ns
t_{DCLK2LE}		1.7		1.7		2.0	ns
t_{SAMELAB}		0.1		0.1		0.2	ns
t_{SAMEROW}		2.3		2.6		3.6	ns
t_{SAMECOLUMN}		2.5		2.7		4.1	ns
t_{DIFFROW}		4.8		5.3		7.7	ns
t_{TWOROWS}		7.1		7.9		11.3	ns
t_{LEPERIPH}		7.0		7.6		9.0	ns
t_{LABCARRY}		0.1		0.1		0.2	ns
t_{LABCASC}		0.9		1.0		1.4	ns

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Table 64. EPF10K200E External Timing Parameters   Notes (1), (2)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		10.0		12.0		16.0	ns
t_{INSU}	2.8		3.4		4.4		ns
t_{INH}	0.0		0.0		0.0		ns
t_{OUTCO}	2.0	4.5	2.0	5.3	2.0	7.8	ns
t_{PCISU}	3.0		6.2		-		ns
t_{PCIH}	0.0		0.0		-		ns
t_{PCICO}	2.0	6.0	2.0	8.9	-	-	ns

Table 65. EPF10K200E External Bidirectional Timing Parameters   Notes (1), (2)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSUBIDIR}	3.0		4.0		5.5		ns
t_{INHBIDIR}	0.0		0.0		0.0		ns
t_{OUTCOBIDIR}	2.0	4.5	2.0	5.3	2.0	7.8	ns
t_{XZBIDIR}		8.1		9.5		13.0	ns
t_{ZXBIDIR}		8.1		9.5		13.0	ns

Notes to tables:

(1)   All timing parameters are described in Tables 24 through 30 in this data sheet.

(2)   These parameters are specified by characterization.

Tables 66 through 79 show EPF10K50S and EPF10K200S device external timing parameters.

Table 66. EPF10K50S Device LE Timing Microparameters (Part 1 of 2)   Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.6		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		0.9	ns
t_{PACKED}		0.2		0.3		0.4	ns
t_{EN}		0.6		0.7		0.9	ns
t_{CICO}		0.1		0.1		0.1	ns
t_{CGEN}		0.4		0.5		0.6	ns

Table 68. EPF10K50S Device EAB Internal Microparameters Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.4		3.2	ns
$t_{EABDATA2}$		0.4		0.6		0.8	ns
t_{EABWE1}		1.0		1.4		1.9	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0.0		0.0		0.0	
t_{EABRE2}		0.4		0.6		0.8	
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		1.1		1.5	ns
$t_{EABBYPASS}$		0.0		0.0		0.0	ns
t_{EABSU}	0.7		1.0		1.3		ns
t_{EABH}	0.4		0.6		0.8		ns
t_{EABCLR}	0.8		1.1		1.5		
t_{AA}		2.0		2.8		3.8	ns
t_{WP}	2.0		2.8		3.8		ns
t_{RP}	1.0		1.4		1.9		
t_{WDSU}	0.5		0.7		0.9		ns
t_{WDH}	0.1		0.1		0.2		ns
t_{WASU}	1.0		1.4		1.9		ns
t_{WAH}	1.5		2.1		2.9		ns
t_{RASU}	1.5		2.1		2.8		
t_{RAH}	0.1		0.1		0.2		
t_{WO}		2.1		2.9		4.0	ns
t_{DD}		2.1		2.9		4.0	ns
t_{EABOUT}		0.0		0.0		0.0	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	1.5		2.0		2.5		ns

Table 73. EPF10K200S Device Internal & External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.2	ns
t_{CLUT}		0.4		0.5		0.6	ns
t_{RLUT}		0.5		0.7		0.9	ns
t_{PACKED}		0.4		0.5		0.7	ns
t_{EN}		0.6		0.5		0.6	ns
t_{CICO}		0.1		0.2		0.3	ns
t_{CGEN}		0.3		0.4		0.6	ns
t_{CGENR}		0.1		0.2		0.3	ns
t_{CASC}		0.7		0.8		1.2	ns
t_C		0.5		0.6		0.8	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.3		0.6		0.8	ns
t_{SU}	0.4		0.6		0.7		ns
t_H	1.0		1.1		1.5		ns
t_{PRE}		0.4		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 74. EPF10K200S Device IOE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.8		1.9		2.6	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		1.7		1.9		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		0.9		1.2		ns
t_{IOH}	0.4		0.8		1.1		ns
t_{IOCLR}		0.2		0.2		0.3	ns
t_{OD1}		1.3		0.7		0.9	ns
t_{OD2}		0.8		0.2		0.4	ns
t_{OD3}		2.9		3.0		3.9	ns
t_{XZ}		5.0		5.3		7.1	ns
t_{ZX1}		5.0		5.3		7.1	ns

Table 76. EPF10K200S Device EAB Internal Timing Macroparameters   *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		3.9		6.4		8.4	ns
t_{EABRCOMB}	3.9		6.4		8.4		ns
t_{EABRCREG}	3.6		5.7		7.6		ns
t_{EABWP}	2.1		4.0		5.3		ns
t_{EABWCOMB}	4.8		8.1		10.7		ns
t_{EABWCREG}	5.4		8.0		10.6		ns
t_{EABDD}		3.8		5.1		6.7	ns
t_{EABDATACO}		0.8		1.0		1.3	ns
t_{EABDATASU}	1.1		1.6		2.1		ns
t_{EABDATAH}	0.0		0.0		0.0		ns
t_{EABWESU}	0.7		1.1		1.5		ns
t_{EABWEH}	0.4		0.5		0.6		ns
t_{EABWDSU}	1.2		1.8		2.4		ns
t_{EABWDH}	0.0		0.0		0.0		ns
t_{EABWASU}	1.9		3.6		4.7		ns
t_{EABWAH}	0.8		0.5		0.7		ns
t_{EABWO}		3.1		4.4		5.8	ns

Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 1 of 2)   *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DIN2IOE}		4.4		4.8		5.5	ns
t_{DIN2LE}		0.6		0.6		0.9	ns
t_{DIN2DATA}		1.8		2.1		2.8	ns
t_{DCLK2IOE}		1.7		2.0		2.8	ns
t_{DCLK2LE}		0.6		0.6		0.9	ns
t_{SAMELAB}		0.1		0.1		0.2	ns
t_{SAMEROW}		3.0		4.6		5.7	ns
t_{SAMECOLUMN}		3.5		4.9		6.4	ns
t_{DIFFROW}		6.5		9.5		12.1	ns
t_{TWOROWS}		9.5		14.1		17.8	ns
t_{LEPERIPH}		5.5		6.2		7.2	ns
t_{LABCARRY}		0.3		0.1		0.2	ns