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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	624
Number of Logic Elements/Cells	4992
Total RAM Bits	49152
Number of I/O	274
Number of Gates	257000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf10k100ebc356-2x

Table 2. FLEX 10KE Device Features

Feature	EPF10K100E *(2)*	EPF10K130E	EPF10K200E EPF10K200S
Typical gates *(1)*	100,000	130,000	200,000
Maximum system gates	257,000	342,000	513,000
Logic elements (LEs)	4,992	6,656	9,984
EABs	12	16	24
Total RAM bits	49,152	65,536	98,304
Maximum user I/O pins	338	413	470

Note to tables:
(1) The embedded IEEE Std. 1149.1 JTAG circuitry adds up to 31,250 gates in addition to the listed typical or maximum system gates.
(2) New EPF10K100B designs should use EPF10K100E devices.

…and More Features

- – Fabricated on an advanced process and operate with a 2.5-V internal supply voltage
- – In-circuit reconfigurability (ICR) via external configuration devices, intelligent controller, or JTAG port
- – ClockLock™ and ClockBoost™ options for reduced clock delay/skew and clock multiplication
- – Built-in low-skew clock distribution trees
- – 100% functional testing of all devices; test vectors or scan chains are not required
- – Pull-up on I/O pins before and during configuration
- ■ Flexible interconnect
  - – FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - – Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - – Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - – Tri-state emulation that implements internal tri-state buses
  - – Up to six global clock signals and four global clear signals
- ■ Powerful I/O pins
  - – Individual tri-state output enable control for each pin
  - – Open-drain option on each I/O pin
  - – Programmable output slew-rate control to reduce switching noise
  - – Clamp to V_{CCIO} user-selectable on a pin-by-pin basis
  - – Supports hot-socketing

Table 4. FLEX 10KE Package Sizes

| Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	–	1.27	1.0
Area (mm²)	484	936	1,197	289	1,225	529	3,904	2,025	729
Length × width (mm × mm)	22 × 22	30.6 × 30.6	34.6 × 34.6	17 × 17	35 × 35	23 × 23	62.5 × 62.5	45 × 45	27 × 27

General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

The EAB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3.

Figure 3. FLEX 10KE EAB in Dual-Port RAM Mode
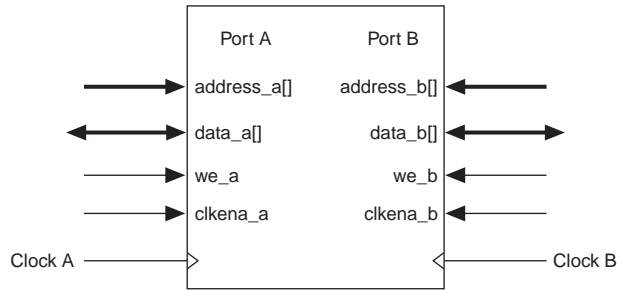
The FLEX 10KE EAB can be used in a single-port mode, which is useful for backward-compatibility with FLEX 10K designs (see Figure 4).

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 4). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see Figure 7).

Figure 9 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 9. FLEX 10KE Carry Chain Operation (n-Bit Full Adder)
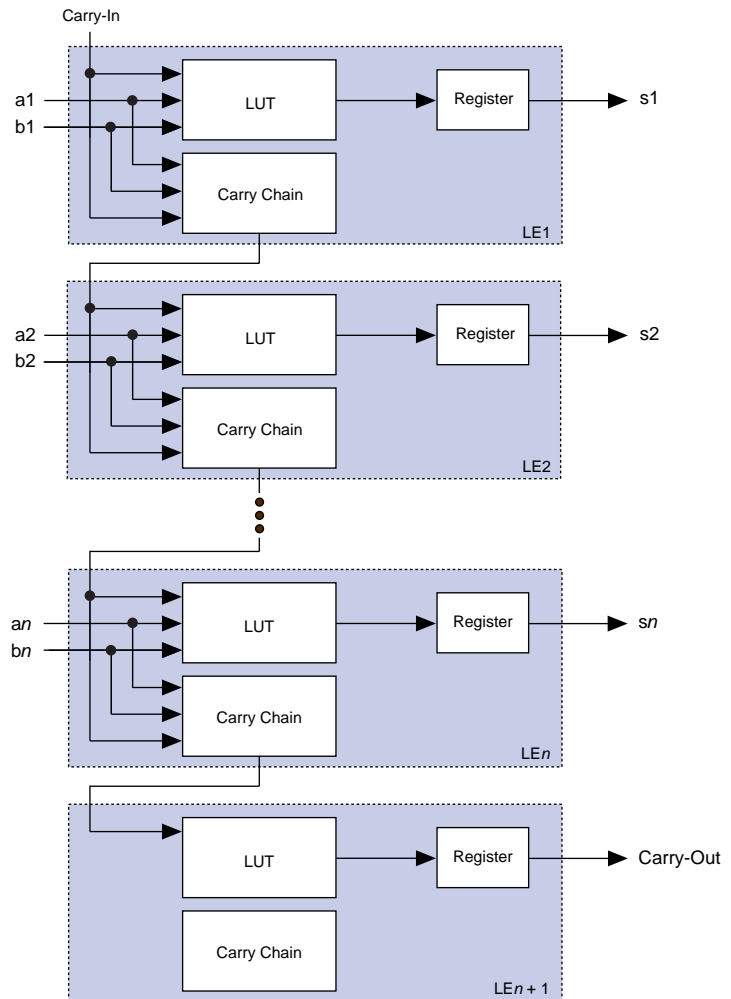
Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Altera Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect routing structure at the same time.

The LUT and the register in the LE can be used independently (register packing). To support register packing, the LE has two outputs; one drives the local interconnect, and the other drives the FastTrack Interconnect routing structure. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect routing structure while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 11 on page 22, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals without using the LUT resources.

On all FLEX 10KE devices (except EPF10K50E and EPF10K200E devices), the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. EPF10K50S and EPF10K200S devices also support this feature. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across the device and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on a LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Tables 8 and 9 list the sources for each peripheral control signal, and show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. The tables also show the rows that can drive global signals.

Table 8. Peripheral Bus Sources for EPF10K30E, EPF10K50E & EPF10K50S Devices

Peripheral Control Signal	EPF10K30E	EPF10K50E EPF10K50S
OE0	Row A	Row A
OE1	Row B	Row B
OE2	Row C	Row D
OE3	Row D	Row F
OE4	Row E	Row H
OE5	Row F	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A
CLKENA1/OE6/GLOBAL1	Row B	Row C
CLKENA2/CLR0	Row C	Row E
CLKENA3/OE7/GLOBAL2	Row D	Row G
CLKENA4/CLR1	Row E	Row I
CLKENA5/CLK1/GLOBAL3	Row F	Row J

SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K200S device in a 672-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 18).

Figure 18. SameFrame Pin-Out Example

Printed Circuit Board
Designed for 672-Pin FineLine BGA Package

100-Pin
FineLine
BGA

256-Pin
FineLine
BGA

256-Pin FineLine BGA Package
(Reduced I/O Count or
Logic Requirements)

672-Pin FineLine BGA Package
(Increased I/O Count or
Logic Requirements)
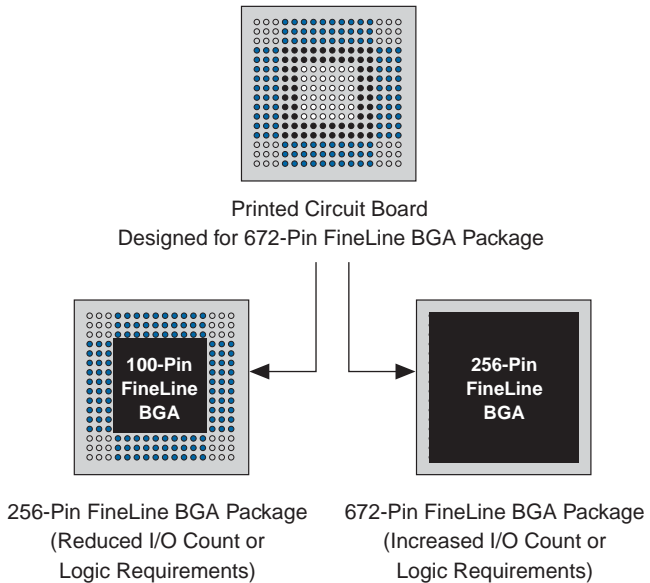
Timing simulation and delay prediction are available with the Altera Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10KE device.

Figure 24. FLEX 10KE Device Timing Model
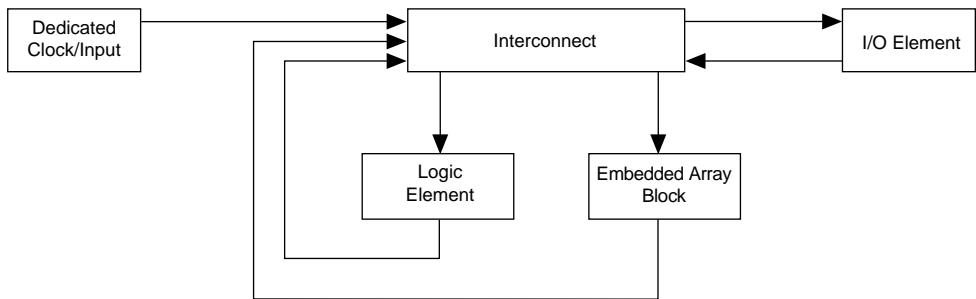
Figures 25 through 28 show the delays that correspond to various paths and functions within the LE, IOE, EAB, and bidirectional timing models.

Figure 25. FLEX 10KE Device LE Timing Model

Table 24. LE Timing Microparameters (Part 2 of 2)   Note (1)

Symbol	Parameter	Condition
t_{CLR}	LE register clear delay	
t_{CH}	Minimum clock high time from clock pin	
t_{CL}	Minimum clock low time from clock pin	

Table 25. IOE Timing Microparameters   Note (1)

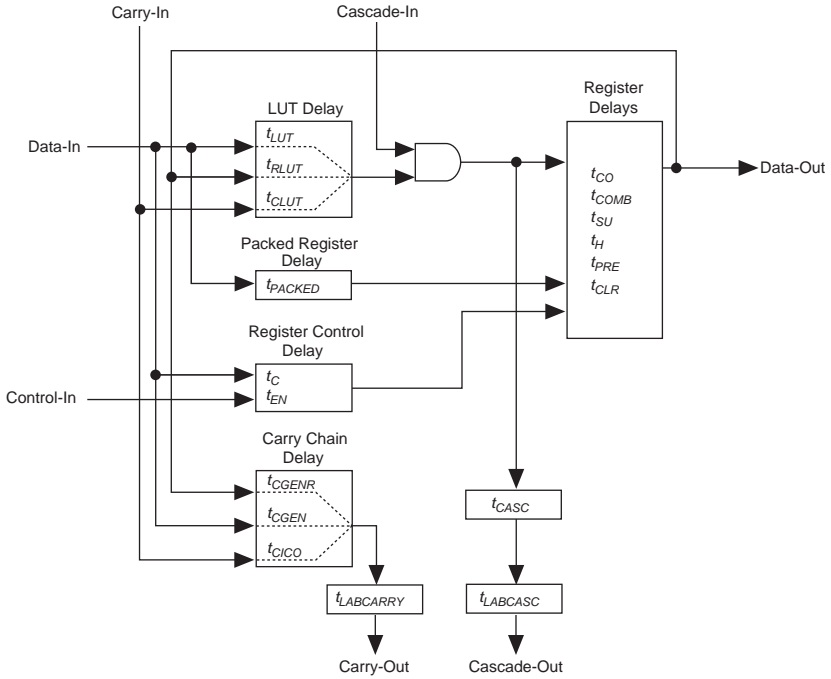| Symbol	Parameter	Conditions
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
t_{IOH}	IOE register hold time for data and enable signals after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF (2)
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF (3)
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF (2)
t_{ZX2}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF (3)
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Figure 30. EAB Synchronous Timing Waveforms

EAB Synchronous Read
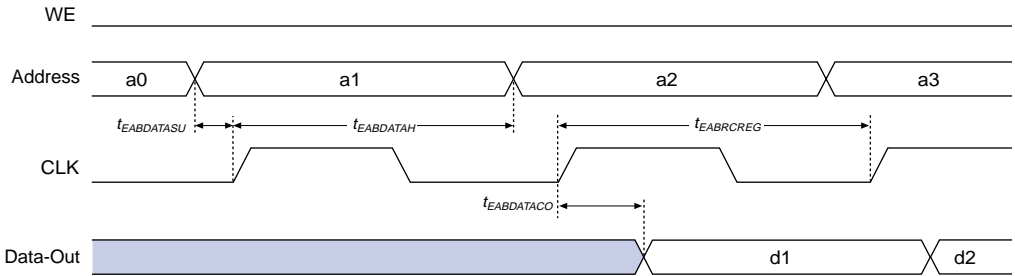
EAB Synchronous Write (EAB Output Registers Used)
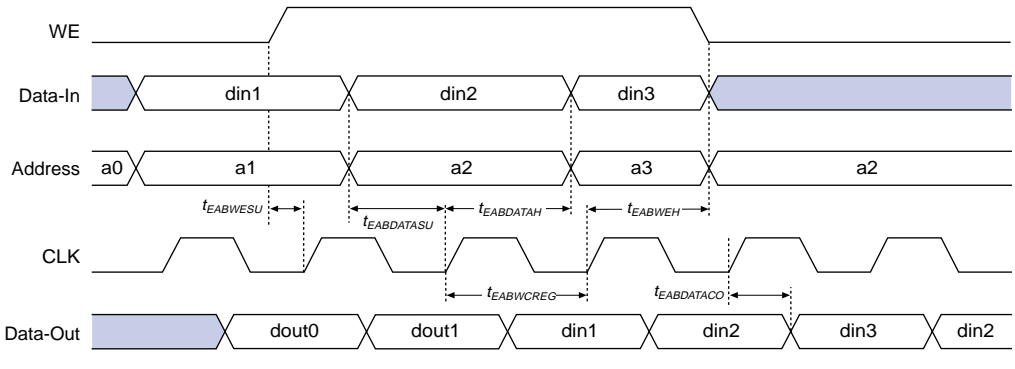
Tables 31 through 37 show EPF10K30E device internal and external timing parameters.

Table 31. EPF10K30E Device LE Timing Microparameters (Part 1 of 2)   Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns

Table 37. EPF10K30E External Bidirectional Timing Parameters   *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{INSUBIDIR}$ (3)	2.8		3.9		5.2		ns
t$_{INHBIDIR}$ (3)	0.0		0.0		0.0		ns
t$_{INSUBIDIR}$ (4)	3.8		4.9		–		ns
t$_{INHBIDIR}$ (4)	0.0		0.0		–		ns
t$_{OUTCOBIDIR}$ (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
t$_{XZBIDIR}$ (3)		6.1		7.5		9.7	ns
t$_{ZXBIDIR}$ (3)		6.1		7.5		9.7	ns
t$_{OUTCOBIDIR}$ (4)	0.5	3.9	0.5	4.9	–	–	ns
t$_{XZBIDIR}$ (4)		5.1		6.5		–	ns
t$_{ZXBIDIR}$ (4)		5.1		6.5		–	ns

Notes to tables:

(1)   All timing parameters are described in Tables 24 through 30 in this data sheet.

(2)   These parameters are specified by characterization.

(3)   This parameter is measured without the use of the ClockLock or ClockBoost circuits.

(4)   This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 38 through 44 show EPF10K50E device internal and external timing parameters.

Table 38. EPF10K50E Device LE Timing Microparameters (Part 1 of 2)   *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{LUT}$		0.6		0.9		1.3	ns
t$_{CLUT}$		0.5		0.6		0.8	ns
t$_{RLUT}$		0.7		0.8		1.1	ns
t$_{PACKED}$		0.4		0.5		0.6	ns
t$_{EN}$		0.6		0.7		0.9	ns
t$_{CICO}$		0.2		0.2		0.3	ns
t$_{CGEN}$		0.5		0.5		0.8	ns
t$_{CGENR}$		0.2		0.2		0.3	ns
t$_{CASC}$		0.8		1.0		1.4	ns
t$_C$		0.5		0.6		0.8	ns
t$_{CO}$		0.7		0.7		0.9	ns
t$_{COMB}$		0.5		0.6		0.8	ns
t$_{SU}$	0.7		0.7		0.8		ns

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Table 50. EPF10K100E External Timing Parameters   *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{DRR}$		9.0		12.0		16.0	ns
t$_{INSU}$ *(3)*	2.0		2.5		3.3		ns
t$_{INH}$ *(3)*	0.0		0.0		0.0		ns
t$_{OUTCO}$ *(3)*	2.0	5.2	2.0	6.9	2.0	9.1	ns
t$_{INSU}$ *(4)*	2.0		2.2		–		ns
t$_{INH}$ *(4)*	0.0		0.0		–		ns
t$_{OUTCO}$ *(4)*	0.5	3.0	0.5	4.6	–	–	ns
t$_{PCISU}$	3.0		6.2		–		ns
t$_{PCIH}$	0.0		0.0		–		ns
t$_{PCICO}$	2.0	6.0	2.0	6.9	–	–	ns

Table 51. EPF10K100E External Bidirectional Timing Parameters   *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{INSUBIDIR}$ *(3)*	1.7		2.5		3.3		ns
t$_{INHBIDIR}$ *(3)*	0.0		0.0		0.0		ns
t$_{INSUBIDIR}$ *(4)*	2.0		2.8		–		ns
t$_{INHBIDIR}$ *(4)*	0.0		0.0		–		ns
t$_{OUTCOBIDIR}$ *(3)*	2.0	5.2	2.0	6.9	2.0	9.1	ns
t$_{XZBIDIR}$ *(3)*		5.6		7.5		10.1	ns
t$_{ZXBIDIR}$ *(3)*		5.6		7.5		10.1	ns
t$_{OUTCOBIDIR}$ *(4)*	0.5	3.0	0.5	4.6	–	–	ns
t$_{XZBIDIR}$ *(4)*		4.6		6.5		–	ns
t$_{ZXBIDIR}$ *(4)*		4.6		6.5		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Table 64. EPF10K200E External Timing Parameters   Notes (1), (2)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		10.0		12.0		16.0	ns
t_{INSU}	2.8		3.4		4.4		ns
t_{INH}	0.0		0.0		0.0		ns
t_{OUTCO}	2.0	4.5	2.0	5.3	2.0	7.8	ns
t_{PCISU}	3.0		6.2		-		ns
t_{PCIH}	0.0		0.0		-		ns
t_{PCICO}	2.0	6.0	2.0	8.9	-	-	ns

Table 65. EPF10K200E External Bidirectional Timing Parameters   Notes (1), (2)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSUBIDIR}	3.0		4.0		5.5		ns
t_{INHBIDIR}	0.0		0.0		0.0		ns
t_{OUTCOBIDIR}	2.0	4.5	2.0	5.3	2.0	7.8	ns
t_{XZBIDIR}		8.1		9.5		13.0	ns
t_{ZXBIDIR}		8.1		9.5		13.0	ns

Notes to tables:

(1)   All timing parameters are described in Tables 24 through 30 in this data sheet.

(2)   These parameters are specified by characterization.

Tables 66 through 79 show EPF10K50S and EPF10K200S device external timing parameters.

Table 66. EPF10K50S Device LE Timing Microparameters (Part 1 of 2)   Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.6		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		0.9	ns
t_{PACKED}		0.2		0.3		0.4	ns
t_{EN}		0.6		0.7		0.9	ns
t_{CICO}		0.1		0.1		0.1	ns
t_{CGEN}		0.4		0.5		0.6	ns

Table 68. EPF10K50S Device EAB Internal Microparameters Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.4		3.2	ns
$t_{EABDATA2}$		0.4		0.6		0.8	ns
t_{EABWE1}		1.0		1.4		1.9	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0.0		0.0		0.0	
t_{EABRE2}		0.4		0.6		0.8	
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		1.1		1.5	ns
$t_{EABBYPASS}$		0.0		0.0		0.0	ns
t_{EABSU}	0.7		1.0		1.3		ns
t_{EABH}	0.4		0.6		0.8		ns
t_{EABCLR}	0.8		1.1		1.5		
t_{AA}		2.0		2.8		3.8	ns
t_{WP}	2.0		2.8		3.8		ns
t_{RP}	1.0		1.4		1.9		
t_{WDSU}	0.5		0.7		0.9		ns
t_{WDH}	0.1		0.1		0.2		ns
t_{WASU}	1.0		1.4		1.9		ns
t_{WAH}	1.5		2.1		2.9		ns
t_{RASU}	1.5		2.1		2.8		
t_{RAH}	0.1		0.1		0.2		
t_{WO}		2.1		2.9		4.0	ns
t_{DD}		2.1		2.9		4.0	ns
t_{EABOUT}		0.0		0.0		0.0	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	1.5		2.0		2.5		ns

Table 71. EPF10K50S External Timing Parameters   Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{DRR}$		8.0		9.5		12.5	ns
t$_{INSU}$ *(2)*	2.4		2.9		3.9		ns
t$_{INH}$ *(2)*	0.0		0.0		0.0		ns
t$_{OUTCO}$ *(2)*	2.0	4.3	2.0	5.2	2.0	7.3	ns
t$_{INSU}$ *(3)*	2.4		2.9				ns
t$_{INH}$ *(3)*	0.0		0.0				ns
t$_{OUTCO}$ *(3)*	0.5	3.3	0.5	4.1			ns
t$_{PCISU}$	2.4		2.9		–		ns
t$_{PCIH}$	0.0		0.0		–		ns
t$_{PCICO}$	2.0	6.0	2.0	7.7	–	–	ns

Table 72. EPF10K50S External Bidirectional Timing Parameters   Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{INSUBIDIR}$ *(2)*	2.7		3.2		4.3		ns
t$_{INHBIDIR}$ *(2)*	0.0		0.0		0.0		ns
t$_{INHBIDIR}$ *(3)*	0.0		0.0		–		ns
t$_{INSUBIDIR}$ *(3)*	3.7		4.2		–		ns
t$_{OUTCOBIDIR}$ *(2)*	2.0	4.5	2.0	5.2	2.0	7.3	ns
t$_{XZBIDIR}$ *(2)*		6.8		7.8		10.1	ns
t$_{ZXBIDIR}$ *(2)*		6.8		7.8		10.1	ns
t$_{OUTCOBIDIR}$ *(3)*	0.5	3.5	0.5	4.2	–	–	ns
t$_{XZBIDIR}$ *(3)*		6.8		8.4		–	ns
t$_{ZXBIDIR}$ *(3)*		6.8		8.4		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30.

(2) This parameter is measured without use of the ClockLock or ClockBoost circuits.

(3) This parameter is measured with use of the ClockLock or ClockBoost circuits

Power Consumption

The supply power (P) for FLEX 10KE devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times tog_{LC} \times \frac{\mu A}{MHz \times LE}$$

Where:

f_{MAX}	=	Maximum operating frequency in MHz
N	=	Total number of LEs used in the device
tog_{LC}	=	Average percent of LEs toggling at each clock (typically 12.5%)
K	=	Constant

Table 80 provides the constant (K) values for FLEX 10KE devices.

Table 80. FLEX 10KE K Constant Values	
Device	**K Value**
EPF10K30E	4.5
EPF10K50E	4.8
EPF10K50S	4.5
EPF10K100E	4.5
EPF10K130E	4.6
EPF10K200E	4.8
EPF10K200S	4.6

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

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Additionally, the Altera software offers several features that help plan for future device migration by preventing the use of conflicting I/O pins.

Table 81. I/O Counts for FLEX 10KA & FLEX 10KE Devices			
FLEX 10KA		**FLEX 10KE**	
Device	**I/O Count**	**Device**	**I/O Count**
EPF10K30AF256	191	EPF10K30EF256	176
EPF10K30AF484	246	EPF10K30EF484	220
EPF10K50VB356	274	EPF10K50SB356	220
EPF10K50VF484	291	EPF10K50EF484	254
EPF10K50VF484	291	EPF10K50SF484	254
EPF10K100AF484	369	EPF10K100EF484	338

Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see Table 82), chosen on the basis of the target application. An EPC1, EPC2, or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

Table 82. Data Sources for FLEX 10KE Configuration	
Configuration Scheme	**Data Source**
Configuration device	EPC1, EPC2, or EPC16 configuration device
Passive serial (PS)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL file or JBC file