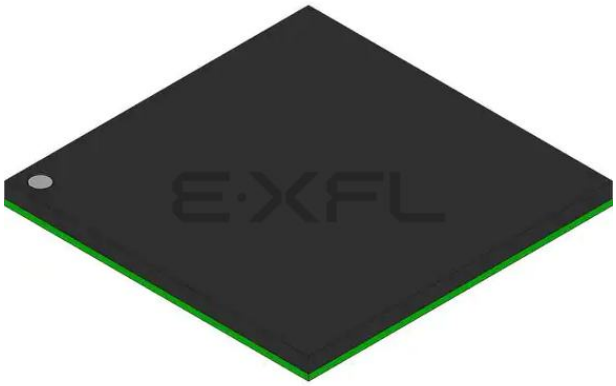
Altera - EPF10K100EFC484-2 Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	624
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	338
Number of Gates	-
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf10k100efc484-2

Table 4. FLEX 10KE Package Sizes

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	–	1.27	1.0
Area (mm^2)	484	936	1,197	289	1,225	529	3,904	2,025	729
Length × width (mm × mm)	22 × 22	30.6 × 30.6	34.6 × 34.6	17 × 17	35 × 35	23 × 23	62.5 × 62.5	45 × 45	27 × 27

General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

For more information on FLEX device configuration, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *MasterBlaster Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices)*

FLEX 10KE devices are supported by the Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

The Altera development system runs on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800.

See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

Cascade Chain

With the cascade chain, the FLEX 10KE architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. An a delay as low as 0.6 ns per LE, each additional LE provides four more inputs to the effective width of a function. Cascade chain logic can be created automatically by the Altera Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are implemented automatically by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EPF10K50E device, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 10 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. The LE delay is 0.9 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 2.7 ns are needed to decode a 16-bit address.

Figure 10. FLEX 10KE Cascade Chain Operation

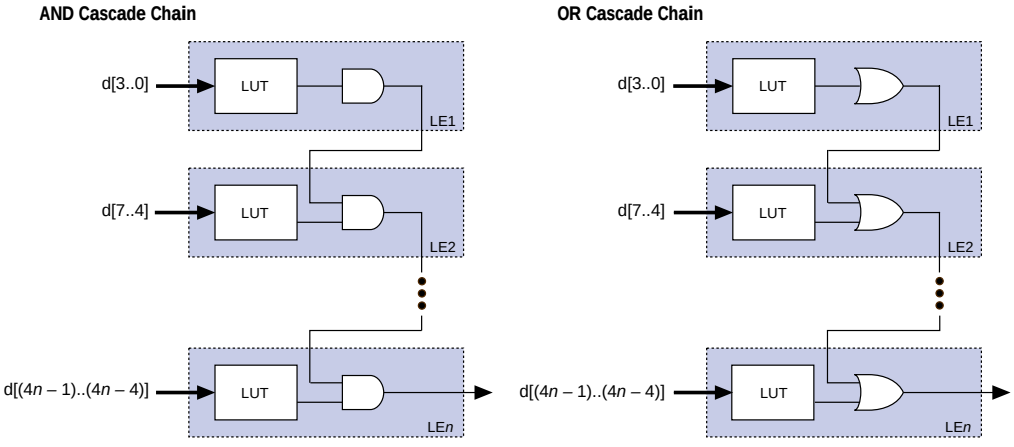
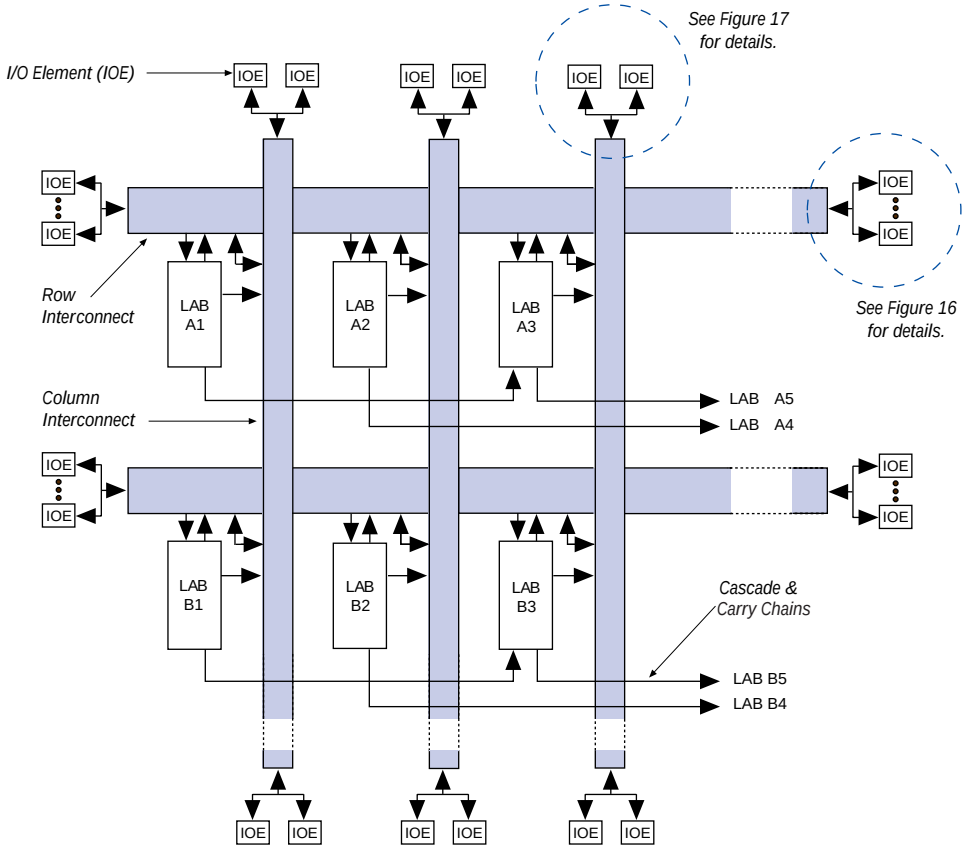


Figure 14. FLEX 10KE Interconnect Resources



I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE, and the data input and output enable registers should be LE registers placed adjacent to the bidirectional pin. The Altera Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Figure 15 shows the bidirectional I/O registers.

When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Tables 8 and 9 list the sources for each peripheral control signal, and show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. The tables also show the rows that can drive global signals.

Table 8. Peripheral Bus Sources for EPF10K30E, EPF10K50E & EPF10K50S Devices

Peripheral Control Signal	EPF10K30E	EPF10K50E EPF10K50S
OE0	Row A	Row A
OE1	Row B	Row B
OE2	Row C	Row D
OE3	Row D	Row F
OE4	Row E	Row H
OE5	Row F	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A
CLKENA1/OE6/GLOBAL1	Row B	Row C
CLKENA2/CLR0	Row C	Row E
CLKENA3/OE7/GLOBAL2	Row D	Row G
CLKENA4/CLR1	Row E	Row I
CLKENA5/CLK1/GLOBAL3	Row F	Row J

ClockLock & ClockBoost Features

To support high-speed designs, FLEX 10KE devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

All FLEX 10KE devices, except EPF10K50E and EPF10K200E devices, support ClockLock and ClockBoost circuitry. EPF10K50S and EPF10K200S devices support this circuitry. Devices that support ClockLock and ClockBoost circuitry are distinguished with an "X" suffix in the ordering code; for instance, the EPF10K200SFC672-1X device supports this circuit.

The ClockLock and ClockBoost features in FLEX 10KE devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (GCLK1) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to the GCLK1 pin. In the Altera software, the GCLK1 pin can feed both the ClockLock and ClockBoost circuitry in the FLEX 10KE device. However, when both circuits are used, the other clock pin cannot be used.

Table 13. ClockLock & ClockBoost Parameters for -2 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		75	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		37.5	MHz
f_{CLKDEV}	Input deviation from user specification in the MAX+PLUS II software *(1)*				25,000 *(2)*	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(3)*				10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(4)*	$t_{INCLKSTB}$ < 100			250	ps
		$t_{INCLKSTB}$ < 50			200 *(4)*	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Notes to tables:

(1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The Altera software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.

(4) The t_{JITTER} specification is measured under long-term observation. The maximum value for t_{JITTER} is 200 ps if $t_{INCLKSTB}$ is lower than 50 ps.

I/O Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for FLEX 10KE devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera software logic options. The MultiVolt I/O interface is controlled by connecting V_{CCIO} to a different voltage than V_{CCINT}. Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10KE devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. FLEX 10KE devices can also be configured using the JTAG pins through the BitBlaster or ByteBlasterMV download cable, or via hardware that uses the Jam™ STAPL programming and test language. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. FLEX 10KE devices support the JTAG instructions shown in Table 15.

Table 15. FLEX 10KE JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
USERCODE	Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a FLEX 10KE device via JTAG ports with a BitBlaster or ByteBlasterMV download cable, or using a Jam File (**.jam**) or Jam Byte-Code File (**.jbc**) via an embedded processor.

The instruction register length of FLEX 10KE devices is 10 bits. The USERCODE register length in FLEX 10KE devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. Tables 16 and 17 show the boundary-scan register length and device IDCODE information for FLEX 10KE devices.

Table 16. FLEX 10KE Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPF10K30E	690
EPF10K50E EPF10K50S	798
EPF10K100E	1,050
EPF10K130E	1,308
EPF10K200E EPF10K200S	1,446

Figure 20 shows the timing requirements for the JTAG signals.

Figure 20. FLEX 10KE JTAG Waveforms

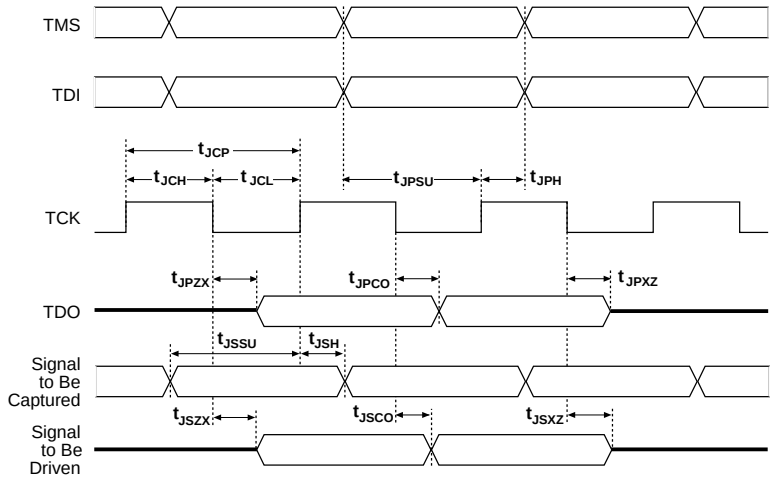


Table 18 shows the timing parameters and values for FLEX 10KE devices.

Table 18. FLEX 10KE JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Table 23. FLEX 10KE Device Capacitance *Note (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 V or 3.3 V.
(7) These values are specified under the FLEX 10KE Recommended Operating Conditions shown in Tables 20 and 21.
(8) The FLEX 10KE input buffers are compatible with 2.5-V, 3.3-V (LVTTL and LVCMOS), and 5.0-V TTL and CMOS signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 22.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) This value is specified for normal device operation. The value may vary during power-up.
(12) This parameter applies to -1 speed-grade commercial-temperature devices and -2 speed-grade-industrial temperature devices.
(13) Pin pull-up resistance values will be lower if the pin is driven higher than V_{CCIO} by an external source.
(14) Capacitance is sample-tested only.

Figure 25. FLEX 10KE Device LE Timing Model

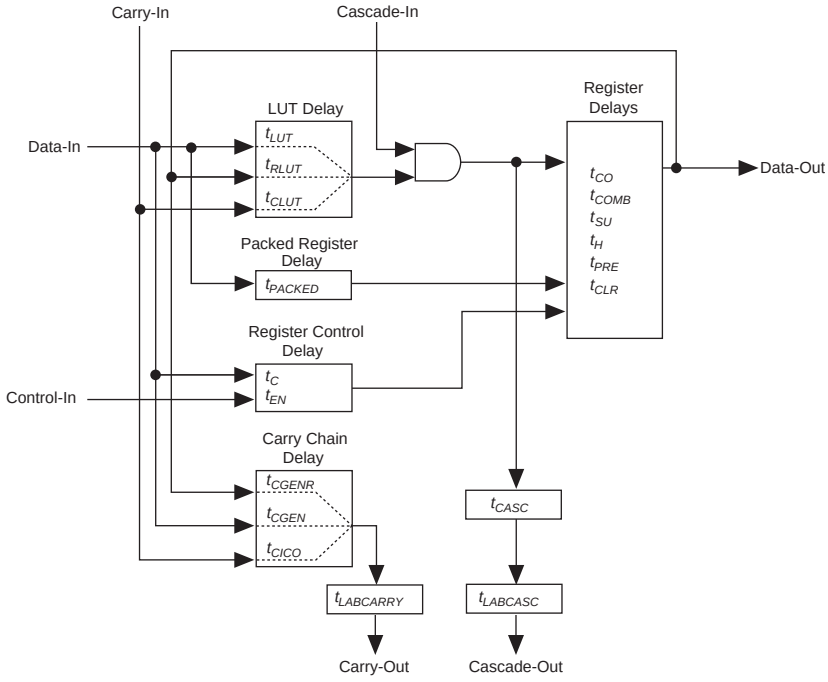


Table 24. LE Timing Microparameters (Part 2 of 2) *Note (1)*		
Symbol	**Parameter**	**Condition**
t_{CLR}	LE register clear delay	
t_{CH}	Minimum clock high time from clock pin	
t_{CL}	Minimum clock low time from clock pin	

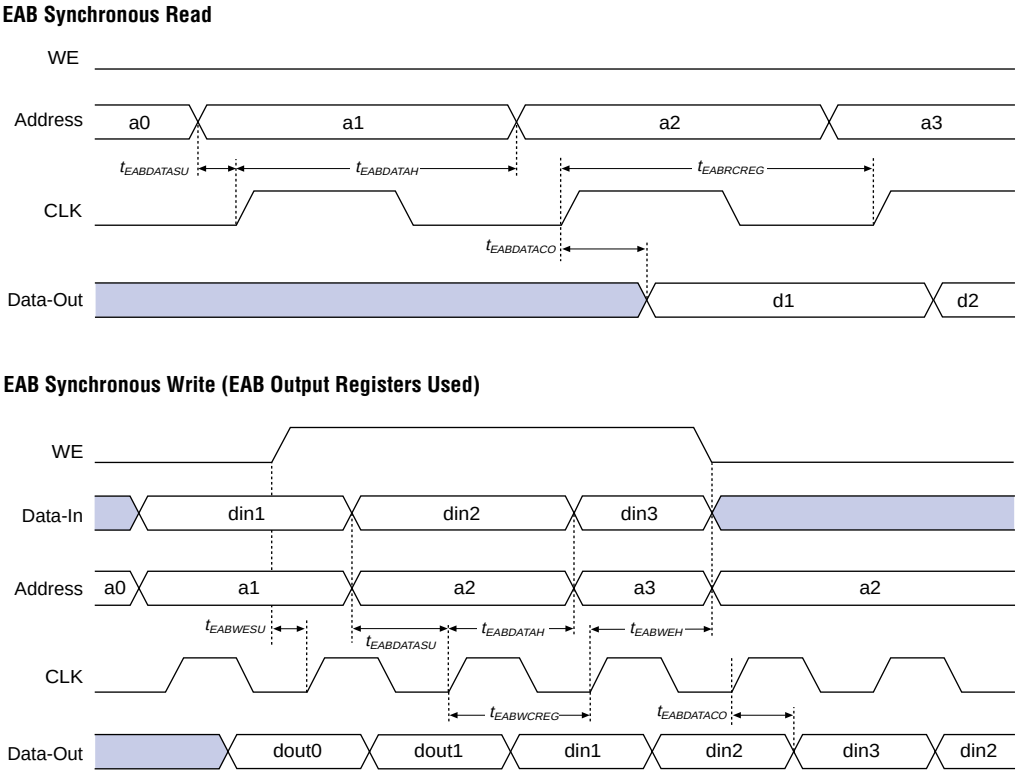
Table 25. IOE Timing Microparameters *Note (1)*		
Symbol	**Parameter**	**Conditions**
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
t_{IOH}	IOE register hold time for data and enable signals after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF *(3)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *(2)*
t_{ZX2}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF *(3)*
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Table 27. EAB Timing Macroparameters *Note (1), (6)*		
Symbol	**Parameter**	**Conditions**
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
t_{EABWEH}	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Table 28. Interconnect Timing Microparameters *Note (1)*		
Symbol	**Parameter**	**Conditions**
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*(7)*
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	*(7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*(7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	*(7)*
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	*(7)*
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*(7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*(7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*(7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*(7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*(7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Table 29. External Timing Parameters		
Symbol	**Parameter**	**Conditions**
$\mathbf{t_{DRR}}$	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	*(8)*
$\mathbf{t_{INSU}}$	Setup time with global clock at IOE register	*(9)*
$\mathbf{t_{INH}}$	Hold time with global clock at IOE register	*(9)*
$\mathbf{t_{OUTCO}}$	Clock-to-output delay with global clock at IOE register	*(9)*
$\mathbf{t_{PCISU}}$	Setup time with global clock for registers used in PCI designs	*(9)*,*(10)*
$\mathbf{t_{PCIH}}$	Hold time with global clock for registers used in PCI designs	*(9)*,*(10)*
$\mathbf{t_{PCICO}}$	Clock-to-output delay with global clock for registers used in PCI designs	*(9)*,*(10)*

Figure 30. EAB Synchronous Timing Waveforms



Tables 31 through 37 show EPF10K30E device internal and external timing parameters.

Table 31. EPF10K30E Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns

Table 50. EPF10K100E External Timing Parameters *Notes (1), (2)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		9.0		12.0		16.0	ns
t_{INSU} *(3)*	2.0		2.5		3.3		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.2	2.0	6.9	2.0	9.1	ns
t_{INSU} *(4)*	2.0		2.2		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	3.0	0.5	4.6	–	–	ns
t_{PCISU}	3.0		6.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	6.9	–	–	ns

Table 51. EPF10K100E External Bidirectional Timing Parameters *Notes (1), (2)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$ *(3)*	1.7		2.5		3.3		ns
$t_{INHBIDIR}$ *(3)*	0.0		0.0		0.0		ns
$t_{INSUBIDIR}$ *(4)*	2.0		2.8		–		ns
$t_{INHBIDIR}$ *(4)*	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ *(3)*	2.0	5.2	2.0	6.9	2.0	9.1	ns
$t_{XZBIDIR}$ *(3)*		5.6		7.5		10.1	ns
$t_{ZXBIDIR}$ *(3)*		5.6		7.5		10.1	ns
$t_{OUTCOBIDIR}$ *(4)*	0.5	3.0	0.5	4.6	–	–	ns
$t_{XZBIDIR}$ *(4)*		4.6		6.5		–	ns
$t_{ZXBIDIR}$ *(4)*		4.6		6.5		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Table 64. EPF10K200E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		10.0		12.0		16.0	ns
t_{INSU}	2.8		3.4		4.4		ns
t_{INH}	0.0		0.0		0.0		ns
t_{OUTCO}	2.0	4.5	2.0	5.3	2.0	7.8	ns
t_{PCISU}	3.0		6.2		-		ns
t_{PCIH}	0.0		0.0		-		ns
t_{PCICO}	2.0	6.0	2.0	8.9	-	-	ns

Table 65. EPF10K200E External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.0		4.0		5.5		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	4.5	2.0	5.3	2.0	7.8	ns
$t_{XZBIDIR}$		8.1		9.5		13.0	ns
$t_{ZXBIDIR}$		8.1		9.5		13.0	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.

Tables 66 through 79 show EPF10K50S and EPF10K200S device external timing parameters.

Table 66. EPF10K50S Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.6		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		0.9	ns
t_{PACKED}		0.2		0.3		0.4	ns
t_{EN}		0.6		0.7		0.9	ns
t_{CICO}		0.1		0.1		0.1	ns
t_{CGEN}		0.4		0.5		0.6	ns

Table 66. EPF10K50S Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CGENR}		0.1		0.1		0.1	ns
t_{CASC}		0.5		0.8		1.0	ns
t_{C}		0.5		0.6		0.8	ns
t_{CO}		0.6		0.6		0.7	ns
t_{COMB}		0.3		0.4		0.5	ns
t_{SU}	0.5		0.6		0.7		ns
t_{H}	0.5		0.6		0.8		ns
t_{PRE}		0.4		0.5		0.7	ns
t_{CLR}		0.8		1.0		1.2	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 67. EPF10K50S Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.3		1.3		1.9	ns
t_{IOC}		0.3		0.4		0.4	ns
t_{IOCO}		1.7		2.1		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		1.0		1.3		ns
t_{IOH}	0.4		0.5		0.6		ns
t_{IOCLR}		0.2		0.2		0.4	ns
t_{OD1}		1.2		1.2		1.9	ns
t_{OD2}		0.7		0.8		1.7	ns
t_{OD3}		2.7		3.0		4.3	ns
t_{XZ}		4.7		5.7		7.5	ns
t_{ZX1}		4.7		5.7		7.5	ns
t_{ZX2}		4.2		5.3		7.3	ns
t_{ZX3}		6.2		7.5		9.9	ns
t_{INREG}		3.5		4.2		5.6	ns
t_{IOFD}		1.1		1.3		1.8	ns
t_{INCOMB}		1.1		1.3		1.8	ns

Table 71. EPF10K50S External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		8.0		9.5		12.5	ns
t_{INSU} *(2)*	2.4		2.9		3.9		ns
t_{INH} *(2)*	0.0		0.0		0.0		ns
t_{OUTCO} *(2)*	2.0	4.3	2.0	5.2	2.0	7.3	ns
t_{INSU} *(3)*	2.4		2.9				ns
t_{INH} *(3)*	0.0		0.0				ns
t_{OUTCO} *(3)*	0.5	3.3	0.5	4.1			ns
t_{PCISU}	2.4		2.9		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	7.7	–	–	ns

Table 72. EPF10K50S External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ *(2)*	2.7		3.2		4.3		ns
$t_{INHBIDIR}$ *(2)*	0.0		0.0		0.0		ns
$t_{INHBIDIR}$ *(3)*	0.0		0.0		–		ns
$t_{INSUBIDIR}$ *(3)*	3.7		4.2		–		ns
$t_{OUTCOBIDIR}$ *(2)*	2.0	4.5	2.0	5.2	2.0	7.3	ns
$t_{XZBIDIR}$ *(2)*		6.8		7.8		10.1	ns
$t_{ZXBIDIR}$ *(2)*		6.8		7.8		10.1	ns
$t_{OUTCOBIDIR}$ *(3)*	0.5	3.5	0.5	4.2	–	–	
$t_{XZBIDIR}$ *(3)*		6.8		8.4		–	ns
$t_{ZXBIDIR}$ *(3)*		6.8		8.4		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30.
(2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with use of the ClockLock or ClockBoost circuits

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com