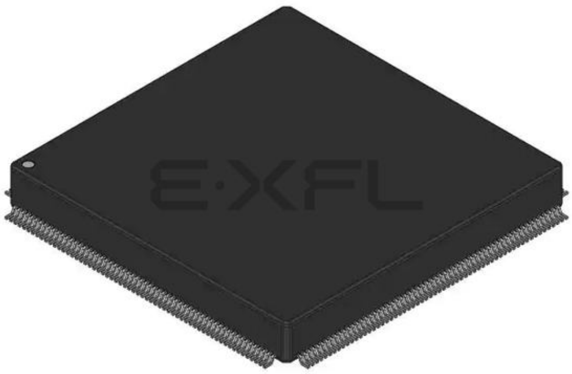

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	624
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	189
Number of Gates	-
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf10k100eqc240-2n

- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800
- Flexible package options
  - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see Tables 3 and 4)
  - SameFrame™ pin-out compatibility between FLEX 10KA and FLEX 10KE devices across a range of device densities and pin counts
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 3. FLEX 10KE Package Options & I/O Pin Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
EPF10K30E	102	147		176		220			220 *(3)*
EPF10K50E	102	147	189	191		254			254 *(3)*
EPF10K50S	102	147	189	191	220	254			254 *(3)*
EPF10K100E		147	189	191	274	338			338 *(3)*
EPF10K130E			186		274	369		424	413
EPF10K200E							470	470	470
EPF10K200S			182		274	369	470	470	470

Notes:

(1) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.

(3) This option is supported with a 484-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin, 484-pin, and 672-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

Functional Description

Each FLEX 10KE device contains an enhanced embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

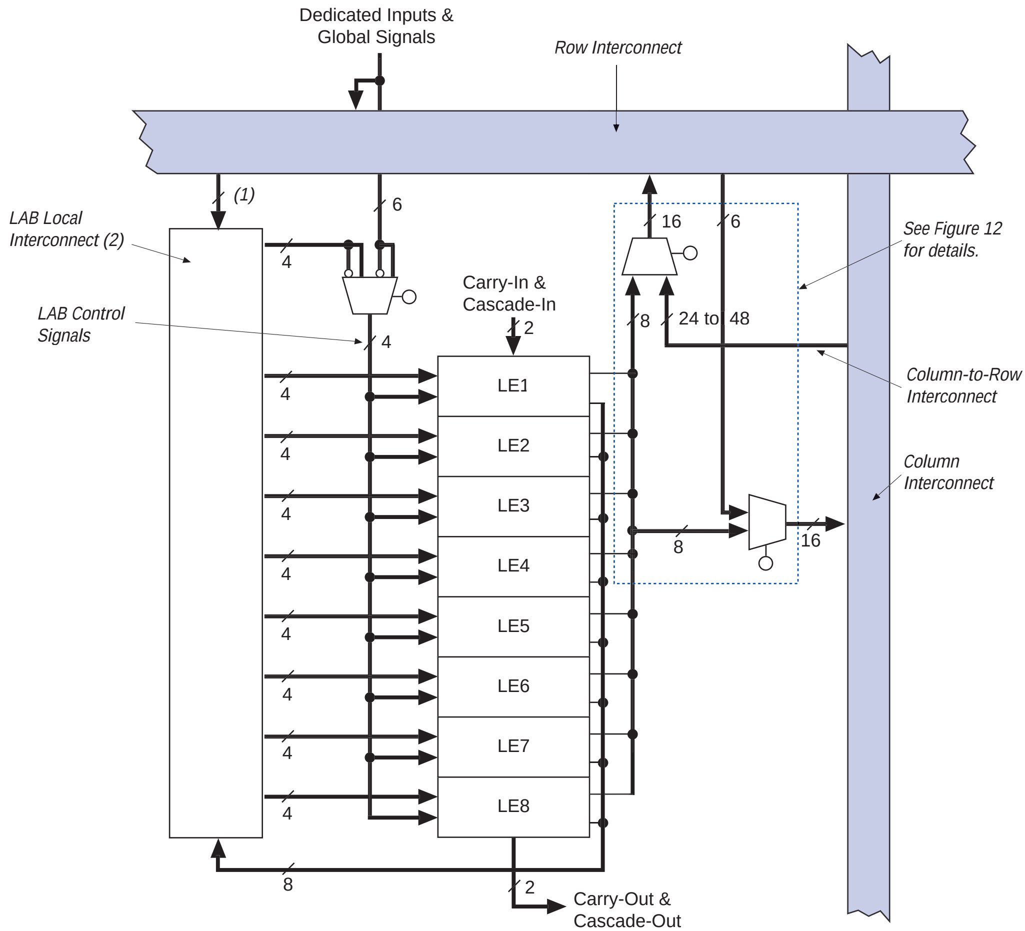
The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a four-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10KE devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 0.9 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 3.0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 7. FLEX 10KE LAB



Notes:

(1) EPF10K30E, EPF10K50E, and EPF10K50S devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 26.

(2) EPF10K30E, EPF10K50E, and EPF10K50S devices have 30 LAB local interconnect channels; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 34.

Figure 13. FLEX 10KE LAB Connections to Row & Column Interconnect

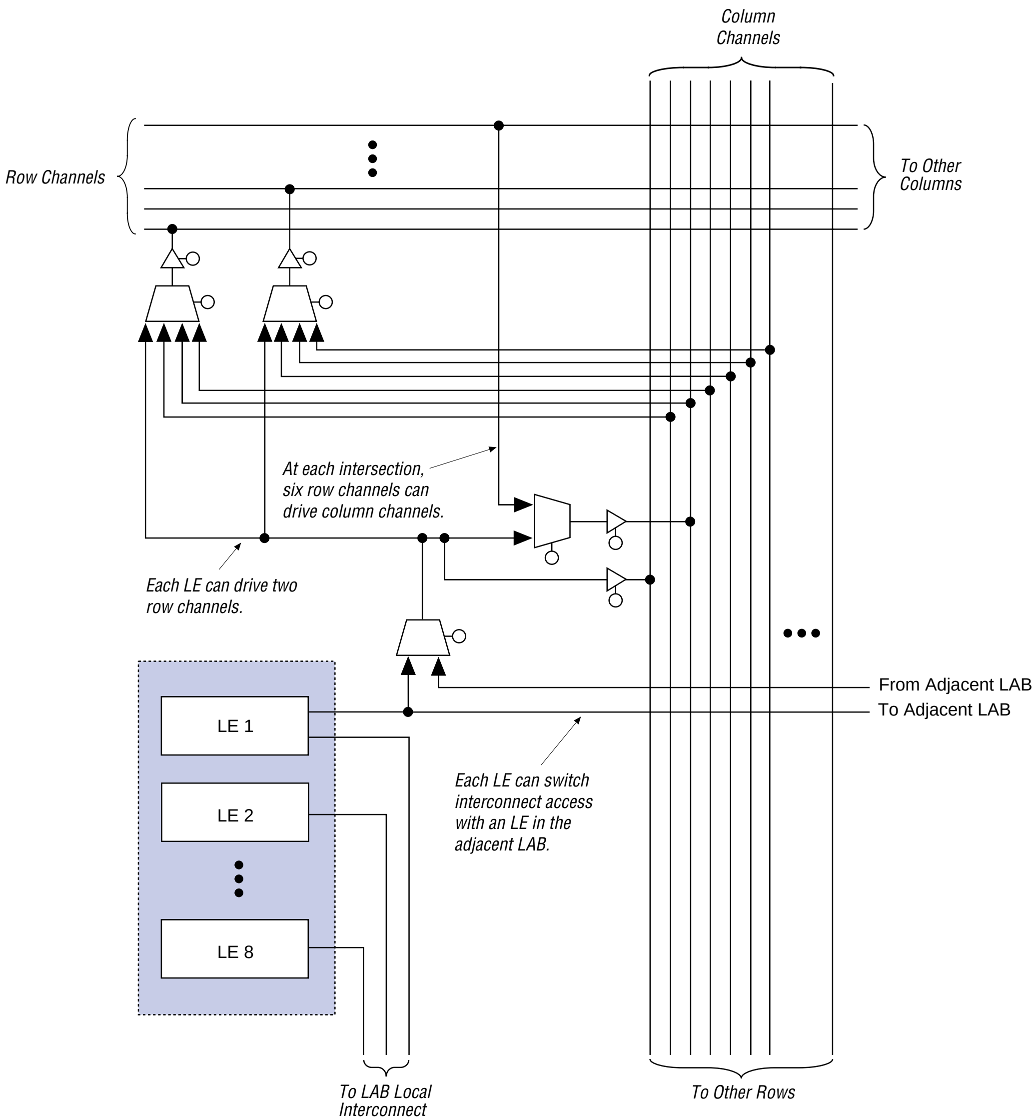


Table 9. Peripheral Bus Sources for EPF10K100E, EPF10K130E, EPF10K200E & EPF10K200S Devices

Peripheral Control Signal	EPF10K100E	EPF10K130E	EPF10K200E EPF10K200S
OE0	Row A	Row C	Row G
OE1	Row C	Row E	Row I
OE2	Row E	Row G	Row K
OE3	Row L	Row N	Row R
OE4	Row I	Row K	Row O
OE5	Row K	Row M	Row Q
CLKENA0/CLK0/GLOBAL0	Row F	Row H	Row L
CLKENA1/OE6/GLOBAL1	Row D	Row F	Row J
CLKENA2/CLR0	Row B	Row D	Row H
CLKENA3/OE7/GLOBAL2	Row H	Row J	Row N
CLKENA4/CLR1	Row J	Row L	Row P
CLKENA5/CLK1/GLOBAL3	Row G	Row I	Row M

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus, which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

The chip-wide output enable pin is an active-high pin (DEV_OE) that can be used to tri-state all pins on the device. This option can be set in the Altera software. On EPF10K50E and EPF10K200E devices, the built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

Figure 16. FLEX 10KE Row-to-IOE Connections

The values for m and n are provided in Table 10.

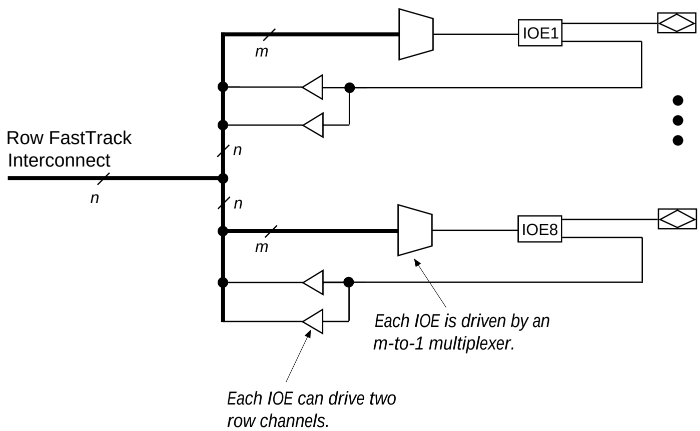


Table 10 lists the FLEX 10KE row-to-IOE interconnect resources.

Table 10. FLEX 10KE Row-to-IOE Interconnect Resources

Device	Channels per Row *(n)*	Row Channels per Pin *(m)*
EPF10K30E	216	27
EPF10K50E EPF10K50S	216	27
EPF10K100E	312	39
EPF10K130E	312	39
EPF10K200E EPF10K200S	312	39

The VCCINT pins must always be connected to a 2.5-V power supply. With a 2.5-V V_{CCINT} level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels higher than 3.0 V achieve a faster timing delay of t_{OD2} instead of t_{OD1}.

Table 14 summarizes FLEX 10KE MultiVolt I/O Support.

Table 14. FLEX 10KE MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

Notes:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, a FLEX 10KE device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on FLEX 10KE devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot-Socketing

Because FLEX 10KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into FLEX 10KE devices before and during power up without damaging the device. Additionally, FLEX 10KE devices do not drive out during power up. Once operating conditions are reached, FLEX 10KE devices operate as specified by the user.

Table 17. 32-Bit IDCODE for FLEX 10KE Devices *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPF10K30E	0001	0001 0000 0011 0000	00001101110	1
EPF10K50E EPF10K50S	0001	0001 0000 0101 0000	00001101110	1
EPF10K100E	0010	0000 0001 0000 0000	00001101110	1
EPF10K130E	0001	0000 0001 0011 0000	00001101110	1
EPF10K200E EPF10K200S	0001	0000 0010 0000 0000	00001101110	1

Notes:

(1) The most significant bit (MSB) is on the left.

(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10KE devices include weak pull-up resistors on the JTAG pins.

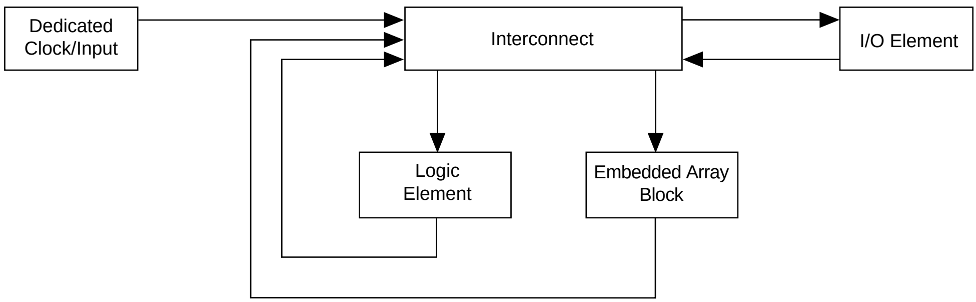
For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Timing simulation and delay prediction are available with the Altera Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10KE device.

Figure 24. FLEX 10KE Device Timing Model



Figures 25 through 28 show the delays that correspond to various paths and functions within the LE, IOE, EAB, and bidirectional timing models.

Table 26. EAB Timing Microparameters *Note (1)*		
Symbol	**Parameter**	**Conditions**
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
t_{EABWE1}	Write enable delay to EAB for combinatorial input	
t_{EABWE2}	Write enable delay to EAB for registered input	
t_{EABRE1}	Read enable delay to EAB for combinatorial input	
t_{EABRE2}	Read enable delay to EAB for registered input	
t_{EABCLK}	EAB register clock delay	
t_{EABCO}	EAB register clock-to-output delay	
$t_{EABBYPASS}$	Bypass register delay	
t_{EABSU}	EAB register setup time before clock	
t_{EABH}	EAB register hold time after clock	
t_{EABCLR}	EAB register asynchronous clear time to output delay	
t_{AA}	Address access delay (including the read enable to output delay)	
t_{WP}	Write pulse width	
t_{RP}	Read pulse width	
t_{WDSU}	Data setup time before falling edge of write pulse	*(5)*
t_{WDH}	Data hold time after falling edge of write pulse	*(5)*
t_{WASU}	Address setup time before rising edge of write pulse	*(5)*
t_{WAH}	Address hold time after falling edge of write pulse	*(5)*
t_{RASU}	Address setup time with respect to the falling edge of the read enable	
t_{RAH}	Address hold time with respect to the falling edge of the read enable	
t_{WO}	Write enable to data output valid delay	
t_{DD}	Data-in to data-out valid delay	
t_{EABOUT}	Data-out delay	
t_{EABCH}	Clock high time	
t_{EABCL}	Clock low time	

Table 30. External Bidirectional Timing Parameters *Note (9)*

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bi-directional pins with global clock at same-row or same-column LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
t_{INH}	Hold time with global clock at IOE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	C1 = 35 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate= off	C1 = 35 pF

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: VCCIO = 3.3 V ±10% for commercial or industrial use.
(3) Operating conditions: VCCIO = 2.5 V ±5% for commercial or industrial use in EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices.
(4) Operating conditions: VCCIO = 3.3 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(8) Contact Altera Applications for test circuit specifications and test conditions.
(9) This timing parameter is sample-tested only.
(10) This parameter is measured with the measurement and test conditions, including load, specified in the PCI Local Bus Specification, revision 2.2.

Table 33. EPF10K30E Device EAB Internal Microparameters Note (1)							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.7		2.0		2.3	ns
$t_{EABDATA1}$		0.6		0.7		0.8	ns
t_{EABWE1}		1.1		1.3		1.4	ns
t_{EABWE2}		0.4		0.4		0.5	ns
t_{EABRE1}		0.8		0.9		1.0	ns
t_{EABRE2}		0.4		0.4		0.5	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.4	ns
$t_{EABBYPASS}$		0.5		0.6		0.7	ns
t_{EABSU}	0.9		1.0		1.2		ns
t_{EABH}	0.4		0.4		0.5		ns
t_{EABCLR}	0.3		0.3		0.3		ns
t_{AA}		3.2		3.8		4.4	ns
t_{WP}	2.5		2.9		3.3		ns
t_{RP}	0.9		1.1		1.2		ns
t_{WDSU}	0.9		1.0		1.1		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.7		2.0		2.3		ns
t_{WAH}	1.8		2.1		2.4		ns
t_{RASU}	3.1		3.7		4.2		ns
t_{RAH}	0.2		0.2		0.2		ns
t_{WO}		2.5		2.9		3.3	ns
t_{DD}		2.5		2.9		3.3	ns
t_{EABOUT}		0.5		0.6		0.7	ns
t_{EABCH}	1.5		2.0		2.3		ns
t_{EABCL}	2.5		2.9		3.3		ns

Table 34. EPF10K30E Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		6.4		7.6		8.8	ns
$t_{EABRCOMB}$	6.4		7.6		8.8		ns
$t_{EABRCREG}$	4.4		5.1		6.0		ns
t_{EABWP}	2.5		2.9		3.3		ns
$t_{EABWCOMB}$	6.0		7.0		8.0		ns
$t_{EABWCREG}$	6.8		7.8		9.0		ns
t_{EABDD}		5.7		6.7		7.7	ns
$t_{EABDATACO}$		0.8		0.9		1.1	ns
$t_{EABDATASU}$	1.5		1.7		2.0		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.3		1.4		1.7		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.5		1.7		2.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.0		3.6		4.3		ns
t_{EABWAH}	0.5		0.5		0.4		ns
t_{EABWO}		5.1		6.0		6.8	ns

Table 37. EPF10K30E External Bidirectional Timing Parameters Notes (1), (2)							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$ (3)	2.8		3.9		5.2		ns
$t_{INHBIDIR}$ (3)	0.0		0.0		0.0		ns
$t_{INSUBIDIR}$ (4)	3.8		4.9		–		ns
$t_{INHBIDIR}$ (4)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{XZBIDIR}$ (3)		6.1		7.5		9.7	ns
$t_{ZXBIDIR}$ (3)		6.1		7.5		9.7	ns
$t_{OUTCOBIDIR}$ (4)	0.5	3.9	0.5	4.9	–	–	ns
$t_{XZBIDIR}$ (4)		5.1		6.5		–	ns
$t_{ZXBIDIR}$ (4)		5.1		6.5		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 38 through 44 show EPF10K50E device internal and external timing parameters.

Table 38. EPF10K50E Device LE Timing Microparameters (Part 1 of 2) Note (1)							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		0.6		0.9		1.3	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.7		0.8		1.1	ns
t_{PACKED}		0.4		0.5		0.6	ns
t_{EN}		0.6		0.7		0.9	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.5		0.5		0.8	ns
t_{CGENR}		0.2		0.2		0.3	ns
t_{CASC}		0.8		1.0		1.4	ns
t_{C}		0.5		0.6		0.8	ns
t_{CO}		0.7		0.7		0.9	ns
t_{COMB}		0.5		0.6		0.8	ns
t_{SU}	0.7		0.7		0.8		ns

Table 43. EPF10K50E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		8.5		10.0		13.5	ns
t_{INSU}	2.7		3.2		4.3		ns
t_{INH}	0.0		0.0		0.0		ns
t_{OUTCO}	2.0	4.5	2.0	5.2	2.0	7.3	ns
t_{PCISU}	3.0		4.2		-		ns
t_{PCIH}	0.0		0.0		-		ns
t_{PCICO}	2.0	6.0	2.0	7.7	-	-	ns

Table 44. EPF10K50E External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.7		3.2		4.3		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	4.5	2.0	5.2	2.0	7.3	ns
$t_{XZBIDIR}$		6.8		7.8		10.1	ns
$t_{ZXBIDIR}$		6.8		7.8		10.1	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.

(2) These parameters are specified by characterization.

Tables 45 through 51 show EPF10K100E device internal and external timing parameters.

Table 45. EPF10K100E Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		1.0		1.5	ns
t_{CLUT}		0.5		0.7		0.9	ns
t_{RLUT}		0.6		0.8		1.1	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.2		0.3		0.3	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns

Table 45. EPF10K100E Device LE Timing Microparameters *Note (1)*							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.6		0.9		1.2	ns
t_C		0.8		1.0		1.4	ns
t_{CO}		0.6		0.8		1.1	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	0.4		0.6		0.7		ns
t_H	0.5		0.7		0.9		ns
t_{PRE}		0.8		1.0		1.4	ns
t_{CLR}		0.8		1.0		1.4	ns
t_{CH}	1.5		2.0		2.5		ns
t_{CL}	1.5		2.0		2.5		ns

Table 46. EPF10K100E Device IOE Timing Microparameters *Note (1)*							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.7		2.0		2.6	ns
t_{IOC}		0.0		0.0		0.0	ns
t_{IOCO}		1.4		1.6		2.1	ns
t_{IOCOMB}		0.5		0.7		0.9	ns
t_{IOSU}	0.8		1.0		1.3		ns
t_{IOH}	0.7		0.9		1.2		ns
t_{IOCLR}		0.5		0.7		0.9	ns
t_{OD1}		3.0		4.2		5.6	ns
t_{OD2}		3.0		4.2		5.6	ns
t_{OD3}		4.0		5.5		7.3	ns
t_{XZ}		3.5		4.6		6.1	ns
t_{ZX1}		3.5		4.6		6.1	ns
t_{ZX2}		3.5		4.6		6.1	ns
t_{ZX3}		4.5		5.9		7.8	ns
t_{INREG}		2.0		2.6		3.5	ns
t_{IOFD}		0.5		0.8		1.2	ns
t_{INCOMB}		0.5		0.8		1.2	ns

Table 61. EPF10K200E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		2.0		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
t_{EABWE1}		1.4		1.7		2.3	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0		0		0	ns
t_{EABRE2}		0.4		0.5		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		0.9		1.2	ns
$t_{EABBYPASS}$		0.0		0.1		0.1	ns
t_{EABSU}	0.9		1.1		1.5		ns
t_{EABH}	0.4		0.5		0.6		ns
t_{EABCLR}	0.8		0.9		1.2		ns
t_{AA}		3.1		3.7		4.9	ns
t_{WP}	3.3		4.0		5.3		ns
t_{RP}	0.9		1.1		1.5		ns
t_{WDSU}	0.9		1.1		1.5		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.3		1.6		2.1		ns
t_{WAH}	2.1		2.5		3.3		ns
t_{RASU}	2.2		2.6		3.5		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		2.0		2.4		3.2	ns
t_{DD}		2.0		2.4		3.2	ns
t_{EABOUT}		0.0		0.1		0.1	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	3.3		4.0		5.3		ns

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.1		6.4		8.4	ns
$t_{EABRCOMB}$	5.1		6.4		8.4		ns
$t_{EABRCREG}$	4.8		5.7		7.6		ns
t_{EABWP}	3.3		4.0		5.3		ns

Table 71. EPF10K50S External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		8.0		9.5		12.5	ns
t_{INSU} *(2)*	2.4		2.9		3.9		ns
t_{INH} *(2)*	0.0		0.0		0.0		ns
t_{OUTCO} *(2)*	2.0	4.3	2.0	5.2	2.0	7.3	ns
t_{INSU} *(3)*	2.4		2.9				ns
t_{INH} *(3)*	0.0		0.0				ns
t_{OUTCO} *(3)*	0.5	3.3	0.5	4.1			ns
t_{PCISU}	2.4		2.9		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	7.7	–	–	ns

Table 72. EPF10K50S External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ *(2)*	2.7		3.2		4.3		ns
$t_{INHBIDIR}$ *(2)*	0.0		0.0		0.0		ns
$t_{INHBIDIR}$ *(3)*	0.0		0.0		–		ns
$t_{INSUBIDIR}$ *(3)*	3.7		4.2		–		ns
$t_{OUTCOBIDIR}$ *(2)*	2.0	4.5	2.0	5.2	2.0	7.3	ns
$t_{XZBIDIR}$ *(2)*		6.8		7.8		10.1	ns
$t_{ZXBIDIR}$ *(2)*		6.8		7.8		10.1	ns
$t_{OUTCOBIDIR}$ *(3)*	0.5	3.5	0.5	4.2	–	–	
$t_{XZBIDIR}$ *(3)*		6.8		8.4		–	ns
$t_{ZXBIDIR}$ *(3)*		6.8		8.4		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30.
(2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with use of the ClockLock or ClockBoost circuits

Table 73. EPF10K200S Device Internal & External Timing Parameters *Note (1)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		0.7		0.8		1.2	ns
t_{CLUT}		0.4		0.5		0.6	ns
t_{RLUT}		0.5		0.7		0.9	ns
t_{PACKED}		0.4		0.5		0.7	ns
t_{EN}		0.6		0.5		0.6	ns
t_{CICO}		0.1		0.2		0.3	ns
t_{CGEN}		0.3		0.4		0.6	ns
t_{CGENR}		0.1		0.2		0.3	ns
t_{CASC}		0.7		0.8		1.2	ns
t_{C}		0.5		0.6		0.8	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.3		0.6		0.8	ns
t_{SU}	0.4		0.6		0.7		ns
t_{H}	1.0		1.1		1.5		ns
t_{PRE}		0.4		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 74. EPF10K200S Device IOE Timing Microparameters (Part 1 of 2) *Note (1)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.8		1.9		2.6	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		1.7		1.9		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		0.9		1.2		ns
t_{IOH}	0.4		0.8		1.1		ns
t_{IOCLR}		0.2		0.2		0.3	ns
t_{OD1}		1.3		0.7		0.9	ns
t_{OD2}		0.8		0.2		0.4	ns
t_{OD3}		2.9		3.0		3.9	ns
t_{XZ}		5.0		5.3		7.1	ns
t_{ZX1}		5.0		5.3		7.1	ns

Table 74. EPF10K200S Device IOE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ZX2}		4.5		4.8		6.6	ns
t_{ZX3}		6.6		7.6		10.1	ns
t_{INREG}		3.7		5.7		7.7	ns
t_{IOFD}		1.8		3.4		4.0	ns
t_{INCOMB}		1.8		3.4		4.0	ns

Table 75. EPF10K200S Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
t_{EABWE1}		1.1		1.7		2.3	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0		0		0	ns
t_{EABRE2}		0.4		0.5		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		0.9		1.2	ns
$t_{EABBYPASS}$		0.0		0.1		0.1	ns
t_{EABSU}	0.7		1.1		1.5		ns
t_{EABH}	0.4		0.5		0.6		ns
t_{EABCLR}	0.8		0.9		1.2		ns
t_{AA}		2.1		3.7		4.9	ns
t_{WP}	2.1		4.0		5.3		ns
t_{RP}	1.1		1.1		1.5		ns
t_{WDSU}	0.5		1.1		1.5		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.1		1.6		2.1		ns
t_{WAH}	1.6		2.5		3.3		ns
t_{RASU}	1.6		2.6		3.5		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		2.0		2.4		3.2	ns
t_{DD}		2.0		2.4		3.2	ns
t_{EABOUT}		0.0		0.1		0.1	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.1		2.8		3.8		ns