



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

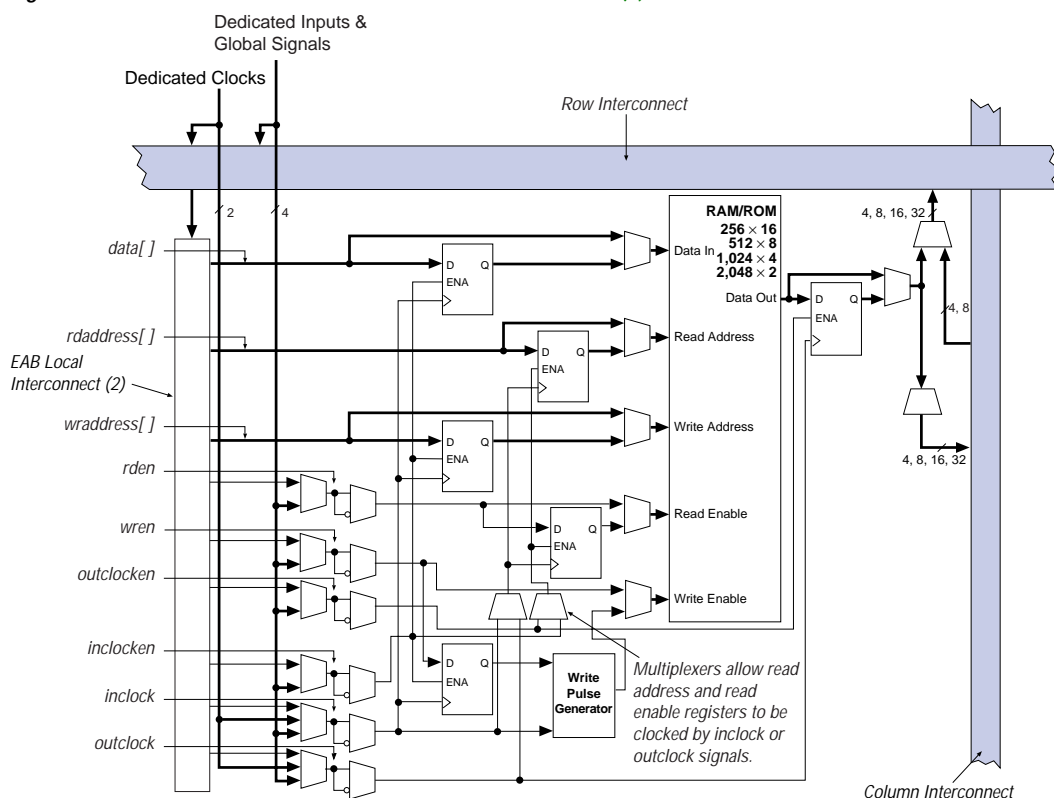
#### Details

Product Status	Obsolete
Number of LABs/CLBs	72
Number of Logic Elements/Cells	576
Total RAM Bits	6144
Number of I/O	102
Number of Gates	31000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf10k10tc144-4">https://www.e-xfl.com/product-detail/intel/epf10k10tc144-4</a>

The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous read or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see Figure 2).

Figure 2. FLEX 10KE Device in Dual-Port RAM Mode Notes (1)



#### Notes:

- (1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
- (2) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, and EPF10K200E devices have 104 EAB local interconnect channels.

### **Asynchronous Clear**

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

### **Asynchronous Preset**

An asynchronous preset is implemented as an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

### **Asynchronous Preset & Clear**

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, so that asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

### **Asynchronous Load with Clear**

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

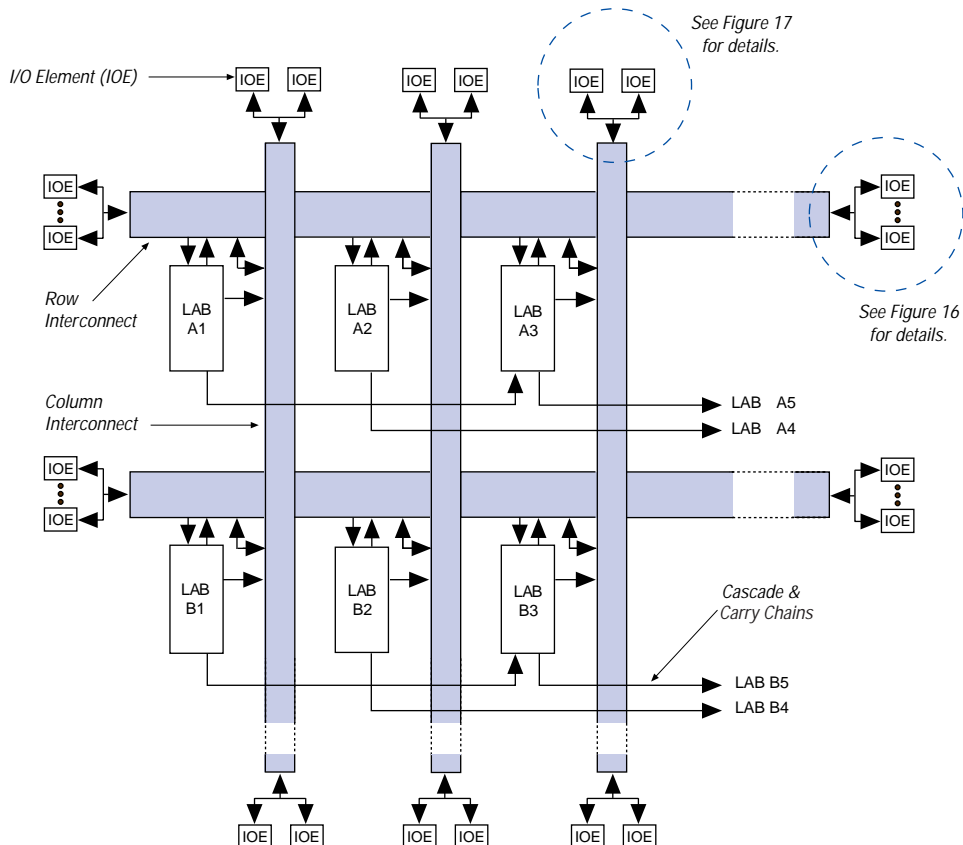
### **Asynchronous Load with Preset**

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

### **Asynchronous Load without Preset or Clear**

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

Figure 14. FLEX 10KE Interconnect Resources



## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE, and the data input and output enable registers should be LE registers placed adjacent to the bidirectional pin. The Altera Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. [Figure 15](#) shows the bidirectional I/O registers.

On all FLEX 10KE devices (except EPF10K50E and EPF10K200E devices), the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. EPF10K50S and EPF10K200S devices also support this feature. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across the device and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on a LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

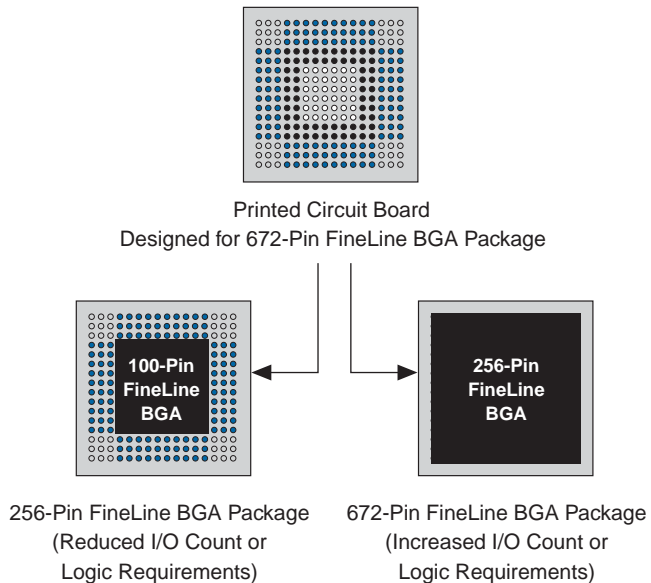
When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

## SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K200S device in a 672-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 18](#)).

*Figure 18. SameFrame Pin-Out Example*



## ClockLock & ClockBoost Features

To support high-speed designs, FLEX 10KE devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

All FLEX 10KE devices, except EPF10K50E and EPF10K200E devices, support ClockLock and ClockBoost circuitry. EPF10K50S and EPF10K200S devices support this circuitry. Devices that support ClockLock and ClockBoost circuitry are distinguished with an "X" suffix in the ordering code; for instance, the EPF10K200SFC672-1X device supports this circuit.

The ClockLock and ClockBoost features in FLEX 10KE devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (`GCLK1`) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to the `GCLK1` pin. In the Altera software, the `GCLK1` pin can feed both the ClockLock and ClockBoost circuitry in the FLEX 10KE device. However, when both circuits are used, the other clock pin cannot be used.

The  $V_{CCINT}$  pins must always be connected to a 2.5-V power supply. With a 2.5-V  $V_{CCINT}$  level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The  $V_{CCIO}$  pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels higher than 3.0 V achieve a faster timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

Table 14 summarizes FLEX 10KE MultiVolt I/O support.

Table 14. FLEX 10KE MultiVolt I/O Support						
$V_{CCIO}$ (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

**Notes:**

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than  $V_{CCIO}$ .
- (2) When  $V_{CCIO} = 3.3$  V, a FLEX 10KE device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on FLEX 10KE devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a  $V_{IH}$  of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

## Power Sequencing & Hot-Socketing

Because FLEX 10KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into FLEX 10KE devices before and during power up without damaging the device. Additionally, FLEX 10KE devices do not drive out during power up. Once operating conditions are reached, FLEX 10KE devices operate as specified by the user.



## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10KE devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. FLEX 10KE devices can also be configured using the JTAG pins through the BitBlaster or ByteBlasterMV download cable, or via hardware that uses the Jam™ STAPL programming and test language. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. FLEX 10KE devices support the JTAG instructions shown in [Table 15](#).

*Table 15. FLEX 10KE JTAG Instructions*

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
USERCODE	Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a FLEX 10KE device via JTAG ports with a BitBlaster or ByteBlasterMV download cable, or using a Jam File (.jam) or Jam Byte-Code File (.jbc) via an embedded processor.

The instruction register length of FLEX 10KE devices is 10 bits. The USERCODE register length in FLEX 10KE devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. [Tables 16](#) and [17](#) show the boundary-scan register length and device IDCODE information for FLEX 10KE devices.

*Table 16. FLEX 10KE Boundary-Scan Register Length*

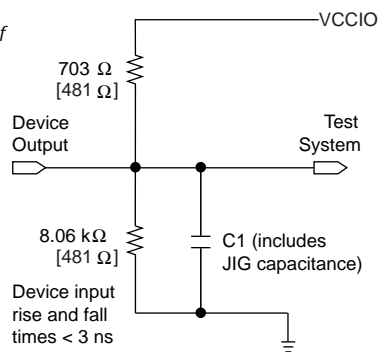
Device	Boundary-Scan Register Length
EPF10K30E	690
EPF10K50E EPF10K50S	798
EPF10K100E	1,050
EPF10K130E	1,308
EPF10K200E EPF10K200S	1,446

## Generic Testing

Each FLEX 10KE device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in [Figure 21](#). Multiple test patterns can be used to configure devices during all stages of the production flow.

**Figure 21. FLEX 10KE AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.



## Operating Conditions

[Tables 19](#) through [23](#) provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V FLEX 10KE devices.

**Table 19. FLEX 10KE 2.5-V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage	With respect to ground (2)	–0.5	3.6	V
$V_{CCIO}$			–0.5	4.6	V
$V_I$	DC input voltage		–2.0	5.75	V
$I_{OUT}$	DC output current, per pin		–25	25	mA
$T_{STG}$	Storage temperature	No bias	–65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	–65	135	°C
$T_J$	Junction temperature	PQFP, TQFP, BGA, and FineLine BGA packages, under bias		135	°C
		Ceramic PGA packages, under bias		150	°C

Table 22. FLEX 10KE 2.5-V Device DC Operating Conditions

Notes (6), (7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ (8)		5.75	V
$V_{IL}$	Low-level input voltage		-0.5		0.8, $0.3 \times V_{CCIO}$ (8)	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (9)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (9)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to $3.60$ V (9)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (9)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (9)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (9)	1.7			V
$V_{OL}$	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (10)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (10)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5$ mA DC, $V_{CCIO} = 3.00$ to $3.60$ V (10)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 2.30$ V (10)			0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (10)			0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (10)			0.7	V
$I_I$	Input pin leakage current	$V_I = V_{CCIOmax}$ to $0$ V (11)	-10		10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to $0$ V (11)	-10		10	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I =$ ground, no load, no toggling inputs		5		mA
		$V_I =$ ground, no load, no toggling inputs (12)		10		mA
$R_{CONF}$	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0$ V (13)	20		50	$k\frac{3}{4}$
		$V_{CCIO} = 2.3$ V (13)	30		80	$k\frac{3}{4}$

Figure 26. FLEX 10KE Device IOE Timing Model

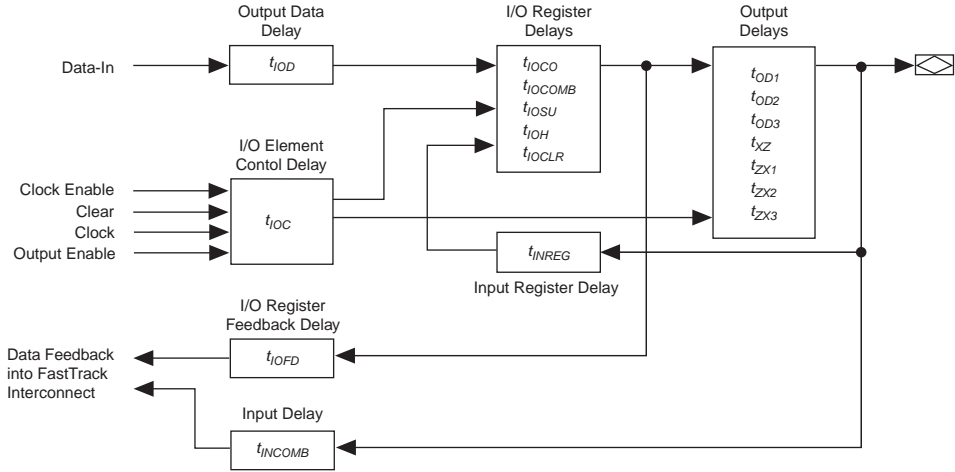


Figure 27. FLEX 10KE Device EAB Timing Model

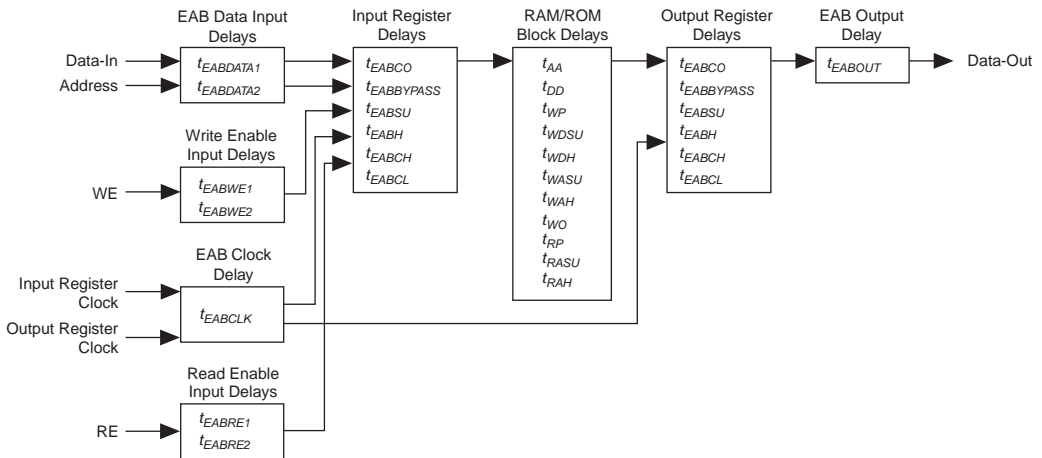


Table 33. EPF10K30E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.0		2.3	ns
$t_{EABDATA1}$		0.6		0.7		0.8	ns
$t_{EABWE1}$		1.1		1.3		1.4	ns
$t_{EABWE2}$		0.4		0.4		0.5	ns
$t_{EABRE1}$		0.8		0.9		1.0	ns
$t_{EABRE2}$		0.4		0.4		0.5	ns
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.3		0.3		0.4	ns
$t_{EABYPASS}$		0.5		0.6		0.7	ns
$t_{EABSU}$	0.9		1.0		1.2		ns
$t_{EABH}$	0.4		0.4		0.5		ns
$t_{EABCLR}$	0.3		0.3		0.3		ns
$t_{AA}$		3.2		3.8		4.4	ns
$t_{WP}$	2.5		2.9		3.3		ns
$t_{RP}$	0.9		1.1		1.2		ns
$t_{WDSU}$	0.9		1.0		1.1		ns
$t_{WDH}$	0.1		0.1		0.1		ns
$t_{WASU}$	1.7		2.0		2.3		ns
$t_{WAH}$	1.8		2.1		2.4		ns
$t_{RASU}$	3.1		3.7		4.2		ns
$t_{RAH}$	0.2		0.2		0.2		ns
$t_{WO}$		2.5		2.9		3.3	ns
$t_{DD}$		2.5		2.9		3.3	ns
$t_{EABOUT}$		0.5		0.6		0.7	ns
$t_{EABCH}$	1.5		2.0		2.3		ns
$t_{EABCL}$	2.5		2.9		3.3		ns

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
$t_{DIN2LE}$		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DDR}$		8.0		9.5		12.5	ns
$t_{INSU}$ (3)	2.1		2.5		3.9		ns
$t_{INH}$ (3)	0.0		0.0		0.0		ns
$t_{OUTCO}$ (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{INSU}$ (4)	1.1		1.5		—		ns
$t_{INH}$ (4)	0.0		0.0		—		ns
$t_{OUTCO}$ (4)	0.5	3.9	0.5	4.9	—	—	ns
$t_{PCISU}$	3.0		4.2		—		ns
$t_{PCIH}$	0.0		0.0		—		ns
$t_{PCICO}$	2.0	6.0	2.0	7.5	—	—	ns

Table 38. EPF10K50E Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_H$	0.9		1.0		1.4		ns
$t_{PRE}$		0.5		0.6		0.8	ns
$t_{CLR}$		0.5		0.6		0.8	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns

Table 39. EPF10K50E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		2.2		2.4		3.3	ns
$t_{IOC}$		0.3		0.3		0.5	ns
$t_{IOCO}$		1.0		1.0		1.4	ns
$t_{IOCOMB}$		0.0		0.0		0.2	ns
$t_{IOSU}$	1.0		1.2		1.7		ns
$t_{IOH}$	0.3		0.3		0.5		ns
$t_{IOCLR}$		0.9		1.0		1.4	ns
$t_{OD1}$		0.8		0.9		1.2	ns
$t_{OD2}$		0.3		0.4		0.7	ns
$t_{OD3}$		3.0		3.5		3.5	ns
$t_{XZ}$		1.4		1.7		2.3	ns
$t_{ZX1}$		1.4		1.7		2.3	ns
$t_{ZX2}$		0.9		1.2		1.8	ns
$t_{ZX3}$		3.6		4.3		4.6	ns
$t_{INREG}$		4.9		5.8		7.8	ns
$t_{IOFD}$		2.8		3.3		4.5	ns
$t_{INCOMB}$		2.8		3.3		4.5	ns

Table 40. EPF10K50E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.0		2.7	ns
$t_{EABDATA1}$		0.6		0.7		0.9	ns
$t_{EABWE1}$		1.1		1.3		1.8	ns
$t_{EABWE2}$		0.4		0.4		0.6	ns
$t_{EABRE1}$		0.8		0.9		1.2	ns
$t_{EABRE2}$		0.4		0.4		0.6	ns
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.3		0.3		0.5	ns
$t_{EABYPASS}$		0.5		0.6		0.8	ns
$t_{EABSU}$	0.9		1.0		1.4		ns
$t_{EABH}$	0.4		0.4		0.6		ns
$t_{EABCLR}$	0.3		0.3		0.5		ns
$t_{AA}$		3.2		3.8		5.1	ns
$t_{WP}$	2.5		2.9		3.9		ns
$t_{RP}$	0.9		1.1		1.5		ns
$t_{WDSU}$	0.9		1.0		1.4		ns
$t_{WDH}$	0.1		0.1		0.2		ns
$t_{WASU}$	1.7		2.0		2.7		ns
$t_{WAH}$	1.8		2.1		2.9		ns
$t_{RASU}$	3.1		3.7		5.0		ns
$t_{RAH}$	0.2		0.2		0.3		ns
$t_{WO}$		2.5		2.9		3.9	ns
$t_{DD}$		2.5		2.9		3.9	ns
$t_{EABOUT}$		0.5		0.6		0.8	ns
$t_{EABCH}$	1.5		2.0		2.5		ns
$t_{EABCL}$	2.5		2.9		3.9		ns



Table 68. EPF10K50S Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.4		3.2	ns
$t_{EABDATA2}$		0.4		0.6		0.8	ns
$t_{EABWE1}$		1.0		1.4		1.9	ns
$t_{EABWE2}$		0.0		0.0		0.0	ns
$t_{EABRE1}$		0.0		0.0		0.0	
$t_{EABRE2}$		0.4		0.6		0.8	
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.8		1.1		1.5	ns
$t_{EABYPASS}$		0.0		0.0		0.0	ns
$t_{EABSU}$	0.7		1.0		1.3		ns
$t_{EABH}$	0.4		0.6		0.8		ns
$t_{EABCLR}$	0.8		1.1		1.5		
$t_{AA}$		2.0		2.8		3.8	ns
$t_{WP}$	2.0		2.8		3.8		ns
$t_{RP}$	1.0		1.4		1.9		
$t_{WDSU}$	0.5		0.7		0.9		ns
$t_{WDH}$	0.1		0.1		0.2		ns
$t_{WASU}$	1.0		1.4		1.9		ns
$t_{WAH}$	1.5		2.1		2.9		ns
$t_{RASU}$	1.5		2.1		2.8		
$t_{RAH}$	0.1		0.1		0.2		
$t_{WO}$		2.1		2.9		4.0	ns
$t_{DD}$		2.1		2.9		4.0	ns
$t_{EABOUT}$		0.0		0.0		0.0	ns
$t_{EABCH}$	1.5		2.0		2.5		ns
$t_{EABCL}$	1.5		2.0		2.5		ns

Table 69. EPF10K50S Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
$t_{EABWP}$	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
$t_{EABDD}$		3.8		5.3		7.2	ns
$t_{EABDATACO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
$t_{EABWEH}$	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
$t_{EABWAH}$	0.9		1.2		1.8		ns
$t_{EABWO}$		3.1		4.3		5.9	ns

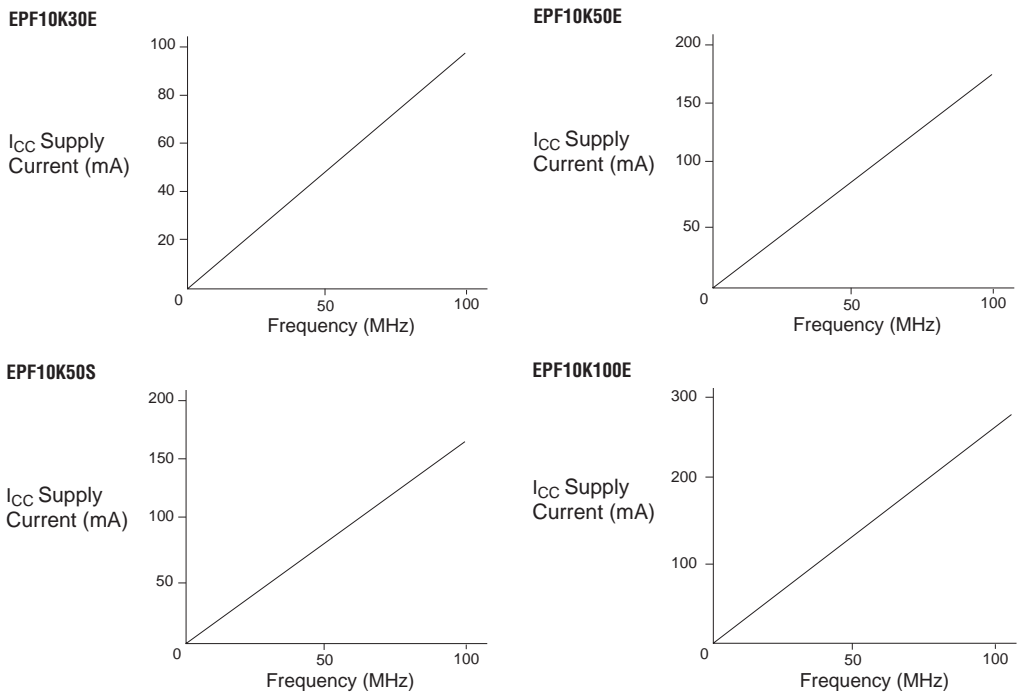
Table 70. EPF10K50S Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.7		4.6	ns
$t_{DIN2LE}$		1.7		2.1		2.7	ns
$t_{DIN2DATA}$		2.7		3.1		5.1	ns
$t_{DCLK2IOE}$		1.6		1.9		2.6	ns
$t_{DCLK2LE}$		1.7		2.1		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		1.7		2.4	ns
$t_{SAMECOLUMN}$		1.0		1.3		2.1	ns
$t_{DIFFROW}$		2.5		3.0		4.5	ns
$t_{TWOROWS}$		4.0		4.7		6.9	ns
$t_{LEPERIPH}$		2.6		2.9		3.4	ns
$t_{LABCARRY}$		0.1		0.2		0.2	ns
$t_{LABCASC}$		0.8		1.0		1.3	ns

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect FLEX devices assumes that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results when compared to measured power consumption for actual designs in segmented FPGAs.

Figure 31 shows the relationship between the current and operating frequency of FLEX 10KE devices.

Figure 31. FLEX 10KE  $I_{CCACTIVE}$  vs. Operating Frequency (Part 1 of 2)



## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the Altera Digital Library for pin-out information.

## Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

### Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to **Figure 23**.
- Text added to “**I/O Element**” section on **page 34**.
- Updated **Table 22**.

### Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on **page 34** and **page 63**.



101 Innovation Drive  
San Jose, CA 95134  
(408) 544-7000  
<http://www.altera.com>  
**Applications Hotline:**  
(800) 800-EPLD  
**Literature Services:**  
[lit\\_req@altera.com](mailto:lit_req@altera.com)

Copyright © 2003 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

